Department of Electrical and Computer Engineering  
CPEN 430  
DIGITAL SYSTEM DESIGN  
☐ Required  ☒ Elective  

<table>
<thead>
<tr>
<th>AY</th>
<th>Revision History: Changes and Rationale</th>
<th>Progress Exam Affected?</th>
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</thead>
<tbody>
<tr>
<td>07/08</td>
<td>Syllabus Created</td>
<td>N</td>
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<tr>
<td>11/12</td>
<td>Syllabus Updated</td>
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<tr>
<td>14/15</td>
<td>Syllabus Updated</td>
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Coordinator: Claudio Talarico, Professor, Electrical and Computer Engineering

Catalog Description: Modern methods of digital design realization. Technology independence. Designs utilizing gate arrays and custom integrated circuits. Use of high level design software. Extensive use of VHDL hardware design language for system description, simulation and implementation. Three hours lecture per week. Prerequisites: CPEN 230 and CPSC 121.

Prerequisites by Topic:
1. Introduction to Digital Logic  
2. C or Python Programming

Textbook(s) / Require Mat’l: Circuit Design and Simulation with VHDL by V. Pedroni, 2/e, MIT Press, 2010

Course Topics:
1. Analysis of clocked synchronous sequential logic networks. (12 hours)  
2. Design of clocked synchronous sequential logic networks. (24 hours)  
3. Examinations. (6 hours)

Course Objectives:
1. To teach the student understanding of synchronous digital logic design techniques  
2. To teach the student tools for programming logic on programmable logic devices  
3. To teach the student practical knowledge required to design, implement and test digital systems
### Professional Components/Course Outcomes:

By the end of this course the student will be able to:

1. Decompose a digital system into datapath and control modules
2. Use VHDL to implement logic modules
3. Program, integrate and test a digital system on a FPGA chip
4. Document the design in a formal report

### Class/Lab Schedule:

- 150 minutes of lecture each week; 3 x 50 minute or 2 x 75 minute sessions
- 3 credit hours

### Relation to Program Outcomes:

<table>
<thead>
<tr>
<th></th>
<th>(a) Fundamental math, science, or engineering</th>
<th>(b) Experimentation</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>(c) Design</td>
<td>(d) Teamwork</td>
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<td></td>
<td>(e) Problem solving</td>
<td>(f) Professional ethics</td>
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<td></td>
<td>(g) Communication</td>
<td>(h) Global awareness</td>
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<td></td>
<td>(i) Life-long learning</td>
<td>(j) Contemporary issues</td>
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<td>(k) Modern tools</td>
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### Computer Tools:

1. Quartus II programming tool from Altera, Modelsim simulator from Mentor Graphics
2. Altera Cyclone IV FPGA (DE2-115 Development Board)

### Laboratory Content:

See CPEN 430L

### Design Content:

Design issues are addressed.

### Relation to Curriculum:

<table>
<thead>
<tr>
<th>Curricular Component</th>
<th>Elect. Power/Power Syst.</th>
<th>Computer</th>
</tr>
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<tbody>
<tr>
<td>Math/Science</td>
<td>EM/Circuits/Elect./Filters</td>
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<td>Design</td>
<td>Comm. Syst./Signal Proc.</td>
<td>Other Engineering</td>
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<td>Foundational</td>
<td>Intermediate</td>
<td>Advanced</td>
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CATALOG DESCRIPTION:

Three hours lab per week. Concurrent with CPEN 430.

PREREQUISITES

1. Introduction to Digital Logic
2. C or Python programming

TEXTBOOK(S) / REQUIRE MAT’L:

Circuit Design and Simulation with VHDL by V. Pedroni, 2/e, MIT Press, 2010

COURSE TOPICS:

1. Programming FPGAs with Quartus
2. “Keypad” Decoder
3. State Machine Implementation
4. LCD Display Driver
5. Storage and Display of “Keypad” Entries
6. Top down Design with Quartus
7. Dice Game Project

COURSE OBJECTIVES:

1. To teach the student understanding of synchronous digital logic design techniques
2. To teach the student tools for programming logic on complex programmable logic devices
3. To teach the student practical knowledge required to design, implement and test digital systems
**Professional Components/Course Outcomes:**

*By the end of this course the student will be able to:*

1. Decompose a digital system into datapath and control modules
2. Use VHDL to implement logic modules
3. Program, integrate and test a digital system on a FPGA chip
4. Document the design in a formal report

**Class/Lab Schedule:**

3 laboratory hours per week, one session
1 credit hour

**Relation to Program Outcomes:**

- (a) Fundamental math, science, or engineering
- (b) Experimentation
- (c) Design
- (d) Teamwork
- (e) Problem solving
- (f) Professional ethics
- (g) Communication
- (h) Global awareness
- (i) Life-long learning
- (j) Contemporary issues
- (k) Modern tools

**Computer Tools:**

1. Quartus II programming tool from Altera, and Modelsim simulator from Mentor Graphics
2. Altera Cyclone IV FPGA (DE2-115 Development Board)

**Laboratory Content:**

See Course Topics

**Design Content:**

Design issues are addressed.

**Relation to Curriculum:**

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