CPEN 230L: Introduction to Digital Logic Lab

Section 2 - Fall 2017 - Claudio Talarico

For the first 4 labs, we will be meeting in Herak 214, then from Lab 5 onwards we will be meeting in Herak 100.

Lab. Schedule:

Lab #	Room	Topic
01	HK 214	Cedar Software and Logic Trainer
02	HK 214	Basic Gates
03	HK 214	One Gate Type
04	HK 214	Full Adder, Design
05	HK 100	Quartus Prime, FPGA Programming
06	HK 100	Verilog, ModelSim
07	HK 100	MUX, Decoder, 7-Segment Displays
08	HK 100	Numbers and Displays
09	HK 100	Latches, Flip-Flops, Counters
10	HK 100	Switch Debouncing, Counters
11	HK 100	State Machines
12a	HK 100	Final Project #1
12b	HK 100	Final Project #2

Main Software Tools:

Cedar	Logic Simulator software (free, Windows only)
Quartus Prime	Design software for Programmable Logic Devices (by Altera), It supports both schematic design entry and Hardware Design Language (HDL) design entry and synthesis.
ModelSim	Hardware Description Language compiler, simulator and waveform viewer (Mentor Graphics)

Optional Free Software Tools (you may find useful for labs 5-12):

Icarus Verilog	Verilog compiler and simulator (no FPGA programming)
GTKWave	Waveform viewer

Summary:

Labs 1-4:	Manual Methods (breadboarding, 7400 series chips, troubleshooting, K-maps)
Lab 5:	Quartus (schematic input, and mapping into a Field Programmable Gate Array)
Lab 6:	ModelSim (Verilog input, and simulation)
Labs 7-10:	Design Entry, Simulation and Synthesis of combinational and sequential circuits using Verilog
Lab 12:	Design, Simulate, Troubleshoot, Synthesize, and Document a project using Verilog