Quartus II Design Flow: Basic Steps Summary

1. Required Files

```
$ pwd
/Users/talarico/VTut
$ ls -1
light.csv
light.v
light_tb.v
```

```
# File: light.csv (comma separated values)
# Pin Assignments

To, Direction, Location
x1, input, PIN_AB28
x2, input, PIN_AC28
f, output, PIN_E21
```

```
/*
   File: light.v
   Simple Tutorial to demonstrate the Verilog based design flow
   with Altera/Modelsim.
   The code implements a 2-input exor gate
*/

module light(x1,x2,f);
input x1,x2;
output f;

assign f = (x1 & ~x2) | (~x1 & x2);

endmodule
```

```
// File: light_tb.v
// Test Bench for the light module
// author: Claudio Talarico

`timescale 1ns / 1ns

module light_tb;

// inputs to device under test (DUT – i.e. RTL Hardware)
reg ain;
reg bin;
//outputs from DUT
wire cout;

// instantiate the DUT
light dut(
.x1( ain ),
.x2( bin ),
.f( cout )
);

// output the simulation in graphical format
initial
begin
  $dumpfile("light.vcd");
  $dumpvars(0, dut);
end

//initialize inputs to DUT
initial
begin
  ain = 0;
  bin = 0;
end

// generate ain values (ain test vectors)
always
begin
# 20 ain = ~ain;
end

// generate bin values (bin test vectors)
always
begin
# 40 bin = ~bin;
end

// output the simulation in textual format
initial
begin
  $monitor("At time %t, X1 is = %b, X2 is %b, F is %b",
           $time, ain, bin, cout);
end
```

```
// stop the simulation from running forever
initial
begin
  # 200 $stop;
end
endmodule
```

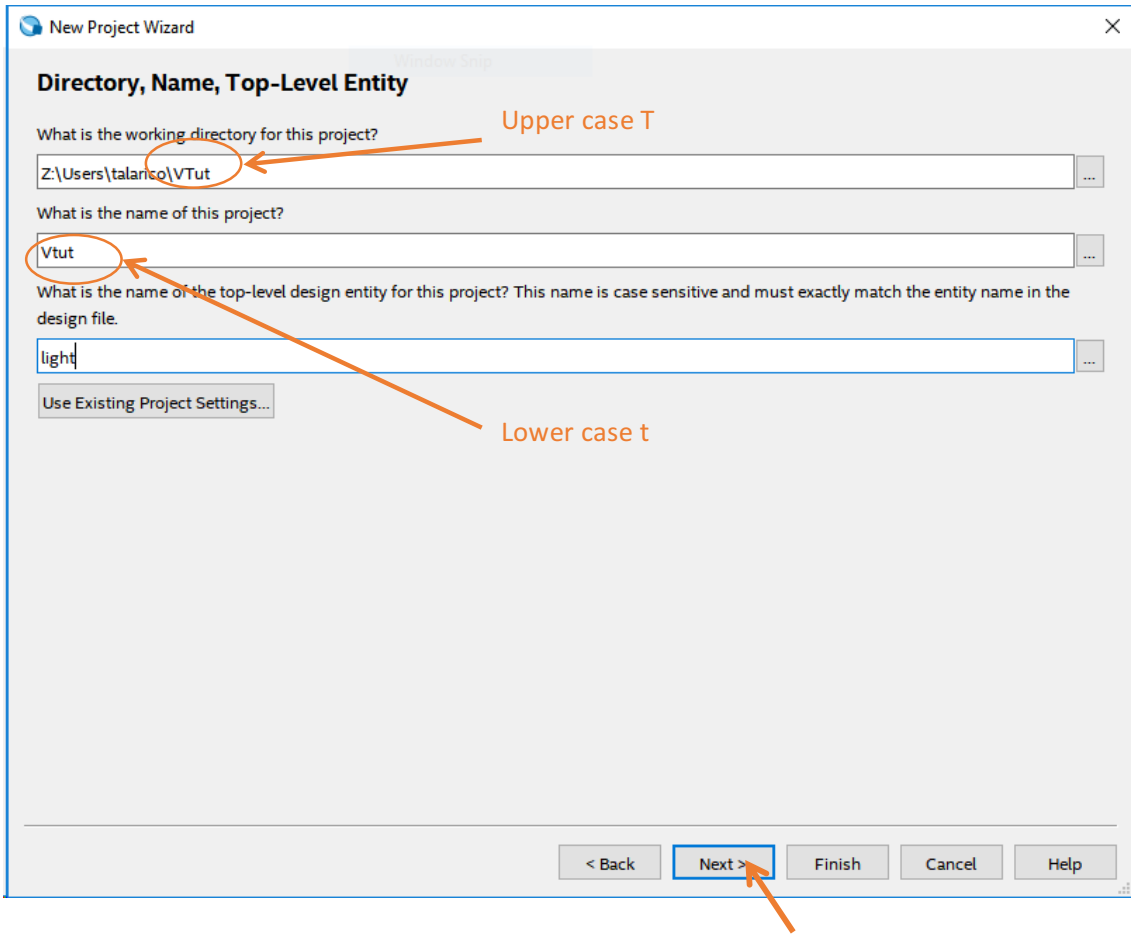
2. Create Project

A project consists of:

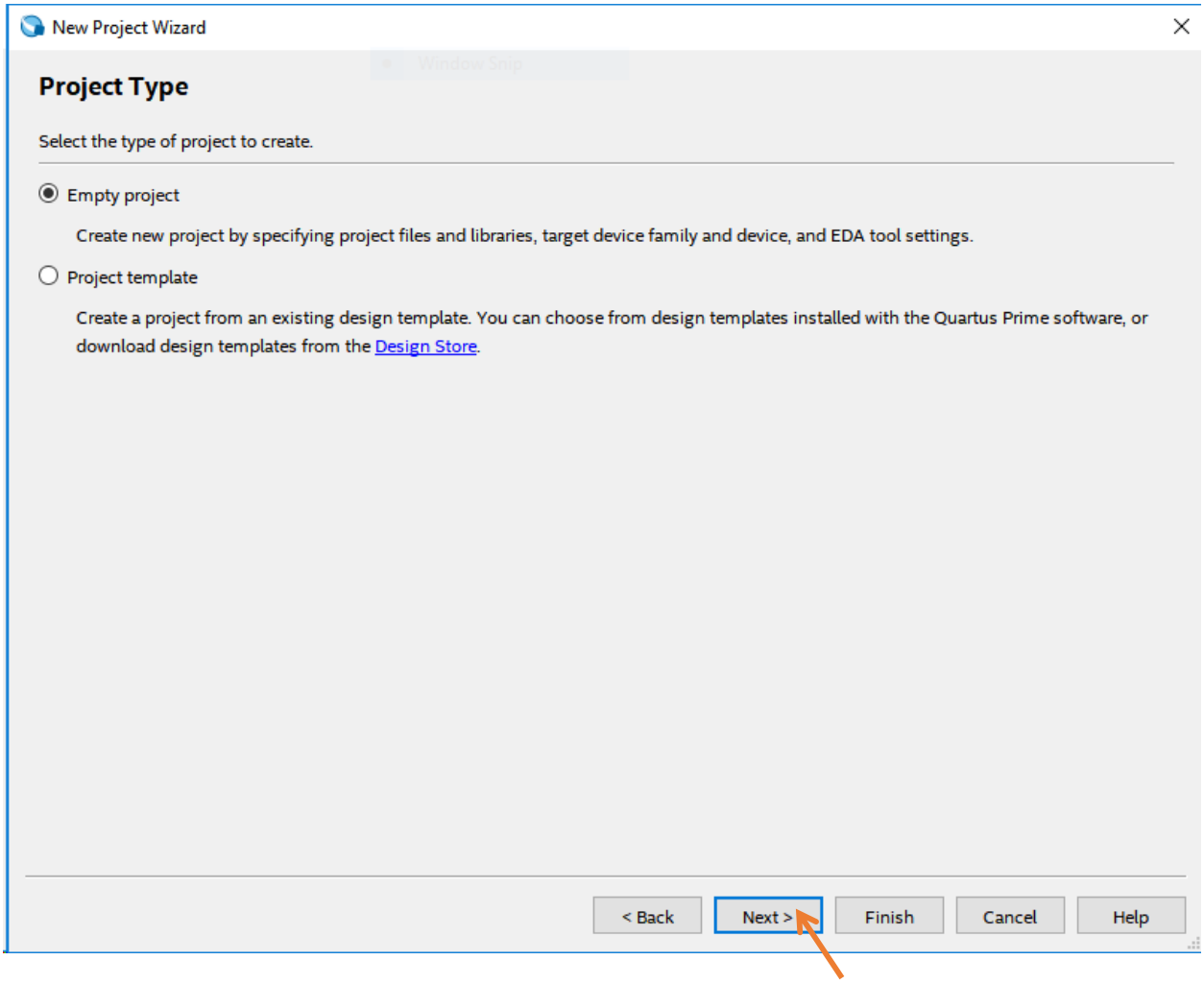
* Project Name and Directory
* Name of the top-level design **module**
* Project Files and Libraries
* Target Device Family and Device
* EDA Tool Setting

File > New Project Wizard

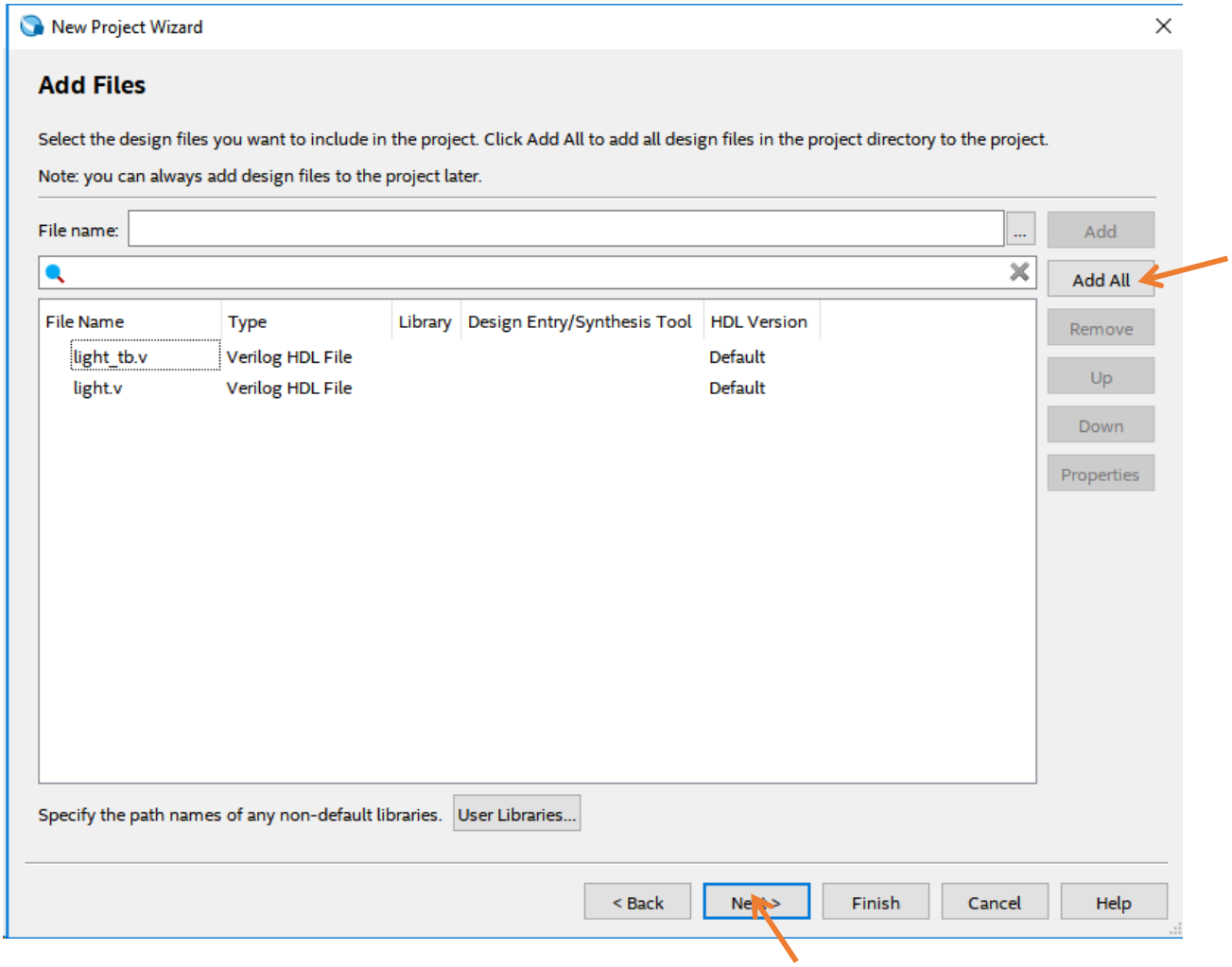
Step 1.



Step 2.


New Project Wizard
Project Type
Select the type of project to create.
Empty project
Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.
Project template
Create a project from an existing design template. You can choose from design templates installed with the Quartus Prime software, or download design templates from the Design Store.
< Back
Next >
Finish
Cancel
Help

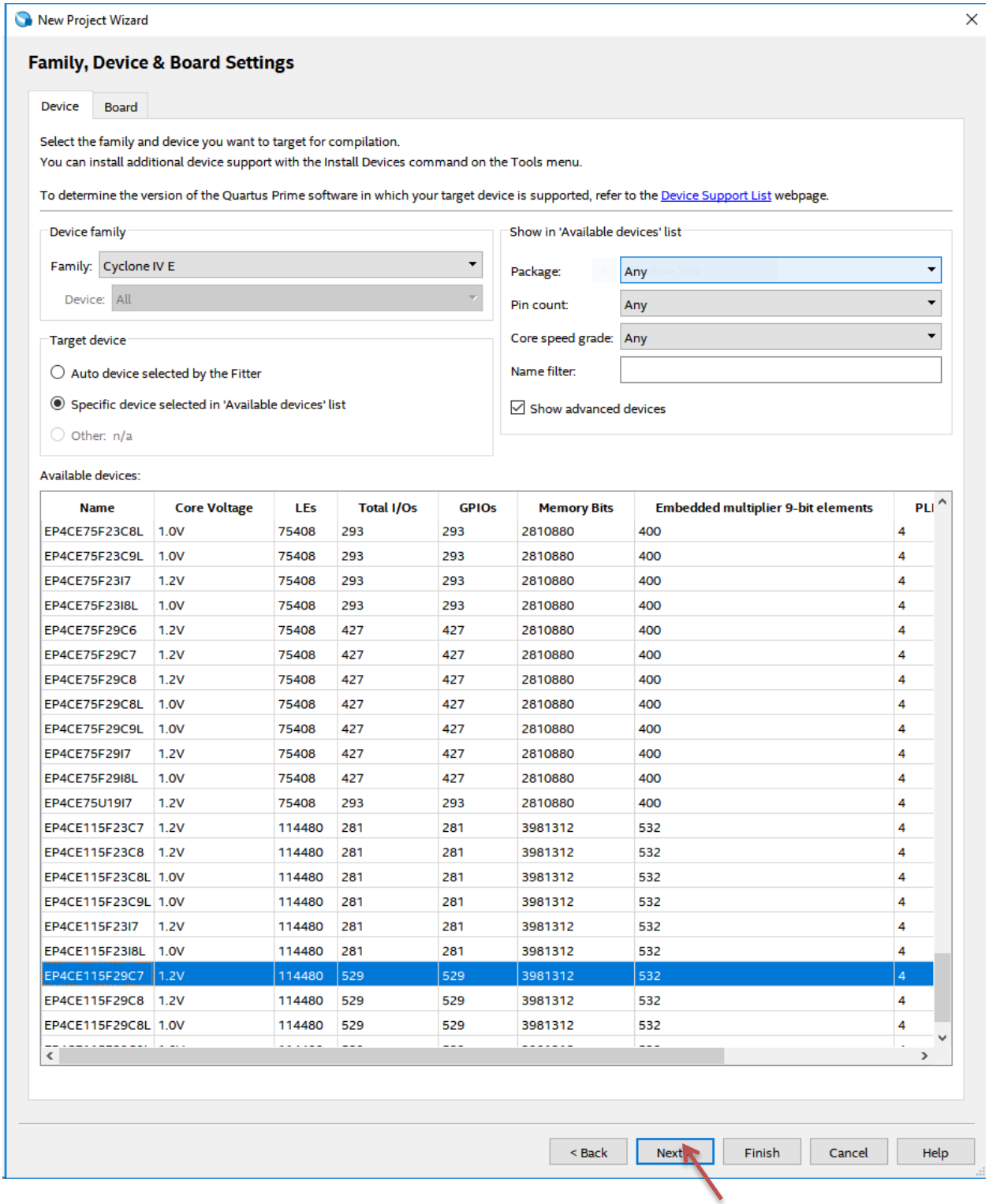
Step 3.



To modify a project use:
Project > Add/Remove Files in Project

To edit a new Verilog File with Quartus Text Editor use:
File > New > (Design Files > Verilog File)

Step 4.

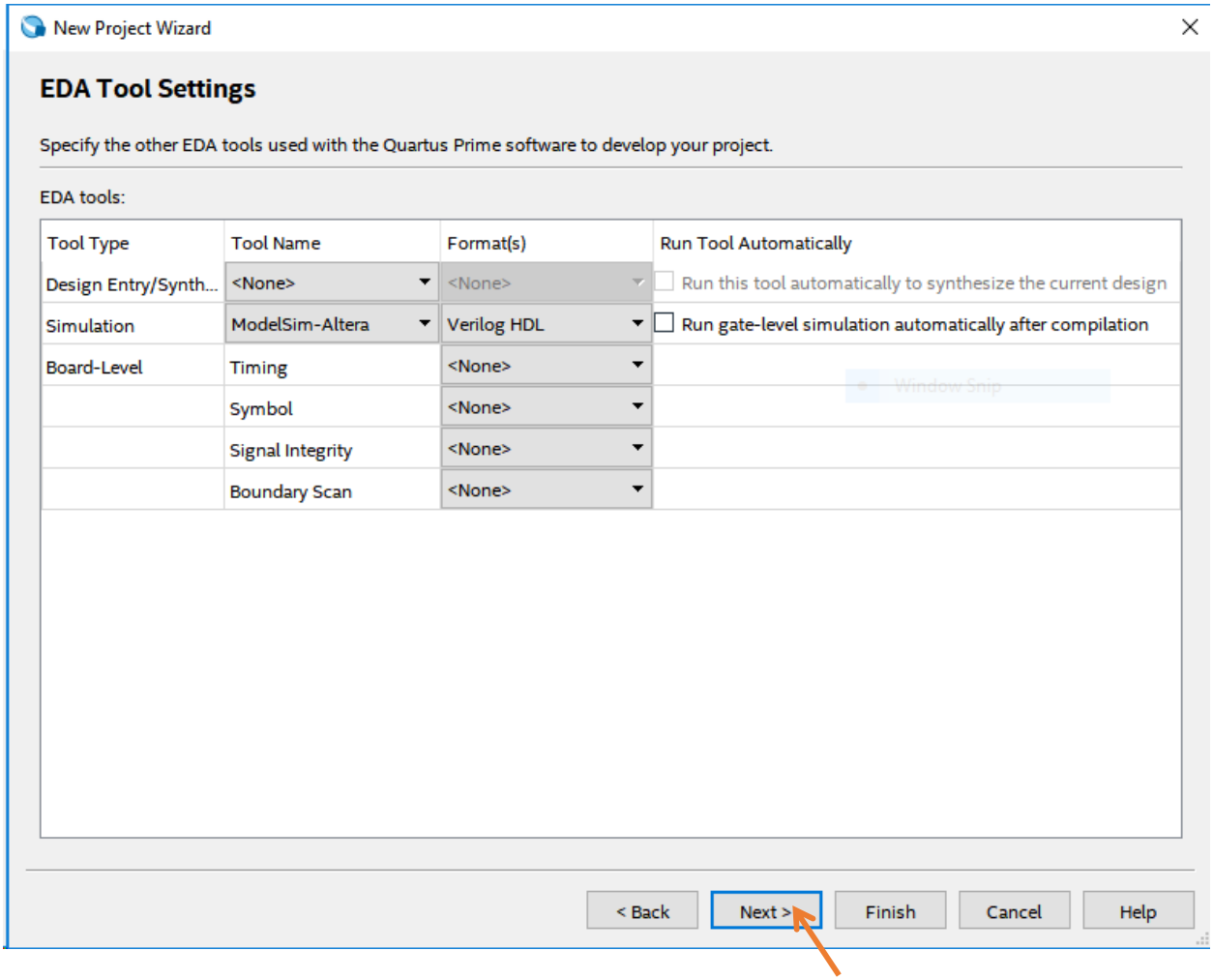


Family: Cyclone IV E

Device: EP4CE115F29C7

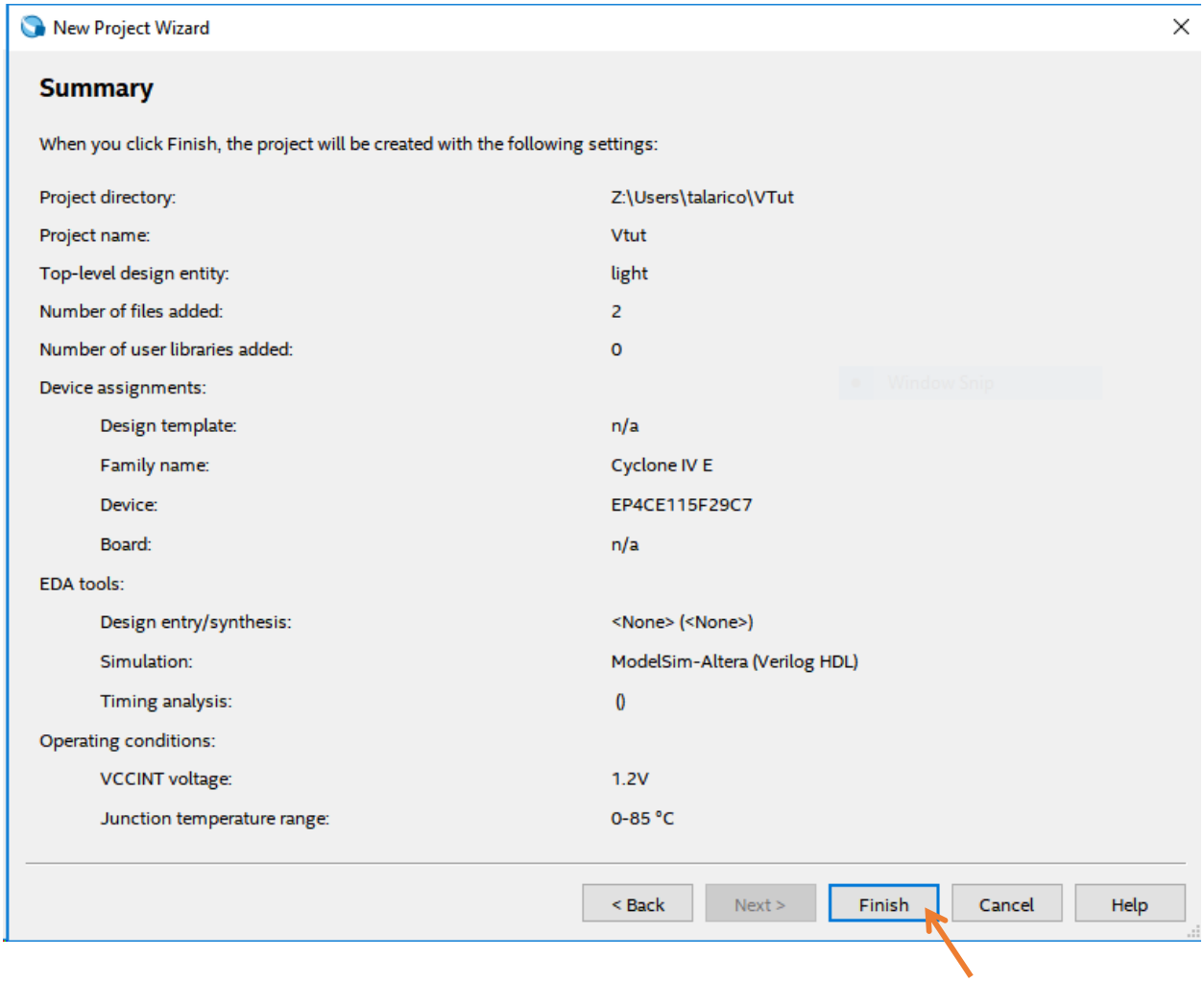
To modify the FPGA family or the specific device use:
Assignments > Device

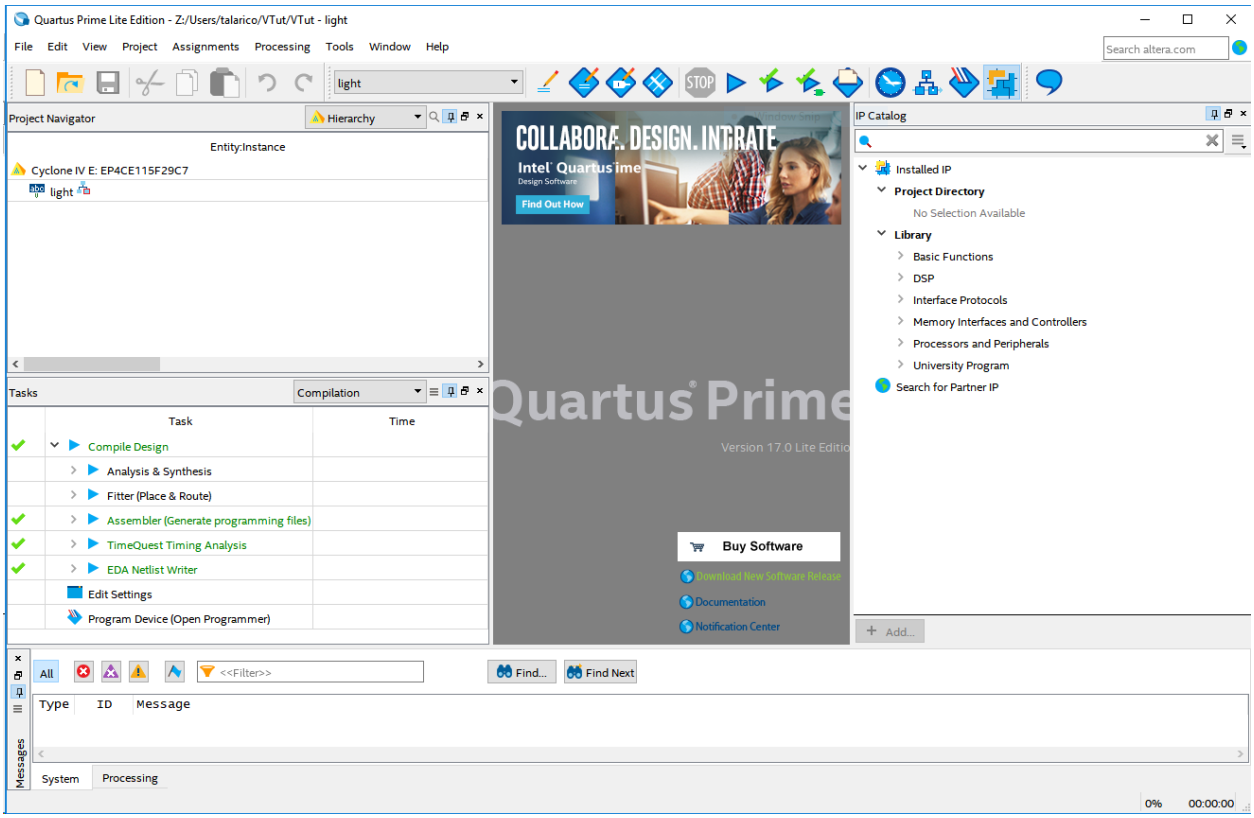
Step 5.



To modify the EDA Setting use:
Assignments > Settings

Step 6.


New Project Wizard
Summary
When you click Finish, the project will be created with the following settings:
Project directory: Z:\Users\talarico\VTut
Project name: Vtut
Top-level design entity: light
Number of files added: 2
Number of user libraries added: 0
Device assignments:
Design template: n/a
Family name: Cyclone IV E
Device: EP4CE115F29C7
Board: n/a
EDA tools:
Design entry/synthesis: <None> (<None>)
Simulation: ModelSim-Altera (Verilog HDL)
Timing analysis: ()
Operating conditions:
VCCINT voltage: 1.2V
Junction temperature range: 0-85 °C
< Back
Next >
Finish
Cancel
Help



3. Files and Directories up to this point

```
$ ls -1p
VTut.qpf
db/
incremental_db/
light.cvs
light.qsf
light.v
light_nativelink_simulation.rpt
light_tb.v
output_files/
simulation/
```

Quartus project file

```
$ cat VTut.qpf
QUARTUS_VERSION = "17.0"
DATE = "14:01:19  August 15, 2017"
# Revisions
PROJECT_REVISION = "light"
```

Quartus settings file

```
$ cat light.qsf
set_global_assignment -name FAMILY "Cyclone IV E"
set_global_assignment -name DEVICE EP4CE115F29C7
set_global_assignment -name TOP_LEVEL_ENTITY light
set_global_assignment -name ORIGINAL_QUARTUS_VERSION 17.0.2
set_global_assignment -name PROJECT_CREATION_TIME_DATE "14:01:19  AUGUST 15, 2017"
set_global_assignment -name LAST_QUARTUS_VERSION "17.0.2 Lite Edition"
```

```
set_global_assignment -name VERILOG_FILE light_tb.v
set_global_assignment -name VERILOG_FILE light.v
set_global_assignment -name PROJECT_OUTPUT_DIRECTORY output_files
set_global_assignment -name MIN_CORE_JUNCTION_TEMP 0
set_global_assignment -name MAX_CORE_JUNCTION_TEMP 85
set_global_assignment -name ERROR_CHECK_FREQUENCY_DIVISOR 1
set_global_assignment -name NOMINAL_CORE_SUPPLY_VOLTAGE 1.2V
set_global_assignment -name EDA_SIMULATION_TOOL "ModelSim-Altera (Verilog)"
set_global_assignment -name EDA_TIME_SCALE "1 ps" -section_id eda_simulation
set_global_assignment -name EDA_OUTPUT_DATA_FORMAT "VERILOG HDL" -section_id eda_simulation
eda_simulation
```

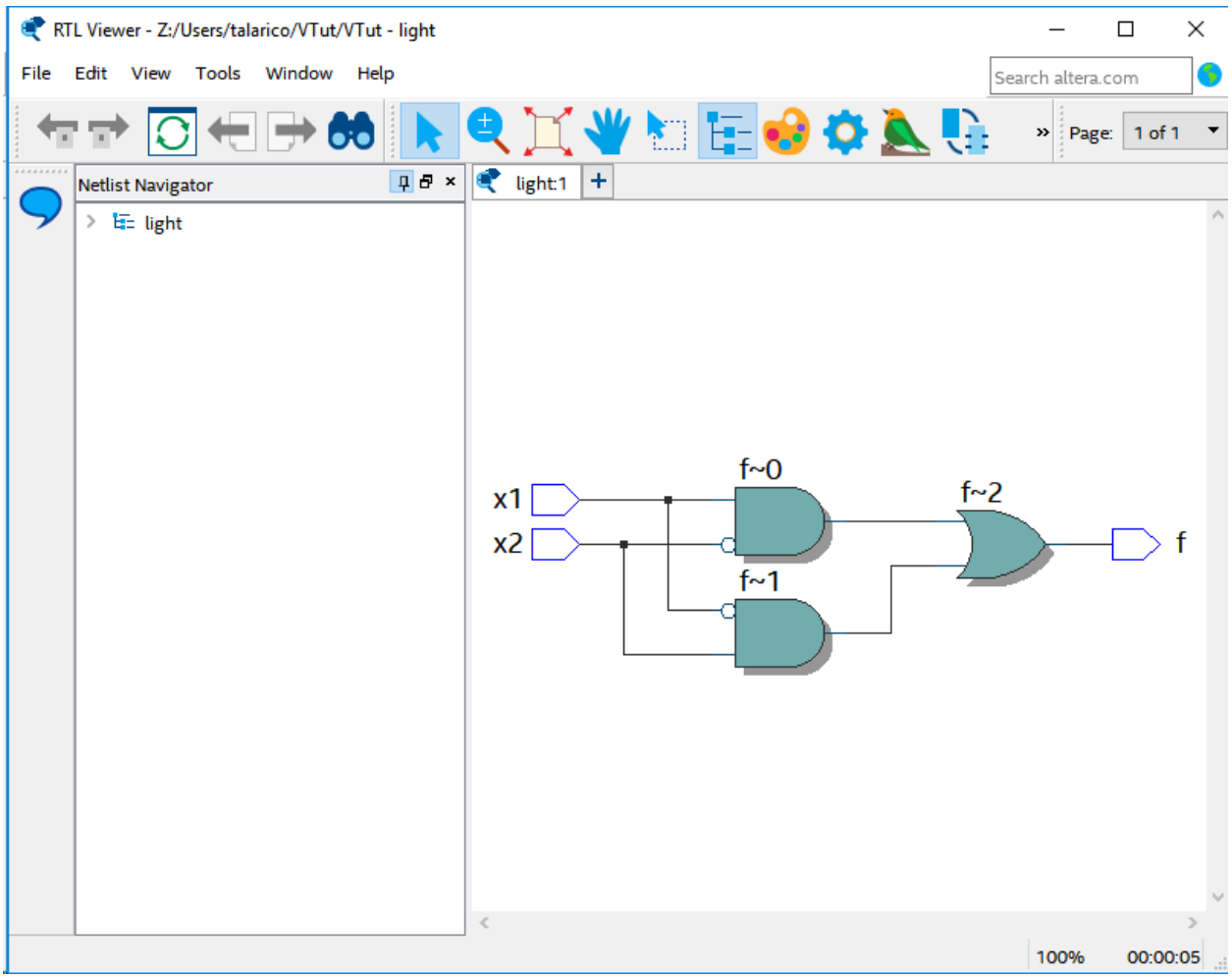
4. Start Compiling the Design

Processing > Analyze Current File > Start > Analysis & Elaboration

Check syntax & translate HDL into generic Boolean equations

Make sure to verify all Info/Warnings/Errors

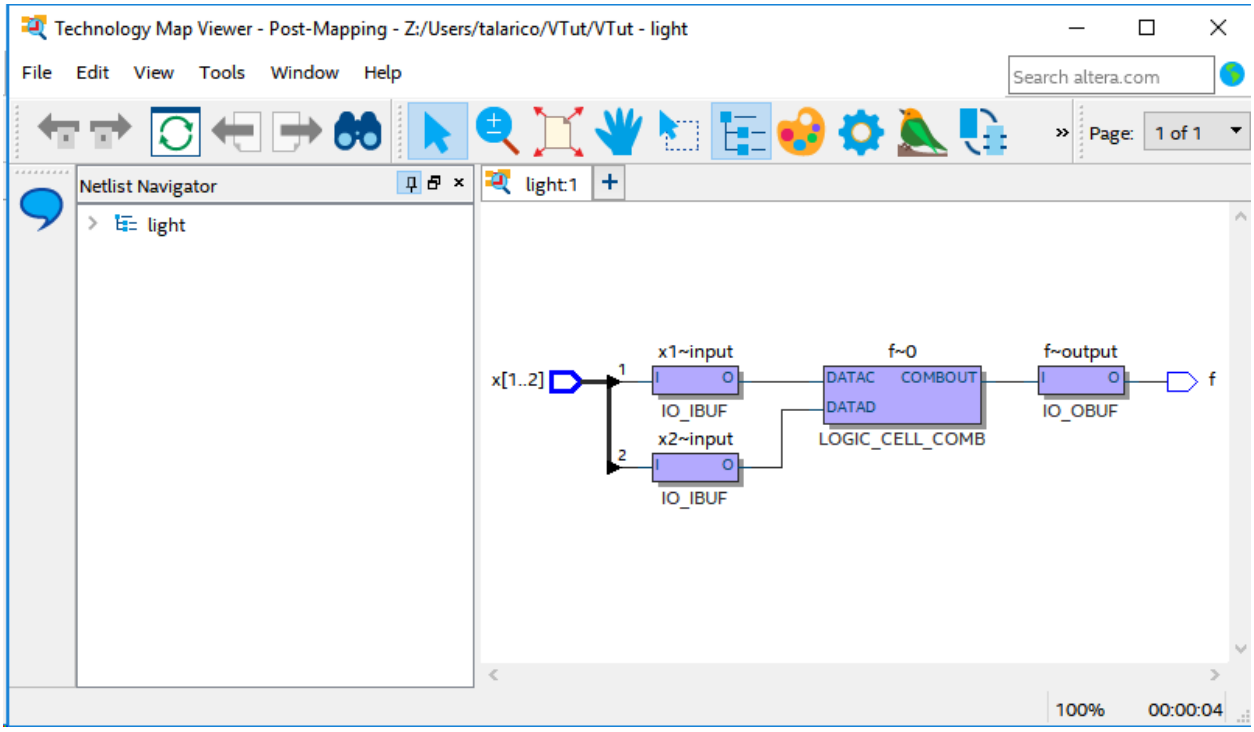
Tools > Netlist Viewers > RTL viewer



Processing > Analyze Current File > Start > Analysis & Synthesis

Synthesize HDL into target Technology

Tools > Netlist Viewers > Technology Map Viewer (Post Mapping)



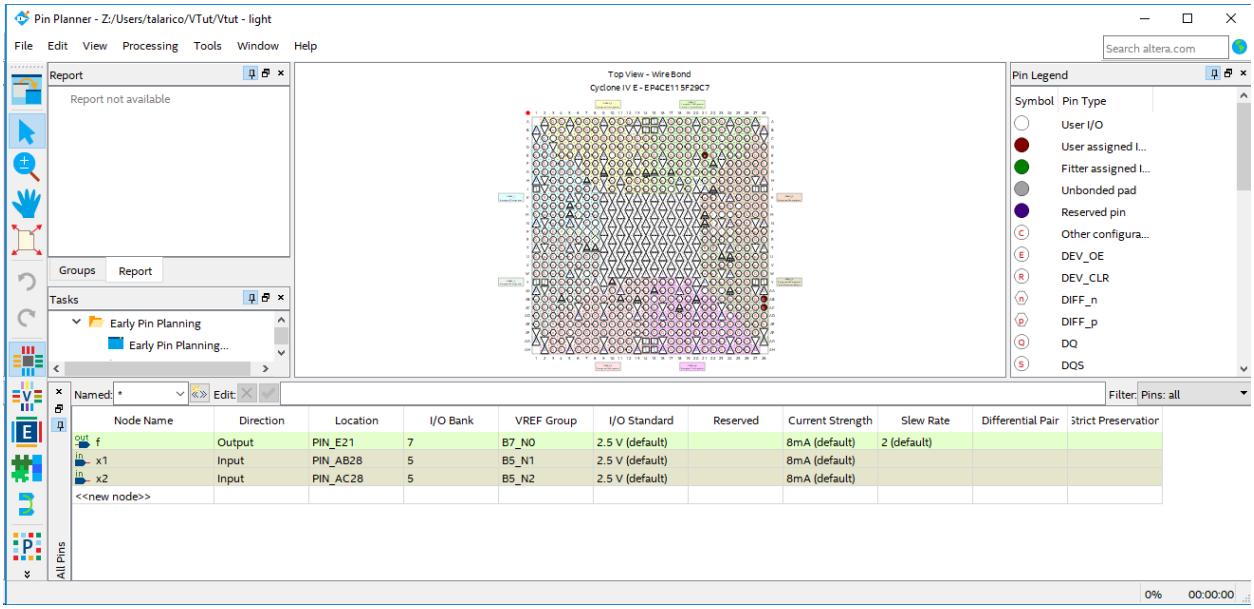
4. Pin Assignments

More often than not, the Pin Planner has issues loading automatically the pinout assignments saved in light.csv. Put the assignments in a text file light.txt and load it manually using:

Assignments > Import Assignments (file name light.txt)

```
$ cat light.txt
# Pin Assignments

To, Direction, Location
x1, input, PIN_AB28
x2, input, PIN_AC28
f, output, PIN_E21
```



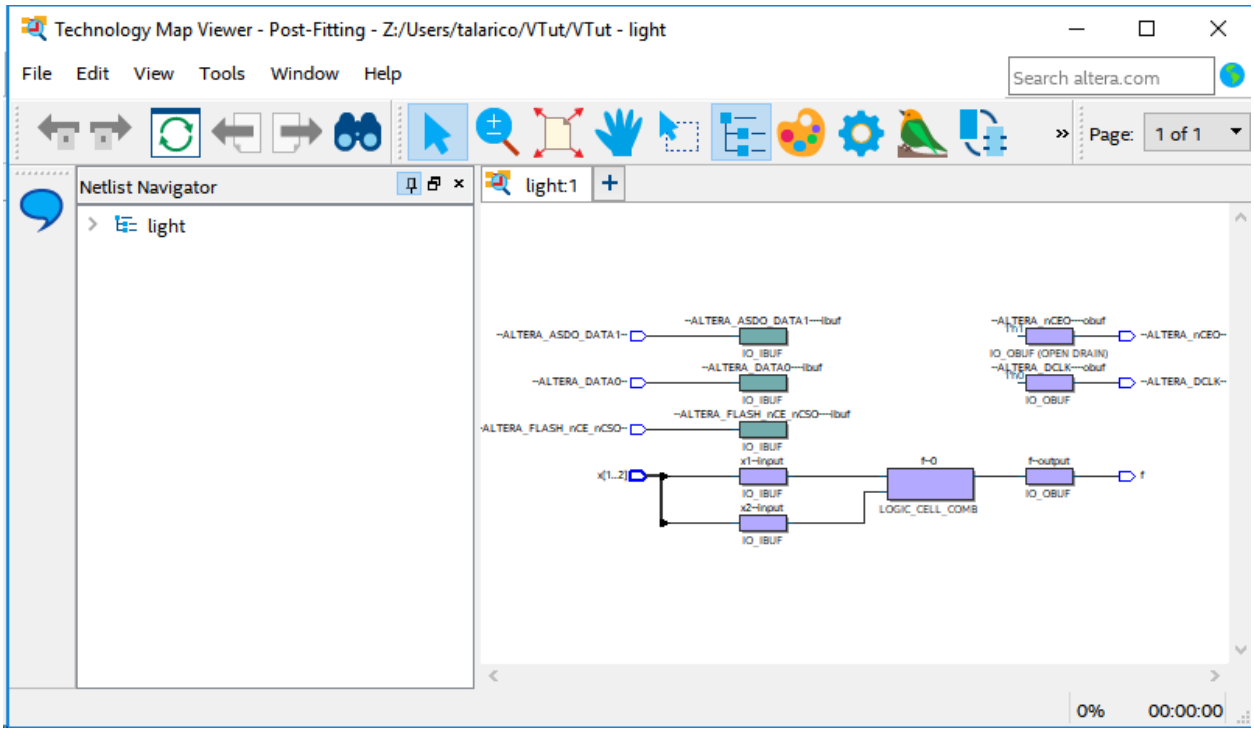
On the DE2-115 board, the input PIN_AB28 is physically mapped with the switch SW[0]
On the DE2-115 board, the input PIN_AC28 is physically mapped with the switch SW[1]
On the DE2-115 board, the output PIN_E21 in mapped with the green light emitting diode LEDG[0]

6. Continue Compiling the Design

Processing > Start > Start Fitter

Place & Route

Tools > Netlist Viewers > Technology Map Viewer (Post Fitting)



7. Simulation

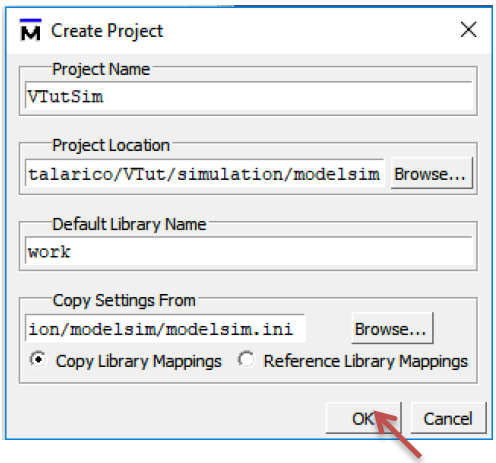
Step 1.

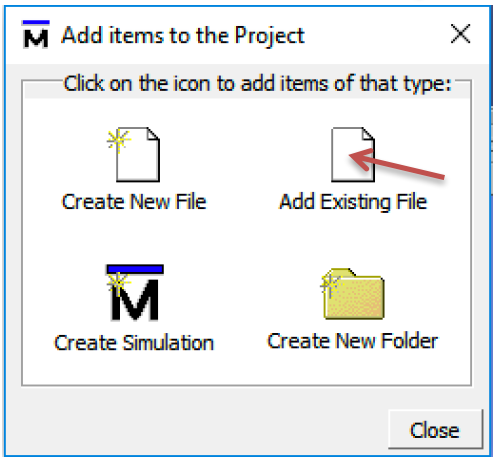
Start Modelsim. The path to the executable should be located to something similar to:
C:/intelFPGA_lite/17.0/modelsim_ase/win32aloem/

For convenience create a shortcut to it:

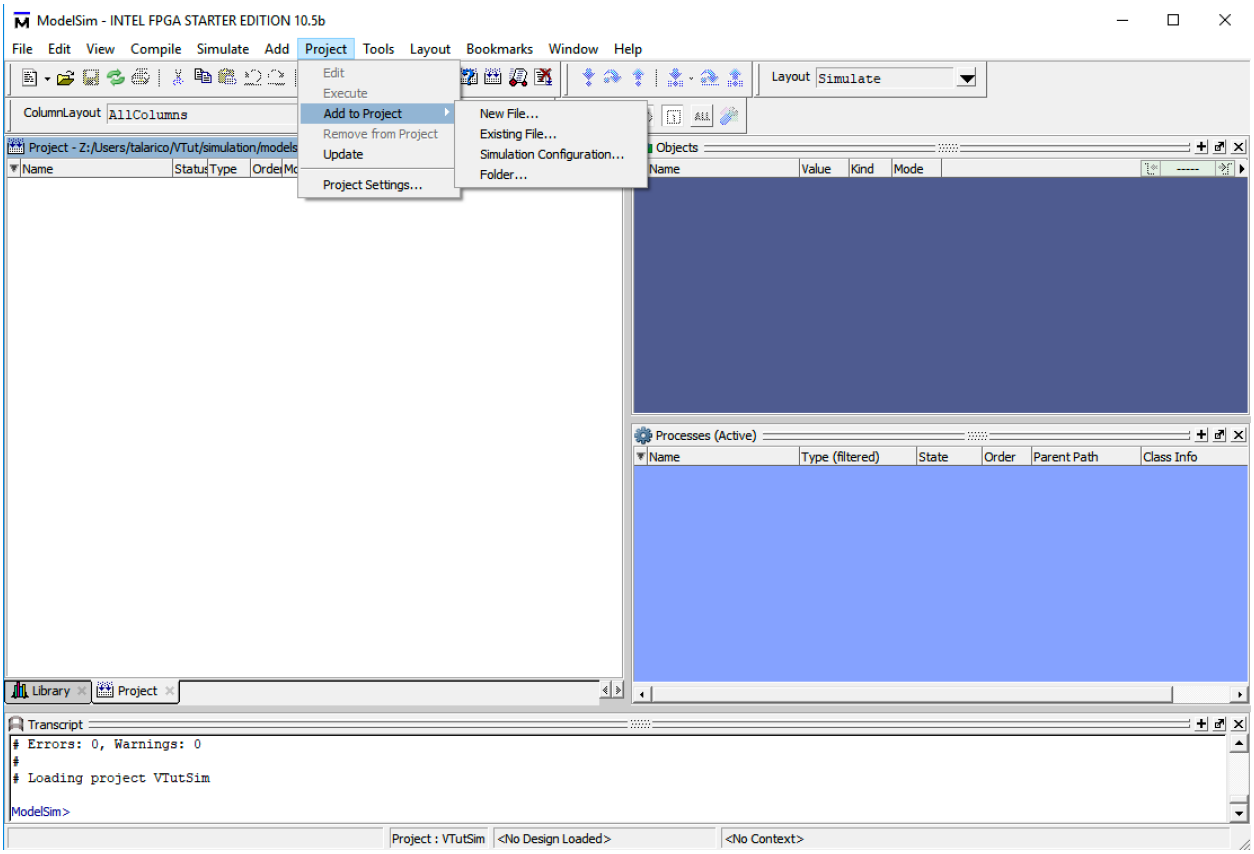
Step 2.

File > New > Project
Project name: VTutSim
Project Location: Z:/Users/talarico/ VTut/simulation/modelsim





Alternatively,
1) ignore the popup window (i.e., hit close),
2) switch from the Library Tab to the Project Tab and
3) select:
Project > Add to project > Existing File:
Z/Users/talarico/VTut/light.vhd
Z:/Users/talarico/VTut/light_tb.vhd



If the files are not ready and you need to create them from scratch use:
Project > Add to project > New File.

Step 3.

Compile > compile all

Step 4.

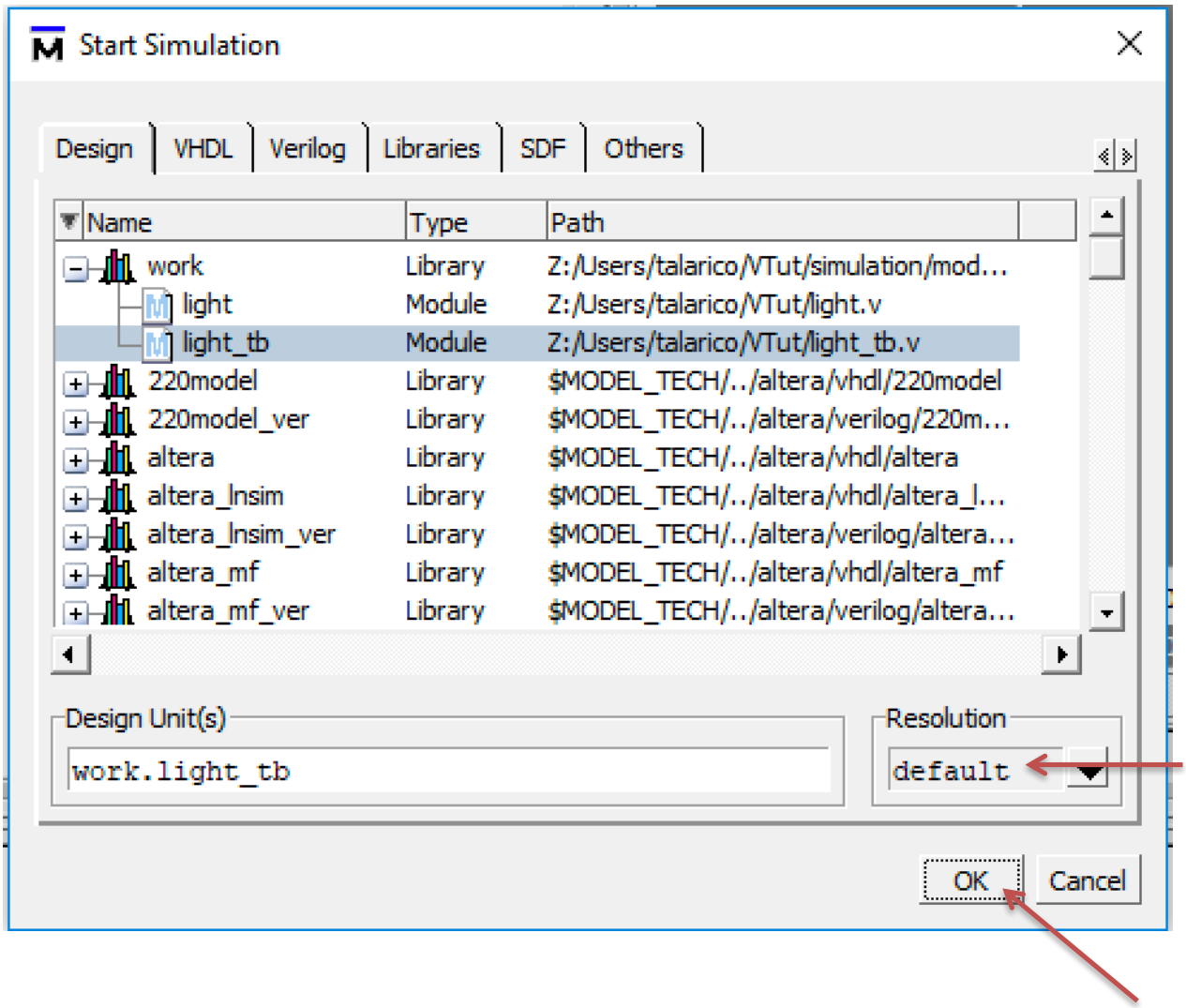
In case you do not see the two compiled files under the work library, remove the work library. The work library will be regenerated with the correct info!

Simulate > Start Simulation

+ work

  + light

  + light_tb



vsim > view wave

vsim > add wave sim: /light_tb/*

vsim > run –all

The simulation runs forever!!!

To stop the simulation, you can use:

Simulate > break

A better approach is to automatically stop the simulation by using a $stop statement in the testbench code.

A few other useful commands to remember are:

vsim > restart –force
vsim > run –all
vsim > wave zoomout
vsim > wave zoomfull

8. Finish Compiling the Design

Processing > Start > Assembler  Generating Programming files (light.sof and light.jdi)

sof = SRAM object file
jdi = JTAG Debugging Information

9. View Reports

Make sure to read carefully the reports generated at each step of the design process.
The reports can be accessed through the Quartus' workspace window or directly in the output_files folder.

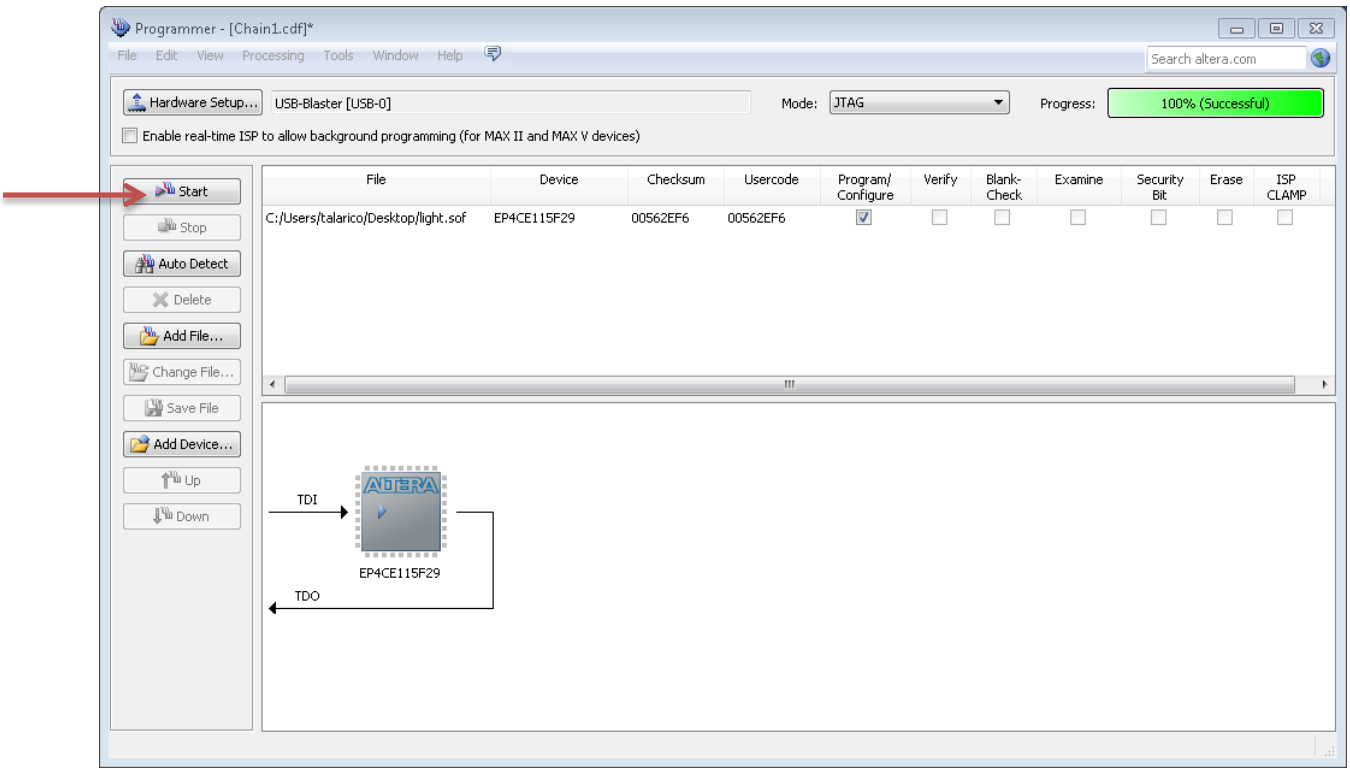
10. Programming and Configuring the FPGA

Before Programming the FPGA make sure to set the board in RUN mode (JTAG mode).

Tools > Programmer

Edit > Add File (Z:/Users/talarico/VTut/output_files/light.sof)

The hardware Setup must be USB-Blaster [USB-0]



11. Testing the Circuit on the Development Board