Introduction and Motivation

- D&H:
  §1.0, §1.1, §1.5, §1.6
  §2.2, §2.3, §2.4
  §4.0, §.4.3.1, §4.3.2

Boolean Algebra

- D&H:
  §3.0, §3.1, §3.2, §3.3, §3.5

Standard Forms

- D&H:
  §3.4, §6.0, §6.1, §6.3

K-maps and Minimization

- D&H:
  §6.3, §6.4, §6.5, §6.6, §6.7
  §6.8, §6.9, §6.10, §4.3.4
- For getting started on Verilog: D&H Ch.7

Binary Representations and Arithmetic

- D&H:
  §10.0, §10.2, §10.3

C.L. Building Blocks and Delays

- D&H:
  §10.2, §8.0, §8.1, §8.2, §8.3
  §8.4, §8.5, §8.6
  §5.0, §5.1, §6.10

S.L. Basic Elements

- D&H:
  §14.0, §14.1, §15.0, §15.1, §15.2

S.L. Building Blocks

- D&H:
  §16.0, §16.1, §16.2

Finite State Machines

- D&H:
  §14.2, §14.3, §14.4, §14.5, §14.6

Timing of Synchronous S.L. Circuits

- D&H:
  §15.0, §15.1, §15.2, §15.3, §15.4