SystemVerilog

CPEN 230 – Introduction to Digital Logic

The divide by 3 FSM in System Verilog

```
// divby3.sv
// divide by 3 counter
module divby3
(
  input logic clk,
  input logic rst,
  output logic y
);

  typedef enum logic [1:0] {S0, S1, S2} statetype;
  statetype state, nextstate;

  // state register
  always @(posedge clk, posedge rst)
    if (rst) state <= S0;
    else state <= nextstate;

  // next state logic
  always @(state)
    case (state)
      S0: nextstate = S1;
      S1: nextstate = S2;
      S2: nextstate = S0;
      default: nextstate = S0;
    endcase

  // output logic
  assign y = (state == S0);

endmodule
```

```
// tb_divby3.sv
// testbench for divvby3.sv

‘timescale 1ns/1ns

module tb_divby3();
  logic clk, rst, y;

  // instantiate the dut
  divby3 dut(clk,rst,y);

  parameter T = 50;

  // dump vcd
  initial begin
    $dumpfile("divby3.vcd");
    $dumpvars(0, tb_divby3);
  end

  // generate clock
  always begin
    clk = 1;
    #(T/2);
    clk = 0;
    #(T/2);
  end

  // at start up generate short async rst
  initial begin
    rst = 0;
    #2;
    rst = 1;
    #2;
    rst = 0;
  end

  // let the simulation run for 10 cycles
  initial begin
    #(T*10);
    $finish;
  end

endmodule
```

Testbench

```
README
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1. iverilog compiles system verilog! Just use the option -g2012 as follows:
   $ iverilog -g2012 divby3.sv tb_divby3.sv

2. NOTE: Modelsim is capable of generating vcd files but cannot open them.
   The format used by modelsim is called wlf. To convert a vcd file into a
   wlf file use the following modelsim command:
   $ vcd2wlf <inputfile>.vcd <outputfile>.wlf
   It is possible to open a wlf file either from within Modelsim browsing to
   File > Open
   or directly using the command:
   $ vsim -gui <filename>.wlf

3. Unfortunately the vcd created using iverilog does not preserve the
   enumerated types (it coverts them). The vcd created using
   modelsim does preserve the enumerated types.

4. GTKwave does not diplays the enumerated types (it converts them)
```
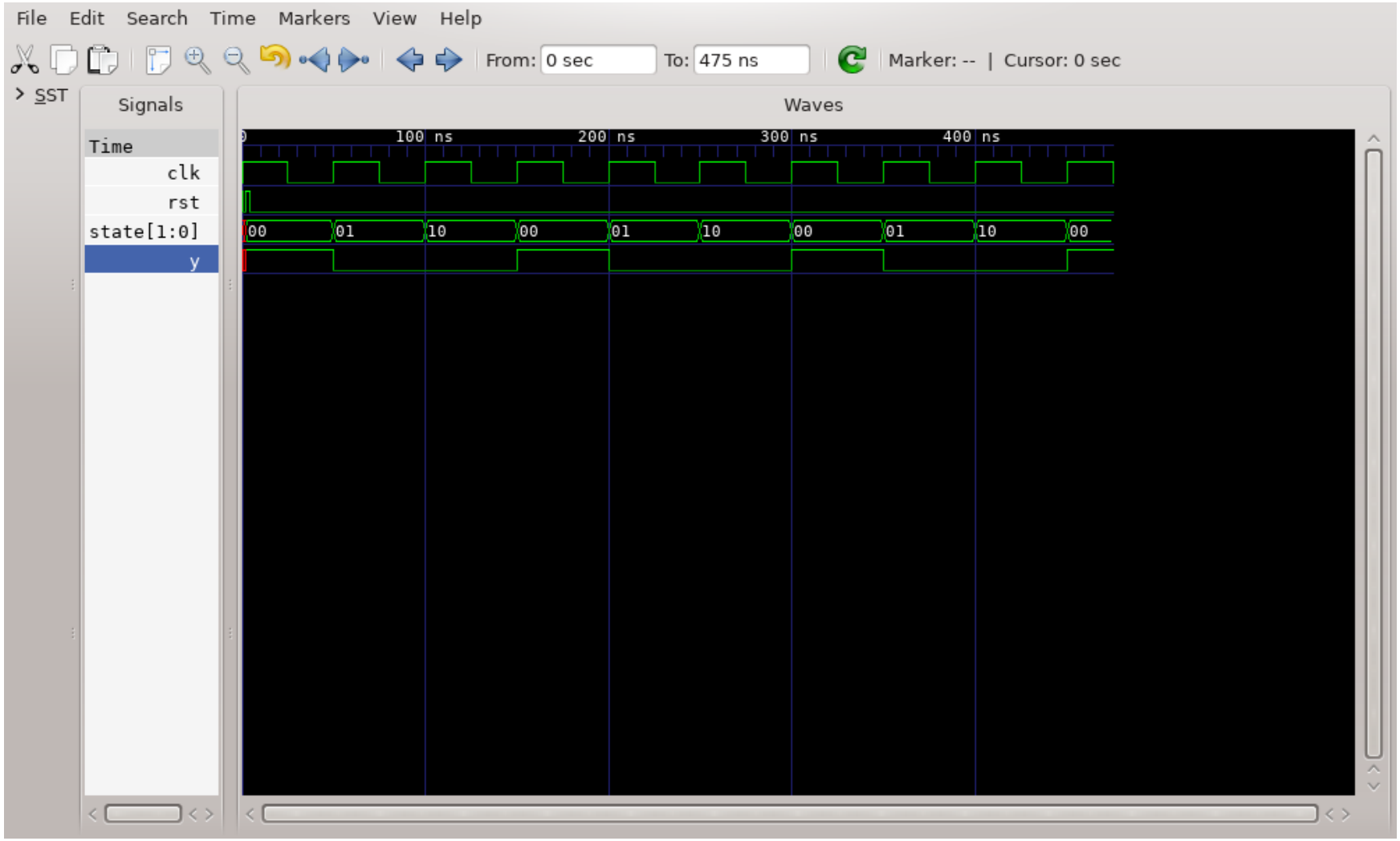
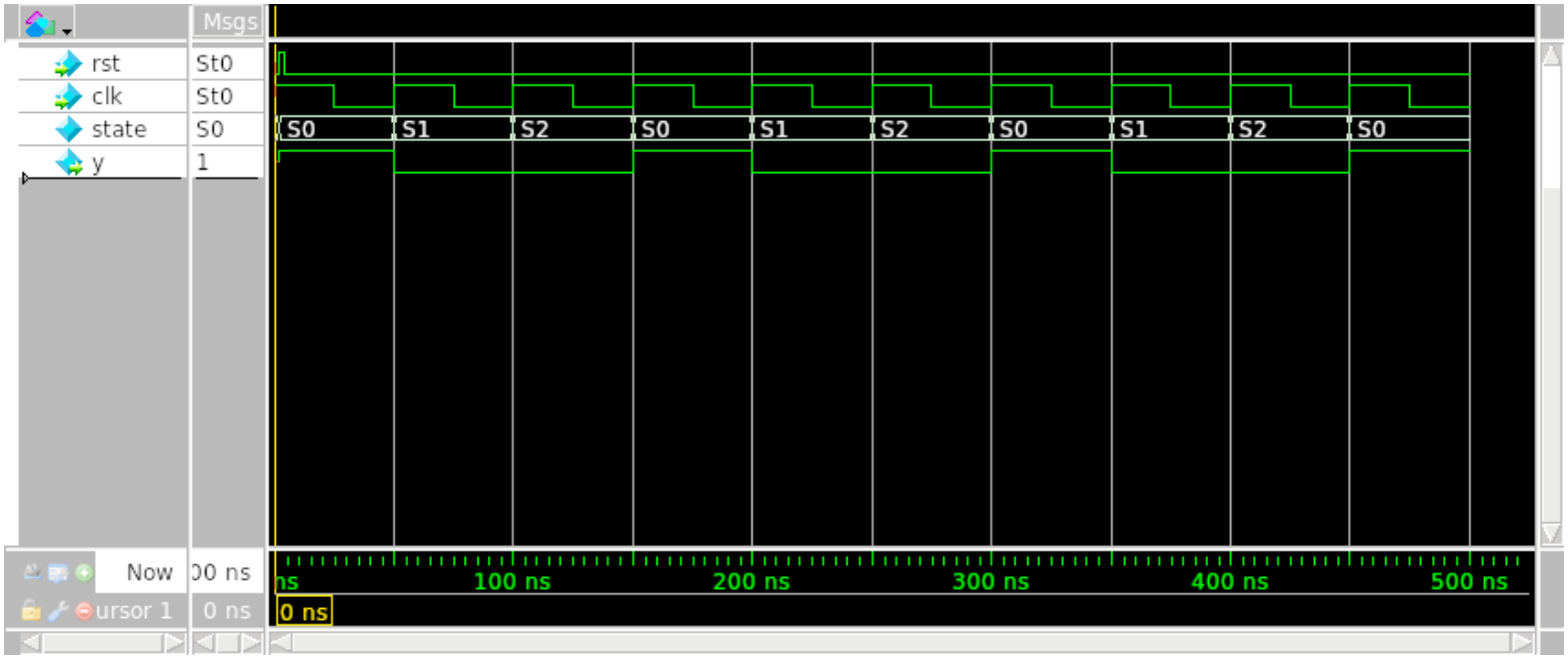

GTKwave Simulation



Modelsim Simulation



rundivby3.scr

```
#!/bin/bash
vlib work
vlog -work work "./divby3.sv"
vlog -work work "./tb_divby3.sv"
vsim -gui work.tb_divby3 -do simdivby3.do
```

simdivby3.do

```
restart -f
add wave sim:/tb_divby3/dut/rst \
         sim:/tb_divby3/dut/clk \
         sim:/tb_divby3/dut/state \
         sim:/tb_divby3/dut/y
run -all
```