CPEN 230L: Introduction to Digital Logic Lab

Section 1 - Spring 2018 - Claudio Talarico

Course Description
Number systems and codes, Boolean Algebra, Logic gates and flip-flops. Verilog HDL. Combinational and sequential Logic Design using FPGAs.

Lab. Schedule:
W 1:10 PM - 3:50 PM, HRK 214 and HRK 100

The first lab. (T0) we will meet in Herak 100, the 4 following labs (01-04) we will meet in Herak 214, then from lab. T1 onwards we will meet in Herak 100.

Lab #	Room	Topic
T0	HK 100	Installing and getting familiar with the free tools
01	HK 214	Logic Trainer
02	HK 214	Basic Gates
03	HK 214	One Gate Type
04	HK 214	Full Adder, Design
T1	HK 100	Quartus Prime and Modelsim Tutorial
05	HK 100	Quartus Prime schematic entry and FPGA Programming
06	HK 100	Quartus Prime Verilog entry and FPGA programming, and ModelSim Verilog Simulation
07	HK 100	MUX, Decoder, 7-Segment Displays
08	HK 100	Numbers and Displays
09	HK 100	Latches, Flip-Flops, Counters
10	HK 100	Switch Debouncing, Counters
11	HK 100	State Machines
12a	HK 100	Final Project #1
12b	HK 100	Final Project #2

In-Lab Software Tools:

Quartus Prime	Design software for Programmable Logic Devices (by Intel/Altera), It supports both schematic design entry and Hardware Design Language (HDL) design entry and synthesis. The HDL we will use in this class is called Verilog.
ModelSim	Hardware Description Language compiler, simulator and waveform viewer (by Mentor Graphics)

Pre-Lab Software Tools (free):

Icarus Verilog	Verilog compiler and simulator (no FPGA programming)
GTKWave	Waveform viewer

Summary:

Lab T0:	Tutorial to learn how to use the free tools required for the pre-labs
Labs 1-4:	Manual Design Methods (breadboarding, 7400 series chips, troubleshooting, K-maps)
Lab T1:	Tutorial to get familiar with the use of Quartus and Modelsim
Lab 5:	Quartus (schematic input, and mapping into a Field Programmable Gate Array)
Lab 6:	Quartus (Verilog design entry) and ModelSim (Verilog simulation)
Labs 7-10:	Design Entry, Simulation and Synthesis of combinational and sequential circuits using Verilog
Lab 12:	Design, Simulate, Troubleshoot, Synthesize, and Document a project using Verilog

Contact Information:
Claudio Talarico
Office: HRK 215
Tel: (509) 313-3561
Fax: (509) 313-5871
email: talarico@gonzaga.edu
www: http://web02.gonzaga.edu/faculty/talarico/CP230/S2018/index.html

Office Hours:
- T, R 11:00 AM - 12:00 PM
- F 1:00 PM - 2:00 PM

Feel free to walk-in anytime or to make an appointment

Lab. Textbook (Recommended)
B. Readler, *Verilog by Example: A concise Introduction for FPGA Design*, Full Arc Press

Grading Policy

Letter	Percentage
A	100-94
A–	93-90
B+	89-86
B	85-82
B–	81-78
C+	77-74
C	73-70
C–	69-66
D+	65-62
D	61-58
F	57-0

Late work will not be accepted.

Classroom Etiquette:

- Arrive in class on time
- Turn off cell phones
- No distracting conversations -- **relevant questions are strongly encouraged**

ADDENDA TO THE SYLLABUS

STATEMENT REGARDING COURSE EXPECTATIONS

As a Jesuit university that seeks to provide an equal opportunity to learn for all students, this course is offered with the expectation that students are here voluntarily, and understand that the university expects all interactions relating to its courses to occur in the context of a professional academic work environment that is welcoming and accessible to all students regardless of gender, race, ethnicity, religion, disability, sexual orientation or identity and any other non-merit factor in educational programs or activities. This environment includes virtual course environments, such as Blackboard, and any course-related communications via e-mail and social media. We strive to create a healthy environment conducive to intellectual honesty and free inquiry; as such, behaviors which constitute harassment, discrimination, or hostile and/or inappropriate conduct will not be tolerated, and faculty, staff and administrators will take action to ensure such matters are addressed promptly and appropriately."

For inquiries or concerns about non-discrimination or the complaint process at Gonzaga, contact the Office of Equity and Inclusion, Business Services Center, 102 E. Boone Avenue or 509.313.5858 or 313-6910. "

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For inquiries or concerns about gender-based harassment, discrimination or sexual misconduct or the complaint process at Gonzaga, contact Stephanie N. Whaley, Title IX Coordinator, Business Services Center, 102 E. Boone Avenue or 509.313.6910, whaleys@gonzaga.edu, www.gonzaga.edu/sexualmisconduct.

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