Quartus II Design Flow with Verilog: CheatSheet

Source Files

```
$ pwd
/Users/talarico/VTut
$ ls -1
light.csv
light.v
light_tb.v
```

Create Project

* Project Name and Directory
* Name of the top-level design **module**
* Project Files and Libraries
* Target Device Family and device
* EDA Tool Setting

File > New Project Wizard

To modify a project:
Project > Add/Remove Files in Project

To edit a new Verilog File with Quartus Text Editor:
File > New > (Design Files > Verilog File)

Family: Cyclone IV E
Device: EP4CE115F29C7

Assignments > Device

Assignments > Settings

Start Compiling the Design

Processing > Analyze Current File > Start > Analysis & Elaboration (→ check syntax and translate Verilog into Generic Boolean eqns.)

Make sure to verify all Info/Warnings/Errors

Tools > Netlist Viewers > RTL viewer

Processing > Analyze Current File > Start > Analysis & Synthesis (→ synthesize HDL into target technology)

Tools > Netlist Viewers > Technology Map Viewer (Post Mapping)

Pin Assignments

Assignments > Pin Planner

If the Pin Planner has issues loading automatically the pinout assignments saved in light.csv put the assignments in a text file light.txt and load it manually.

Assignments > Import Assignments (file name light.txt)

```
$ cat light.txt
# Pin Assignments

To, Direction, Location
x1, input, PIN_AB28
x2, input, PIN_AC28
f, output, PIN_E21
```

6. Continue Compiling the Design

Processing > Start > Start Fitter (→ Place and Route)

Tools > Netlist Viewers > Technology Map Viewer (Post Fitting)

Simulation

Invoke Modelsim

File > New > Project
Project name: lightSim
Project Location: C:/Users/talarico/VTut/simulation/modelsim

Project > Add to project > Existing File:
C:/Users/talarico/VTut/light.v
C:/Users/talarico/VTut/light_tb.v

Project > Add to project > New File

Compile > compile all

Simulate > Start Simulation
+ work
  + light
  + light_tb

vsim > view wave
vsim > add wave sim: /light_tb/*
vsim > run –all (→ the simulation run forever !!)

Simulate > break

To automatically end the simulator use **$stop** statement in the testbench code.

Useful commands to remember:

vsim > restart –force
vsim > run –all
vsim > wave zoomout
vsim > wave zoomfull

Finish Compiling the Design

Processing > Start > Assembler (→ generating the programming file)
sof = SRAM object file

View Reports

Make sure to read carefully the reports generated at each step of the design process.
The reports can be accessed through the Quartus' workspace window or directly in the output_files folder.

10. Programming and Configuring the FPGA

Before Programming the FPGA make sure to set the board in RUN mode (JTAG mode).

Tools > Programmer

Edit > Add File (C:/Users/talarico/VTut/output_files/light.sof)

The hardware Setup must be USB-Blaster [USB-0]

11. Testing the Circuit on the Development Board