CPEN 230L: Introduction to Digital Logic Laboratory
Lab #1: Logic Trainer

Objectives

- Model and simulate the functionality of a simple digital logic expression
- Become familiar with the Elenco XK-550 Digital/Analog Trainer ("Logic Trainer"), the Integrated Circuit (IC) Tester, the 7408 Quad 2-Input AND Gate, and the 7432 Quad 2-Input OR Gate.
- Learn how to build and test a logic circuit on the Logic Trainer.
- Learn how to create a lab report for this class.

PreLab: Icarus Verilog and GTKWave

1. Installing Icarus Verilog and GTKWave

- Install a text Editor on your own computer (examples: Visual Studio Code, emacs, vim, notepad++, etc.). Visual Studio Code can be found at https://code.visualstudio.com/
  If you already have a text editor you are comfortable with skip this step.
- If your computer is a PC with Windows OS install MobaXterm Home Edition v10.4 (portable edition): https://mobaxterm.mobatek.net/download-home-edition.html/
- If your computer is a PC with Windows OS install Icarus Verilog and GTKWave as follows. Go to the url: http://bleyer.org/icarus and download the installation file
  iverilog-10.0-x86_setup.exe
- If your computer is a PC setup the path for Icarus Verilog and GTKWave as shown in the link Instructions to set up the PATH
- If your computer is a Mac follow the instructions in the link Instructions for MAC users
- Test the installation of Icarus Verilog and GTKWave by compiling, simulating, and viewing the simulation waveforms for the supporting files provided: simple.v and simple_tb.v

2: Model and Simulate the SOP (sum of product) circuit E = SW1.SW2 + SW3.SW4

- Copy the supporting files muxgate.v and muxgate_tb.v into sop.v and sop_tb.v
- Modify sop.v to model the circuit E = SW1.SW2 + SW3.SW4 provided in figure 1. The simplest approach is to model the circuit using a structural gate level coding style, that is a coding style similar to the one used in the muxgate.v example provided. The code provided corresponds to the circuit shown in figure 2.

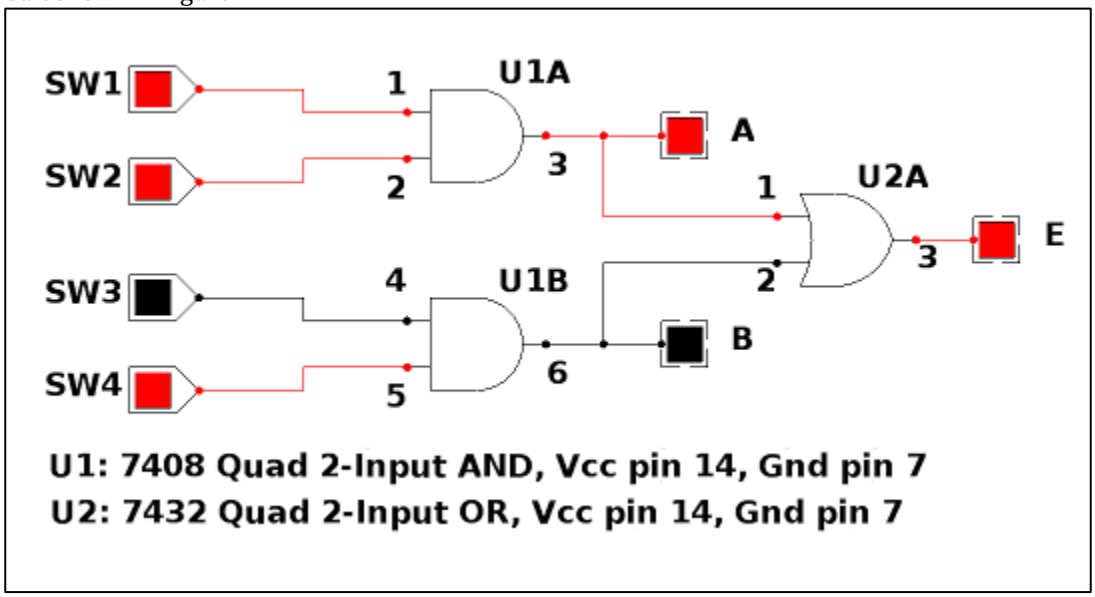


Figure 1. SOP circuit to implement

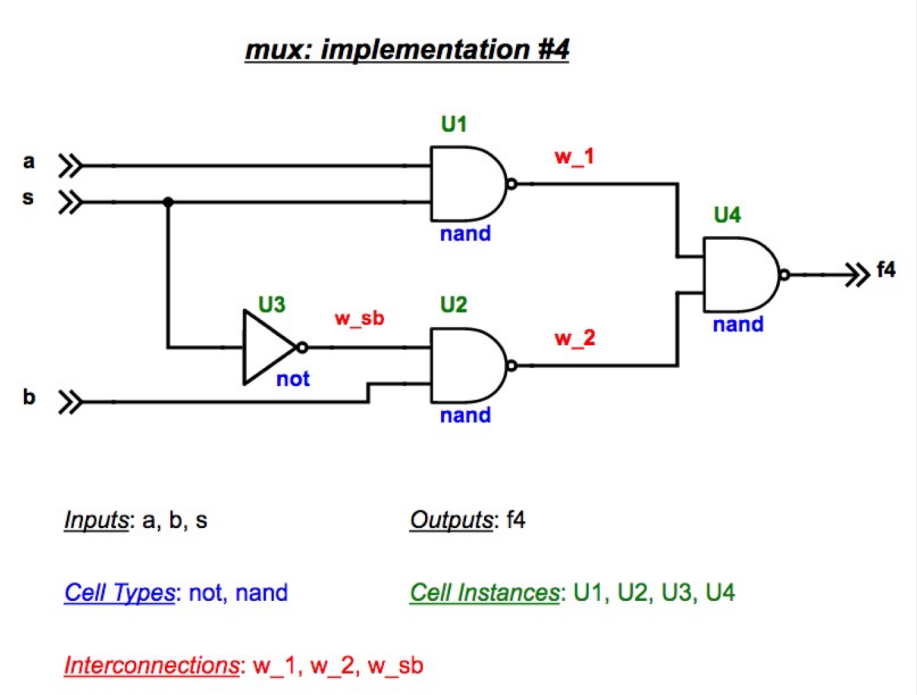


Figure 2. example of mux gate level structural implementation

- Modify sop_tb.v to check the correct functionality of the circuit. Generate a table showing the values of A, B, E for all combinations of SW1, SW2, SW3, SW4

SW1	SW2	SW3	SW4	A	B	E
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

3: Bread Board Tutorial

Read carefully the link Breadboard Tutorial and take a quick look at the links 74F08 data sheet (Quad 2-input AND gate) and 74F32 data sheet (Quad 2-input OR gate).

During Lab: Elenco Logic Trainer, IC Tester, and ICs Data Sheets

Background: Equipment Familiarization (led by the instructor)

- Logic Trainer: Power Switch; +5 Volts & GND (ground); Logic Indicators; Data Switches; Breadboard Area (buses and tie points).
- Logic Probe: See "Logic Probe Overview" below
- IC Testing Station: Read a chip part number. Identify pin 1. Place a chip in the tester socket and verify it works correctly.
- ICs: See the 7408 and 7432 data sheets below, with special attention to "Pin Configuration" and "Logic Diagram".
- Build the circuit and complete the following Truth Table.

SW1	SW2	SW3	SW4	A = SW1.SW2	B = SW3.SW4	E = SW1.SW2 + SW3.SW4
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

- When you are satisfied that your results are correct, show your circuit to your lab instructor.

Reminder: Always clean up at the end of the lab session. Leave everything in better shape than you found it.

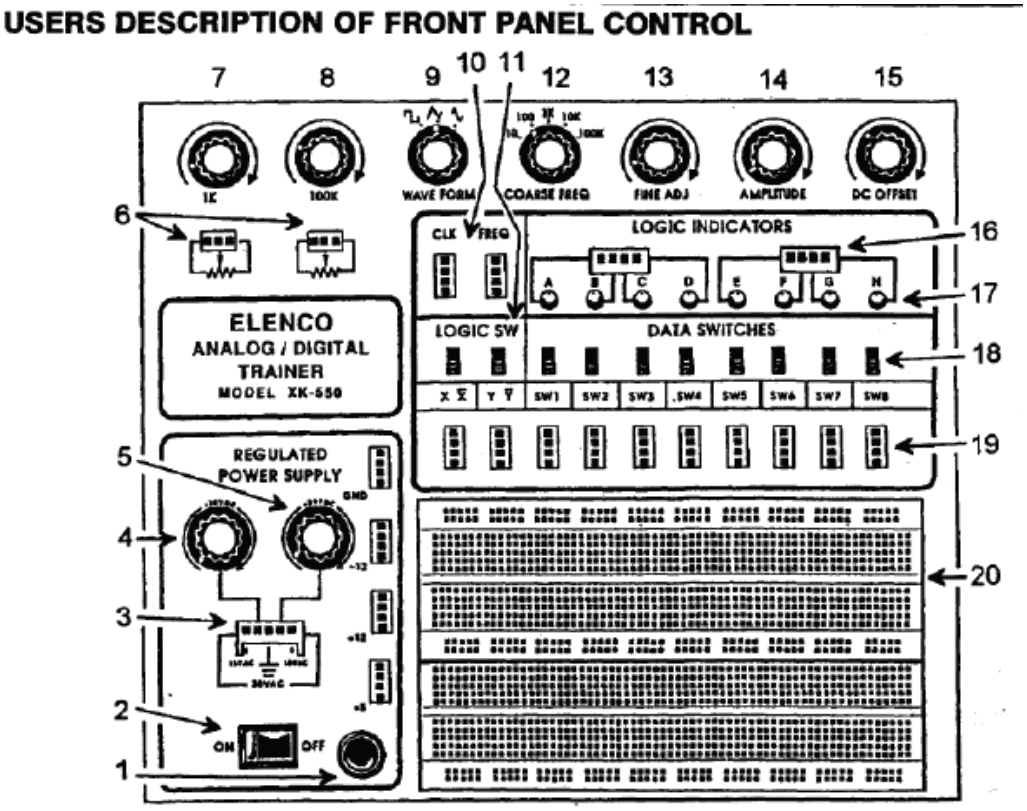
Prelab Deliverables

Before the lab. starts, hand in the following documents:

- sop.v
- sop_tb.v
- screenshot of the table generated through the Icarus Verilog simulation

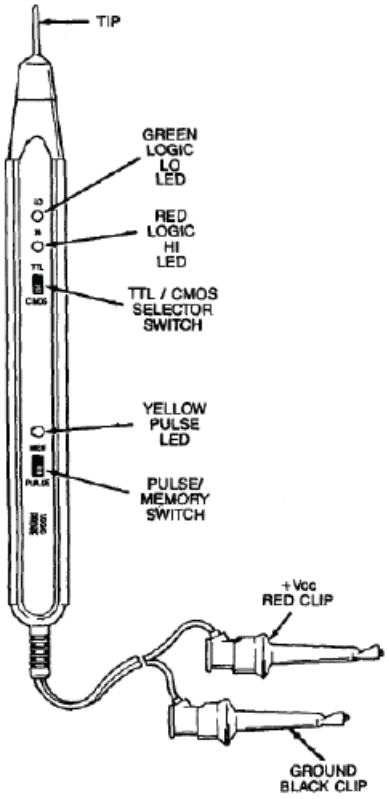
NOTE: A failure to hand in the prelab deliverables will result in a **50% penalty** in the lab's grade.

Logic Trainer Overview (from the Instruction Manual)



1. Fuse holder - Easy access for replacement of 1.25A 250V fuse.
2. On-Off switch – Applies power to all outputs. Switch lights when on.
3. Power output terminals - This provides 30VAC center tapped at 15VAC - also provides output terminal for positive and negative variable voltages.
4. Variable positive voltage control - Varies positive voltage from 1.25 to 20V at indicated output connector pin.
5. Variable negative voltage control - Varies negative voltage from -1.25 to -20V at indicated output connector pin.
6. Output terminals for 1 kΩ and 100 kΩ undedicated potentiometers.
7. 1 kΩ undedicated potentiometer.
8. 100 kΩ undedicated potentiometer.
9. Waveform selection control, square, triangle or sine generator waveforms.
10. Output terminals for all functions as stated, 4 pins per block.
11. Two logic switches - These are no bounce logic switches. Give one signal state change per movement of switch.
12. Selects five ranges of frequencies from 10 to 100,000 hertz.
13. Fine frequency control – Fine tunes function generator and clock frequency.
14. Amplitude control - Function generation output amplitude, 0-15Vpp.
15. DC offset control - controls the DC level of the generator output. DC may be varied ±.10 volts from zero level.
16. Input points for logic indicator LEDs. ‘A' input corresponds with A lamp, etc.
17. Logic Indicators LEDs, total eight.
18. Eight data switches - output 5V or 0V depending on position.
19. Output terminal for all functions as stated, 4 pins per block.
20. Two breadboards containing a total of 1,660 tie points including 6 independent bus lines.

Reference 2: Logic Probe Overview



Applying power to the probe

1. Connect the black clip to GND (-).
2. Connect the red clip to the Vcc (+). Be sure Vcc is less than 20V.

Probe Usage

1. TTL/CMOS switch: The TTL/CMOS switch can be switched to TTL mode for use in TTL circuits. The TTL logic 1 threshold is 2.3V ± 0.2V, logic 0 threshold is 0.8 ± 0.2V. When switched to CMOS mode, the CMOS logic 1 threshold is 70% Vcc, logic 0 threshold is 30% Vcc.

2. Pulse/Memory switch: The logic probe can detect and memorize the level transition. Either positive or negative level transition can be detected or memorized, depending on the mode selected.

a) Pulse position: An input state transition will activate the pulse indicator (flicker for 500 ms).

b) Memory position: An input state transition will activate the pulse indicator (and keep it on until reset). Switch from Pulse to Memory with the probe tip touching a measurement point, not when open circuited.

TYPICAL SIGNALS AND CORRESPONDING LED INDICATION:

ITEMS	WAVEFORM	LED INDICATIONS LEVEL (RED)	PULSE (GREEN)	PULSE (YELLOW)
Logic "1" no pulse activity	1 / 0	●	○	○
Logic "0" no pulse activity	1 / 0	○	●	○
Signal level between "1" & "0"	1 / 0	○	○	○
Logic "1" with pulse	1 / 0	●	○	☆
Logic "0" with pulse	1 / 0	○	●	☆
Pulse train with freq. < 200KHZ	1 / 0	●	●	☆
Pulse train with freq. > 200KHZ	1 / 0	○	○	☆

● LED On ○ LED Off ☆ LED blinks - - - - - - - - ref. level ——— signal