CPEN 230L: Introduction to Digital Logic Laboratory
Lab #2: Combinational Logic with Basic Gates

Objectives

- Evaluate several logic gate ICs using the Logic Trainer.
- Learn how open inputs impact logic gate outputs.
- Build and test a fairly complicated logic function.

Part 1: Logic Operation of Gates

Chips to be tested:

- 7400 Quad 2-input NAND gates
- 7402 Quad 2-input NOR gates
- 7404 Hex Inverters
- 7408 Quad 2-input AND gates
- 7432 Quad 2-input OR gates
- 7486 Quad 2-input XOR gates

Pre-Lab

- Use Icarus Verilog to model and simulate to the operation of the 6 gates listed above. The circuit has 2 inputs SW1 and SW2 (corresponding to switches on the Logic Trainer), 6 gates, and 6 outputs A, B, C, D, E, and F (corresponding to LEDs on the Logic Trainer). The LEDs corresponding to the output of the 6 gates, must be set in the order listed above (A for 7400 to F for 7486). Call the verilog file modeling the circuit basicgates.v, and the file checking its operation basicgates_tb.v

- Use Icarus Verilog to generate the following truth tables showing the expected gate output for all possible gate inputs.

SW1	SW2	A (nand)	B (nor)	D (and)	E (or)	F (xor)
0	0					
0	1					
1	0					
1	1					

SW1	C (not)
0	
1	

- Draw a detailed schematic of the circuit. Include everything a reader would need to recreate your circuit: reference designators, pin numbers, Vcc and Ground, parts list, and Logic Trainer connections. See the attached data sheets for IC details.
- Develop a test procedure for each gate to determine the logic level (0 or 1) associated with an open (not connected to anything) input. For example, "7408 Quad 2-input AND Gate: Set input pin 1 to logic level 1 and leave input pin 2 unconnected. If the output on pin 3 is a 1 (0), then open input pin 2 must have been sensed as a 1 (0)." For 2-input gates, you can assume both inputs behave the same way -- You only need to test one of the two inputs being open, as in the provided example text. Prepare 6 truth tables showing expected gate output.

SW1	SW2	A (nand)	B (nor)	D (and)	E (or)	F (xor)
0	X					
1	X					

SW1	C (not)
X	

During Lab

- Build and test the 6 gates simulated in your pre-lab work. **Tips:** Test one chip at a time, swapping chips into the same breadboard location so power supply and ground need only be connected once. Plan the chip order so all chips with inputs on pins 1 and 2, output on pin 3, are tested in sequence. When testing it is fine to use the same Logic Indicator (A for example) instead of a separate one for each chip as shown in your schematic. **Perform your "open input" test procedure for each chip as its truth table is tested, so each chip is inserted into the breadboard only once.**
- Verify that all 6 chips perform as your truth tables specify (including the open input scenarios)

Part 2: Implementation of a Boolean expression

Consider the Boolean expression below where signals are assigned to switches as: A = SW1, B = SW2, and C = SW3. The indicator H *toggles* state whenever any of the switches A, B, or C changes state. This is the exact expression for the three-way light control example presented in lecture.

H = A B' C' + A' B C' + A' B' C + A B C

Pre-Lab

- Prepare a truth table with columns A, B, C, and H to show output H for all 8 possible values of inputs A, B, and C.

A = SW1	B= SW2	C = SW3	H
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

- Draw a schematic diagram implementing the above expression using only 7404 Inverters, 7408 AND gates, and 7432 OR gates. You will need to synthesize 3-input AND gates and a 4-input OR gate from the gates on those ICs. Include everything needed to build the circuit on the Logic Trainer -- reference designators, pin numbers, Vcc and Ground, parts list, and Logic Trainer connections.
- Model and check the correct operation the circuit with Icarus Verilog (call the file for the circuit: threeway.v and the file for the testing threeway_tb.v). Generate the truth tables showing the expected gate output for all possible gate inputs and make sure they match your expectations.

During Lab

- Build and test the circuit on the Logic Trainer, verifying each row of your truth table.
- When you are satisfied that your results are correct, show your circuit to your lab instructor.

Prelab Deliverables:

Before the lab starts hand in the following documents. A failure to do so will result in a 50% penalty in the lab's grade:

Part 1

- basicgates.v, basicgates_tb.v
- screenshot of the table(s) generated through Icarus Verilog simulation
- detailed schematic of the circuit
- truth tables for the open input testing scenarios

Part 2

- detailed schematic of the circuit
- threeway.v, threeway_tb.v
- screenshot of the table(s) generated through Icarus Verilog simulation