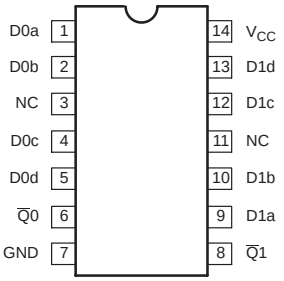
Dual 4-input NAND gate 74F20

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F20	3.5ns	2.2mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
14-pin plastic DIP	N74F20N	SOT27-1
14-pin plastic SO	N74F20D	SOT108-1

PIN CONFIGURATION



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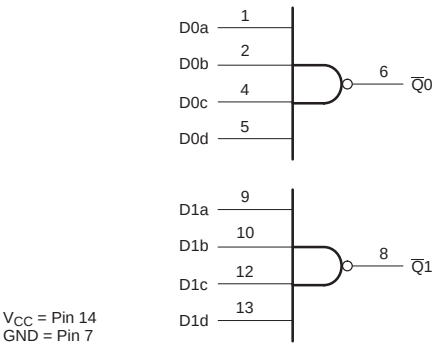
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dna, Dnb, Dnc, Dnd	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}$0, $\overline{Q}$1	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC DIAGRAM



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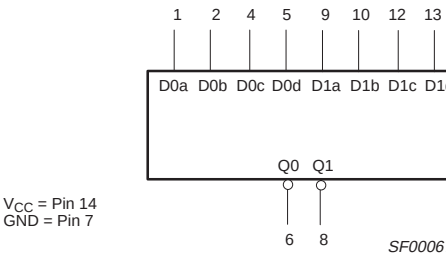
FUNCTION TABLE

INPUTS				OUTPUT
Dna	Dnb	Dnc	Dnd	$\overline{Q}$n
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

NOTES:
H = High voltage level
L = Low voltage level
X = Don't care

LOGIC SYMBOL



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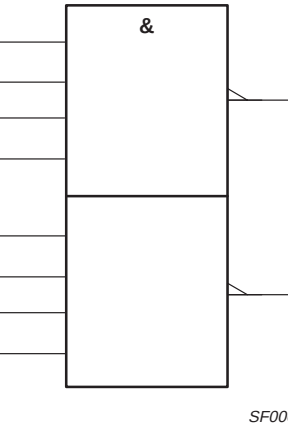
IEC/IEEE SYMBOL



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