CPEN 230L: Introduction to Digital Logic Laboratory
Lab #3: Logic Synthesis with One Gate Type

Purpose
- Simulate AND, OR and NOT functions using only NAND gates and only NOR gates.
- Simulate the logic function of the previous lab using only NAND gates.
- Design, build and test the logic function of the previous lab using only NOR gates.
- Design, build and test a Majority Gate using only NAND gates.

Part 1: Simple logic using only NAND gates and only NOR gates

Pre-Lab: Complete the following diagram to show how AND, OR, and NOT logic can be implemented using only 2-input NAND gates and only 2-input NOR gates. The NAND implementation of the NOT gate is provided as an example. Replace the five "gates here" comments with the number and type of 2-input gates they mention. In this diagram **reference designators, pin numbers, power supply connections, and parts list are <u>not needed</u>**. Use Verilog to verify that each column of outputs behaves the same, for all four possible input values (call the files onegatetype.v and onegateverilog_tb.v).
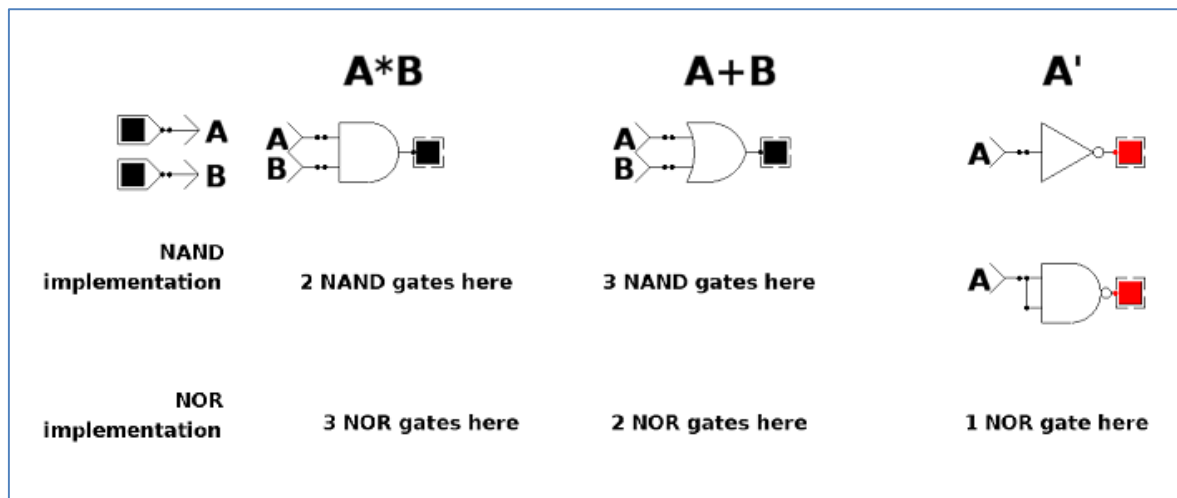

Figure 1. Implementing AND, OR and NOT by using only NAND and NOR gates

There is no During-Lab work for Part 1 and your report does not need to include Part 1.

Part 2: Complex logic using NAND gates

Pre-Lab: Design the expression **H = AB'C' + A'BC' + A'B'C + ABC** using only Quad 2-input or Triple 3-input or Dual 4-input NAND gate chips, and only 3 chips total. (Read the previous sentence carefully.) Leaving gates unused on any of the three chips is fine. Let A = SW1, B = SW2, C = SW3. Draw the schematic diagram of your design. In this diagram **reference designators, pin numbers, power supply connections, and parts list are <u>not needed</u>**. **Tips:** Apply DeMorgan's Theorem to (H')' to convert it to NAND sub-expressions, then figure out how to combine gates to satisfy the 3-chip limit. (This is not an arbitrary requirement, but an example of keeping chip count low to minimize circuit cost.) For example, you can use twelve 2-input gates (4+4+4, 3 chips), or eight 2-input and three 3-input gates (4+4+3, 3 chips), or four 2-input and three 3-input and two 4-input gates (4+3+2, 3 chips), or any other 3-chip combination. Recall that in the previous lab you used two 2-input AND gates to synthesize a 3-input AND gate. A 4-input NAND gate can synthesize a 3-input NAND gate by fixing one input at value 1. Understand and extend these principles. Verify the correctness of your design using Verilog (call the files threewaynand.v and threewaynand_tb.v)

There is no During-Lab work for Part 2, and your lab report does not need to include Part 2

Part 3: Complex logic using NOR gates

Pre-lab: Design the same function as in Part 2 using only Quad 2-input or Triple 3-input NOR gates, 3 chips maximum. Draw the schematic diagram of your design. This time the diagram <u>must include</u> reference designators, pin numbers, Vcc and Ground, and Logic Trainer connections (SW1, SW2, SW3 and H). **Tips:** Convert the expression for H to Product-of-Sums (POS) form, then apply DeMorgan's Theorem to (H')' to convert it to NOR sub-expressions. The datasheet for the 7402 Quad 2-input NOR gate and the datasheet for the 7427 Triple 3-input NOR gate are provided. No 4-input NOR gates are available. Simulate your design using Verilog (call the files threewaynor.v and threewaynor_tb.v).

During-Lab: Build, test and debug the circuit. When working correctly show it to your instructor. Your report for Part 3 should include pre-Lab's diagram image, Procedure Changes (likely "None"), Results (and Discussion. See Lab Report Template for details.

Part 4: Majority Gate using NAND gates

A majority gate produces output 1 when the majority of its inputs have value 1, or output 0 when the majority of its inputs have value 0.

Pre-lab: Design a 3-input majority gate using only NAND gates. See Part 3 for detailed diagram requirements. **Tips:** Similarly, to the "Three-Way Light Control" of the previous lab, go from problem statement to truth table. Use a 3-variable K-Map to reduce the logic expression to simplest Sum-of-Products (SOP) form. Apply DeMorgan's Theorem to convert the expression to NAND sub-expressions. The datasheets for the 7400 Quad 2-input NAND gate, the 7410 Triple 3-input NAND gate and the 7420 Dual 4-input NAND gate are provided. Any working design is fine, but **it is possible to implement this circuit with only 2 NAND chips** from the allowed choices of 7400, 7410, and 7420**.** Simulate your design using Verilog (call the files majoritynand.v and majoritynand_tb.v).

During-Lab: Follow the same instructions as Part 3.

Prelab Deliverables:
Before the lab starts hand in the following documents:
Part 1
   • Schematic diagram showing how to implement AND, OR and NOT logic using only NAND and NOR gates
   • onegatetype.v, onegateverilog_tb.v, snapshot of table(s) generated to verify correct operation
Part 2
   • Schematic diagram
   • threewaynand.v, threewaynand_tb.v, snapshot of table(s) generated to verify correct operation
Part 3
   • Detailed schematic diagram
   • threewaynor.v, threewaynor_tb.v, snapshot of table(s) generated to verify correct operation
Part 4
   • Detailed schematic diagram
   • majoritynand.v, majoritynand_tb.v, snapshot of table(s) generated to verify correct operation

NOTE: A failure in submitting the prelab deliverables will result in the lab's grade to be halved.