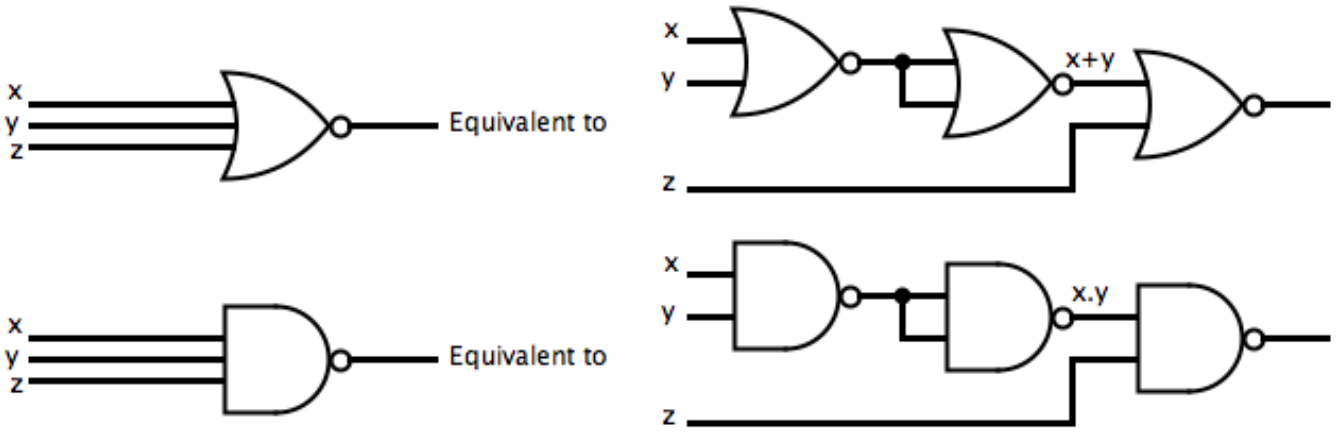
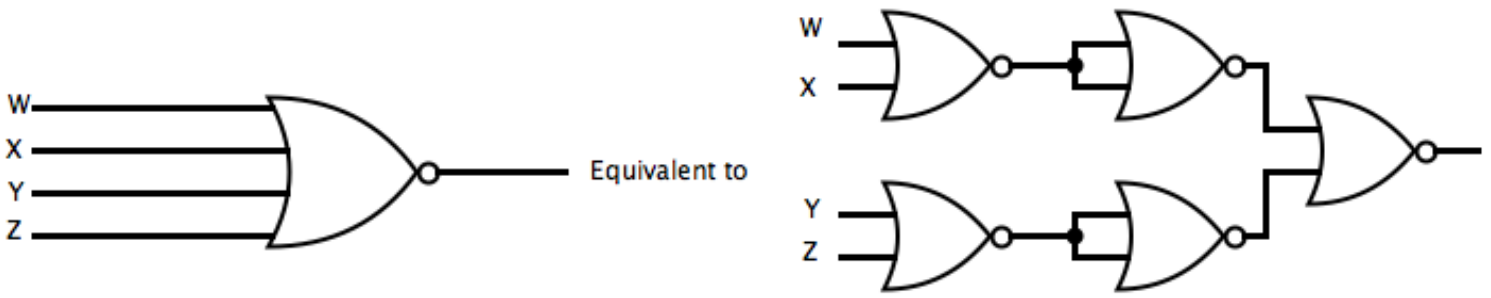
Realizing a Three-input NOR/NAND Gate from Two-input NOR/NAND Gates



Generalization



Help for Part 3 of Lab 3