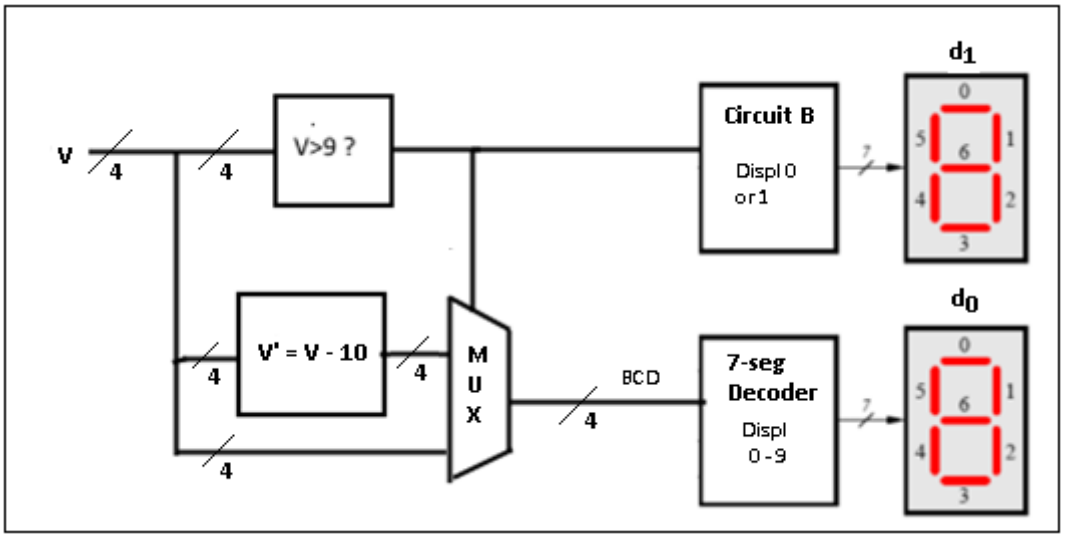
CPEN 230L: Introduction to Digital Logic Laboratory

Lab #8: Numbers and Displays

Purpose

- Gain proficiency with Verilog, ModelSim, Quartus, the DE2-115 board, hierarchical design, and development processes.
- Design, simulate, and synthesize combinational logic to convert binary to binary-coded decimal (BCD).

Four-bit binary to two-digit BCD conversion



The above diagram shows a 4-bit number V converted into a 2-digit BCD. For example, if V = binary 1100 (decimal 12) then d1 displays 1 and d0 displays 2. If V = binary 0011 then d1 displays 0 and d0 displays 3. The comparator labeled "V > 9?" outputs 1 if true, 0 if false. That result gets displayed on 7-segment display d1, and makes the MUX select V or V−10 to display on d0.

Pre-Lab

- Create the following directory structure and files:

```
Lab8\
  bin2bcd\
    sim\
      bin2bcd_tb.v
    src\
      bin2bcd_top.v
      bin2bcd.v
      dec7seg.v
    synth\
      bin2bcd_top.tcl
      bin2bcd_top.sdc
```

- Module **dec7seg** is the "7-seg Decoder" block in the diagram. Its input is a 4-bit vector representing decimal values 0 through 9. Its output is a 7-bit vector providing the values needed to display "0" through "9" on a DE2-115 board 7-segment display. When the input value is > 9, the output is Don't Care.
- Module **bin2bcd** encloses "Comparator (V > 9)", "V' = V−10", and "MUX" blocks in the diagram. Its input is a 4-bit vector representing decimal values 0 through 15. Its output is two 4-bit vectors providing the input

value converted to BCD. **Notice this is different than what the diagram indicates.** In the diagram, the 1-bit "V > 9?" comparator output drives "Circuit B". We will instead let the comparator output be a 4-bit BCD value and only use values 0 or 1, to drive a second "7-seg Decoder" block. This is an example of **reuse** – module dec7seg is more complicated and costly than needed to implement "Circuit B", but using it saves development and test time.

- Module **bin2bcd_top** connects the previous modules to the DE2-115 board switches and displays. Input will come from SW[3:0]. Output will go to the HEX1 and HEX0 7-segment displays (the rightmost two on the board).
- Module **bin2bcd_tb** tests module bin2bcd. Its stimulus to the input of bin2bcd is the decimal values 0 through 15 (binary 0000 through 1111). It verifies that the output from bin2bcd is BCD 00 through 15.
    - Notice this **leaves modules bin2bcd_top and dec7seg untested** during the simulation phase of development. Their contents are specific to the DE2-115 board, and they will be debugged during in-lab synthesis. This demonstrates the common development process of making a circuit (bin2bcd) and then using it with either a **simulation test bench** (bin2bcd_tb) or a **hardware-specific synthesis shell** (bin2bcd_top and dec7seg). This way, if circuit bin2bcd were ported to another hardware platform, only the hardware-specific shell would have to change.
- File **bin2bcd_top.tcl** can be completed from previous lab content and information found in the DE2-115 User Manual (a lab 5 handout).
- File **bin2bcd_top.sdc** can be completed from previous lab content.
- Compile all Verilog code to eliminate compile errors and verify bin2bcd_tb output using Icarus Verilog.

During-Lab

- Use ModelSim and directory \Lab8\bin2bcd\sim to test module bin2bcd.
- Use Quartus and directory \Lab8\bin2bcd\synth to build the circuit on the DE2-115 board. All warnings need to be eliminated or understood and ignored for good reason.
- When completed **show your Quartus warnings and circuit to your instructor**.
- Your lab report should include:
    - contents of the six files listed in the pre-lab work, in the order shown there
    - ModelSim Wave and Transcript results
    - Quartus RTL Viewer results (whatever you think will best help your target reader)
    - Quartus warnings you ignored for good reason, and why you ignored them
    - anything else that will help your target reader complete and understand the lab

Pre-Lab deliverables

- dec7seg.v, bin2bcd.v, bin2bcd_tb.v, bin2bcd_top.v
- snapshot of simulation waveforms and/or true tables generated to verify the correctness of the operation of bin2bcd

NOTE: Pre-Lab deliverables are mandatory. The lack of deliverables will result in a 50% penalty of the lab's grade.