CPEN 230L: Introduction to Digital Logic Laboratory
Lab #12 (Final Project): Five-Digit Up/Down Timer

- **Design** a 5-digit up/down timer with disable and load controls.
  - If counting up, the timer will wrap around from 99.999 ms to 00.000 ms.
  - If counting down, the timer will wrap around from 00.000 ms to 99.999 ms.
  - The load value for the timer is two 4-bit digits, the two most significant digits of the 5-digit count. The three least significant digits always load to values of 0.
  - The load control is active-low and synchronous.
  - The disable control is active-low and synchronous.
  - The timer count must be synchronous.
  - Both the update time (default 1ms) and counting base (default 10) of the timer can be changed by higher-level Verilog code. It must also be possible for the higher-level code to optimize the number of flip-flops used in counting the update period of the timer (hint: use the `$clog2` verilog function). The number of flip-flops used to count each digit should be fixed at 4, and counting base is limited from 2 to 16.
- **Simulate** the timer, with these waveform details:
  - The simulation must show 2 clock cycles per ms.
  - The simulation must show the timer counting down in base 2 from 00000 to 11111 (wrap-around) to 11110 … 00000 (its full range) to 11100 (a few counts further).
  - The simulation must show the timer updating every ms. For example, at time = 1 ms, the timer should transition from 11111 to 11110.
  - The simulation must demonstrate that the load control is active-low and synchronous, loading the value 10000 and counting-up from that a few counts.
  - The simulation must demonstrate that the disable control is active-low and synchronous.
- **Synthesize** the timer on the DE2-115 board:
  - Use HEX5 to HEX1 for the timer output display. The gap on the DE2-115 board between displays HEX4 and HEX3 serves as the decimal point location. For example, to display a time of 12.345, the 7-segment displays will appear as
    "-- 12 345-"where "-" indicates all segments off.
  - Times less than 10s have their 10s digit blank. For example, the time 1.234 displays as "-- -1 234-" not "-- 01 234-".
  - Pressing KEY3 stops the timer. Releasing KEY3 allows it to continue.
  - Pressing KEY0 loads the timer to the BCD value on switches SW[17:14], SW[13:10]. For example, if SW[17:10] are set to 0001 0010 then 12000 will be loaded into the timer. If the value on the switches is greater than the counter per-digit terminal count, its value should be accepted as the terminal count. For example, if the counter is counting in base 10, SW[17:14] being set to 1100 (12) should load the value 9 into the counter's most significant digit.
  - SW[9] controls up (1) or down (0).
  - Verify your synthesis can change counter base and update rate only modifying the _top module to make it count hexadecimal seconds -- Change the counter base to 16 and change the update rate to 16^–3 = 244.140 us. (The leading 0 for times < 10_{16} seconds should be blanked, similar to the base 10 case.)
- **Demonstrate** your simulation, base 10 synthesis, and base 16 synthesis to your instructor.
- **Report** your project as described in the Lab Report Template.