CPEN 230L: Introduction to Digital Logic Laboratory
Lab T1: Verilog-based design, implementation and simulation of circuits using Quartus and Modelsim

Objectives

- Learn to design logic circuits using Field Programmable Gate Arrays (FPGAs) rather than discrete ICs
- Getting familiar with the use of Quartus (Altera/Intel's CAD tool for the design and implementation of circuits into FPGAs)
- Getting familiar with the use of Modelsim (Mentor Graphics' CAD tool for simulating the operation of a circuit)

Part 1. Quartus/Modelsim Tutorial

Pre-lab:

Use Verilog Icarus and GTKwave to model and check the correct operation of the circuit provided in the supporting file light.v. The associated testbench is provided in the file light_tb.v

During-lab

- *Option 1:* go through the tutorial: *Quartus II Verilog Design Flow: Basic Steps Summary*
- *Option 2:* if you find the tutorial suggested in option 1 too terse and hard to follow, please feel free to go through the original Altera's tutorial (*Altera: Quartus II Introduction Using Verilog. 2010*), **BUT** make sure to **skip section 6** (follow instead "*section 7: simulation"* of the more condensed tutorial recommended as option 1*)* **and section 7-2.**

- When you are comfortable that everything is working as expected show it to your instructor.

- *Recommended:* if you have a little extra time and would like to learn more about ModelSim take a look at the document *Altera: Using ModelSim to Simulate Logic Circuits in Verilog (2015)*

Pre-lab deliverable:

- Snapshot of the simulation waveforms (it must be in black & white)

NOTE:

- From now on, coding in Verilog using the gate level style is BANNED!
- As we move forward in the semester I strongly encourage you to read the concise document on how to write good quality Verilog for synthesis written by Cliff Cummings. The document is posted at the bottom of the Course Info link.