Lab. 4 - Solution Hints (LCD)

The controller's initialization procedure, can be done as follows:

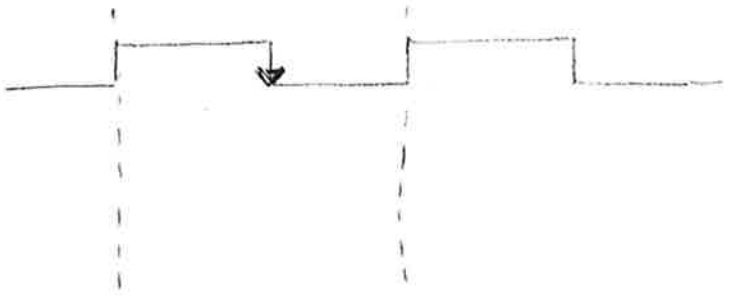
1. Turn ON the power
2. Wait > 15ms after V_{DD} rises to 4.5V (or > 40 ms after 2.7V)
3. execute instruction "Function Set" (37 µs) with RW=0, RS=0, DB= 0011----
4. wait for 4.1 ms
5. execute instruction "Function set" (37 µs) with RW=0, RS=0, DB= 0011----
6. wait > 100 µs
7. execute instruction "Function set" (37 µs) with RW=0, RS=0, DB= 0011----
8. execute instruction "Function set" (37 µs) with RW=0, RS=0, DB= 0011NF-- choose N and F (number of display lines and font)
9. execute instruction "Display on/off control" (37µs) with RW=0, RS=0, DB= 0000 1000
10. execute instruction "Clear Display" (1.52 ms) with RW=0, RS=0, DB= 0000 0001
11. Execute instruction "entry mode" (37 µs) with RW=0, RS=0, DB= 0000 01 I/D S Choose I/D and S (Increment/Decrement and shift)

cursor/blink, shift or not the display)

1. and 2. are abundantly elapsed during the FPGA programming phase

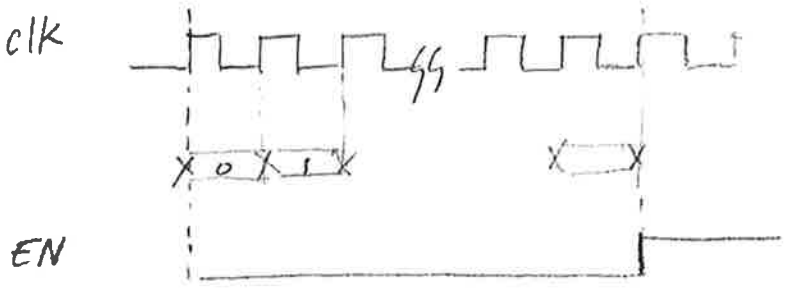
$37\,\mu s + 4.1\,ms = 4.137\,ms$

$37\,\mu s + 100\,\mu s = 137\,\mu s$



EN

the actual writing occurs at the negative edge of EN



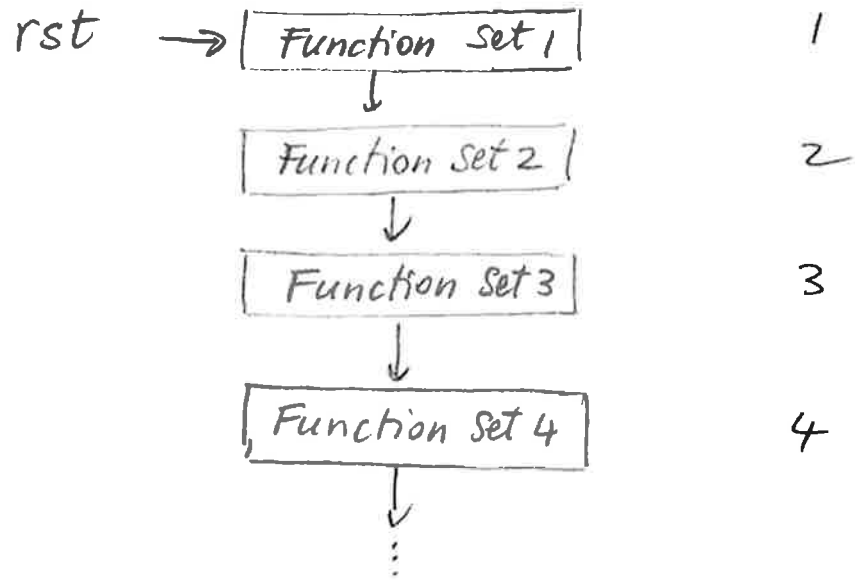
$T_{clk} = 20\,ns$ (50 MHz)

$50001 \times 20\,ns \times 2 = T_{EN} \cong 2\,ms$ (2ms + 40ns)

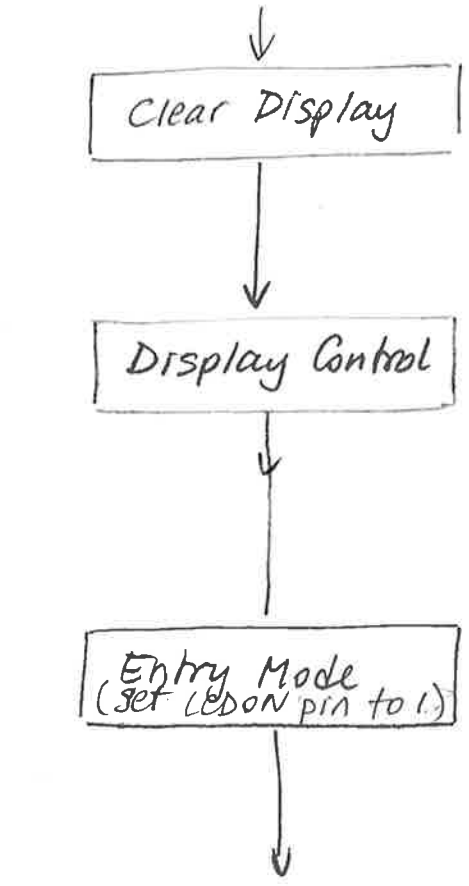
A low frequency clock (EN) is used to move the FSM from one state to another.
Every instruction will have ~ 2ms to complete which is more than any execution time required.

Because the actual writing occurs at the negedge of EN, the machine must move from one state to another at the positive edge of EN, such that RS, R/W, and DB will be firmly available when EN's negedge occurs.

The initialization and setup procedure consists of 7 states



The first four states initialize the controller in the LCD to operate with an 8-bit bus, and a 2 line mode and 5x8 dot characters



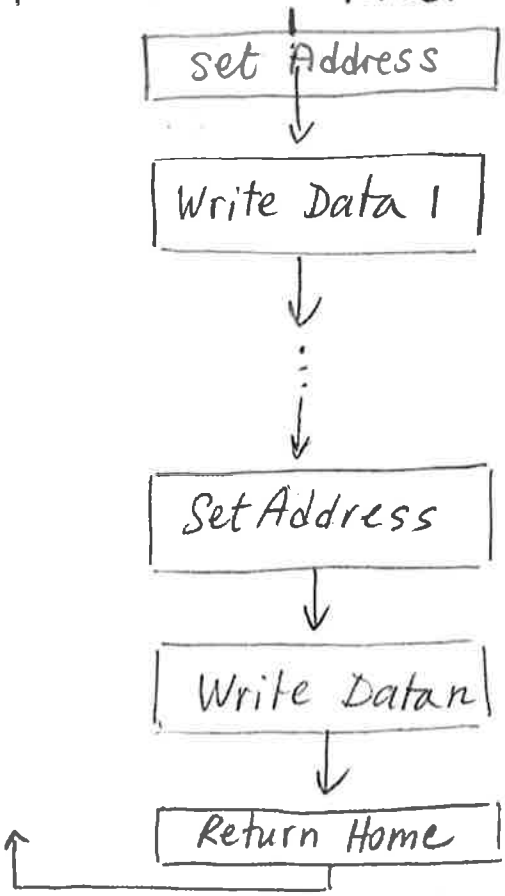
the display is cleared and the memory addr. is zeroed (cursor return to the beginning of line 1)

The display is turned on, while the cursor and blink are kept OFF

The RAM address is set to increment mode, no shift *

= register set

In all the 7 states RS is kept low to select the instruction register and so is R/W because information must always be written



write data in DDRAM thru the Data Register (to select the data register RS must be set high, RW=0)

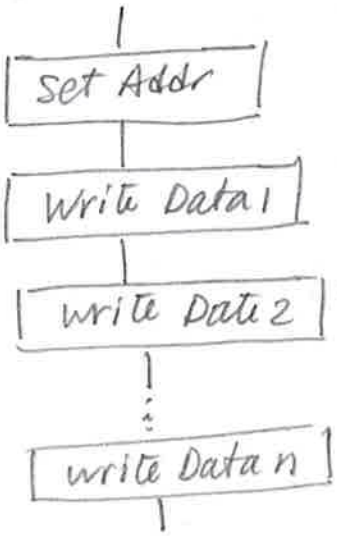
Set DDRAM address (RS=0, R/W=0)

The memory addr. is zeroed (the cursor return to the beginning of line 1) but w/o clearing the display

The controller employs 7 bits to address the LCD characters, hence with a total of 128 addresses, distributed over two lines of 64 addresses each (0-63 in the first line, 64-127 in the second).

This addressing scheme is independent from the actual LCD size. In our case the LCD size is 16×2, but still the first character is at address 0, while the first char in the second line is at address 64.

* Having the RAM address in increment mode allows to write "consecutive" characters without the need of providing the address of every char (we need to pass the addr. only of the first char.)



However
If we want to write char. in non consecutive locations we need to return home and then set Addr

Instruction	RS	RW-	DB7 ... DB0	Description	Max. exec. time (*)
1) Clear Display	0	0	0 0 0 0 0 0 0 1	Clears display and sets DD RAM address to zero.	1.52 ms
2) Return Home	0	0	0 0 0 0 0 0 1 X (X=don't care)	Returns display to origin and sets DD RAM address to zero.	1.52 ms
3) Entry Mode Set	0	0	0 0 0 0 0 1 I/D S	Sets cursor direction and display shift during read and write. I/D=1 increment DD RAM address, =0 decrement S=1 shift display, =0 do not shift	37 us
4) Display ON/OFF Control	0	0	0 0 0 0 1 D C B	D=1 display on, =0 off C=1 cursor on, =0 off B=1 blink char., =0 do not blink	37 us
5) Cursor or Display Shift	0	0	0 0 0 1 S/C R/L X X	Moves cursor or display without changing DD RAM contents. S/C=1 shift display, =0 shift cursor R/L=1 shift to right, =0 shift to left	37 us
6) Function Set	0	0	0 0 1 DL N F X X	Sets bus size, number of lines, and digit size (font). DL=1 8-bit bus, =0 4-bit bus N=0 1-line operation, =1 2-line F=0 5x8 dots, =1 5x10 dots	37 us
7) Set CG RAM Address	0	0	0 1 A A A A A A	Sets CG RAM address to AAAAAA	37 us
8) Set DD RAM Address	0	0	1 A A A A A A A	Sets DD RAM address to AAAAAAA	37 us
9) Read Busy Flag and Address	0	1	BF A A A A A A A	Reads busy flag and address counter	0 us
10) Write Data to CG or DD RAM	1	0	D D D D D D D D	Writes data into DD RAM or CG RAM (defined by last DD or CG RAM address set)	41 us
11) Read Data from CG or DD RAM	1	1	D D D D D D D D	Reads data from DD RAM or CG RAM (defined by last DD or CG RAM address set)	41 us
(*) For 270 kHz internal oscillator; for other frequencies (100 to 500 kHz), multiply time given by 270 kHz/foscillator.					

FIGURE 23.13. LCD controller (HD44780U or KS0066U) instruction set.