Tutorial 4

The goal of this lab. is to design, verify and synthesize a synchronous 4x32 bits FIFO inside the Cyclone IV EP4CE115F29 FPGA provided on your DE2-115 board. The synthesis process must be fully constrained and automated that is, all constrains should be entered into a script file in SDC format. Make sure to include in your script also any report you feel useful to check that the synthesis has been performed successfully. Save the results of your reports in a file called fifo.rpt.

Synchronous FIFO Specifications

A synchronous FIFO is a First-In-First-Out queue consisting of a storage array with control logic that manages the read and write of data and generates status flags. The number of rows of the array is called the DEPTH of the FIFO, and the bit length of each row (i.e., the number of columns of the array) is called the WIDTH of the FIFO.

A Synchronous FIFO has a single clock port for both data-read and data-write operations. Data presented at the module's data-input port (DIN) is written into the next available empty FIFO location on a rising clock edge when the write-request input (WR) is high.

The FIFO full status output (FULL) indicates that no more empty locations remains in the module's internal array. Data can be read out of the FIFO via the module's data-output port (DOUT) in the order in which it was written by asserting read-request (RD) prior to a rising clock edge. The FIFO-empty status output (EMPTY) indicates that no more data resides in the module's internal memory.

The FIFO status cannot be corrupted by invalid requests. Requesting a read operation while the EMPTY flag is active will not cause any change in the current state of the FIFO. Similarly, a write operation while the FULL flag is active will not cause any change in the current state of the FIFO. The RESET signal clears internal control logic and the status flags