ALTERA's "Development" Methodology

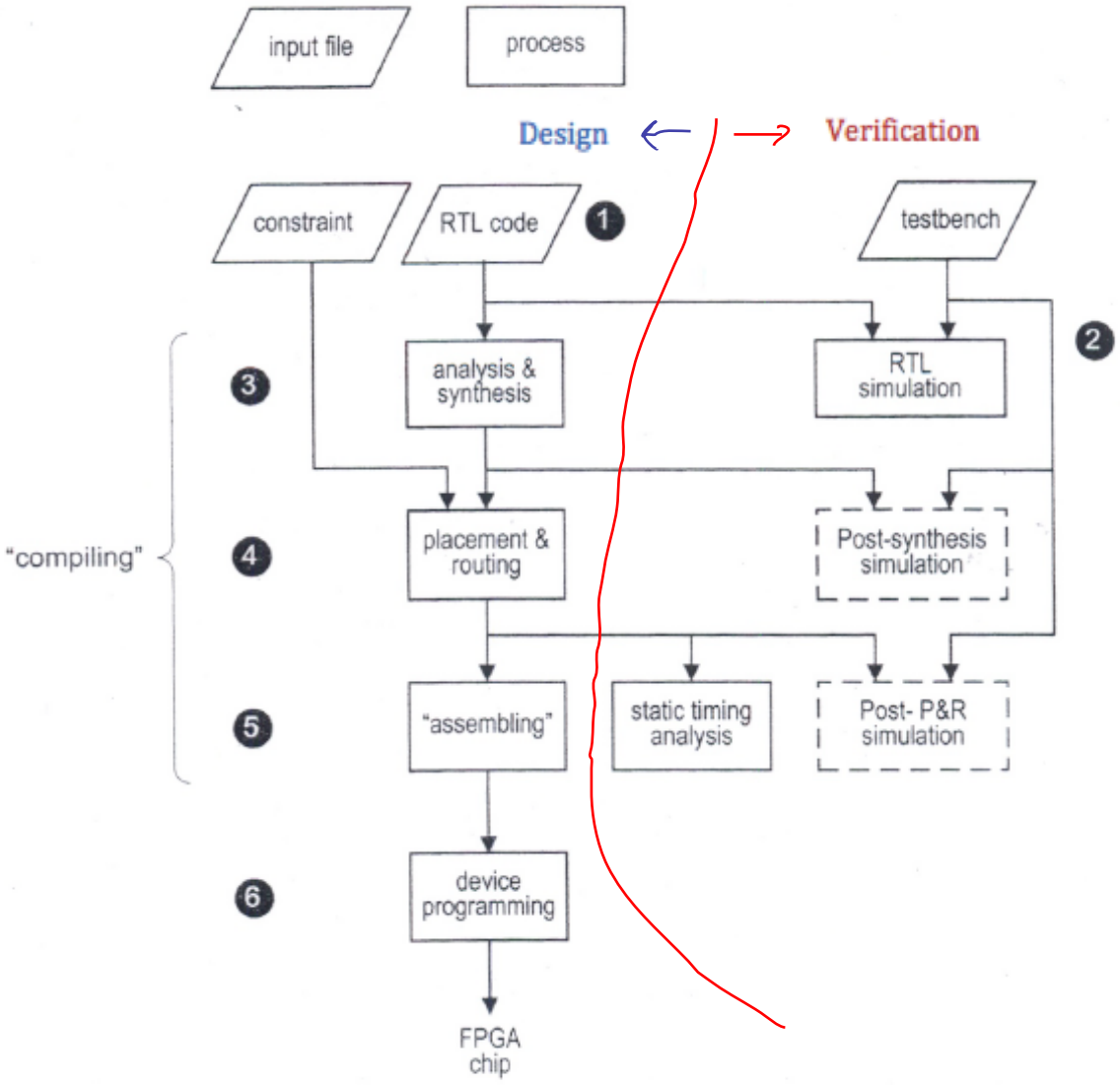

Figure 3.7 Development flow.

RTL = Register Transfer Level

Analysis and Synthesis = check HDL code and construct gate level netlist

P&R = derive physical layout inside the FPGA chip (a.k.a. *fitting*)

Assembling = generate the configuration file (a.k.a. bit file)

Device programming: = downloading the configuration file into the target device

Overview of Altera's Quartus II software tools

ISE (integrated Software Environment) Window Structure:

1. Project Navigator
2. Tasks Window (a.k.a. process window)
3. Messages Window (ak.a. log window)
4. Workplace Window

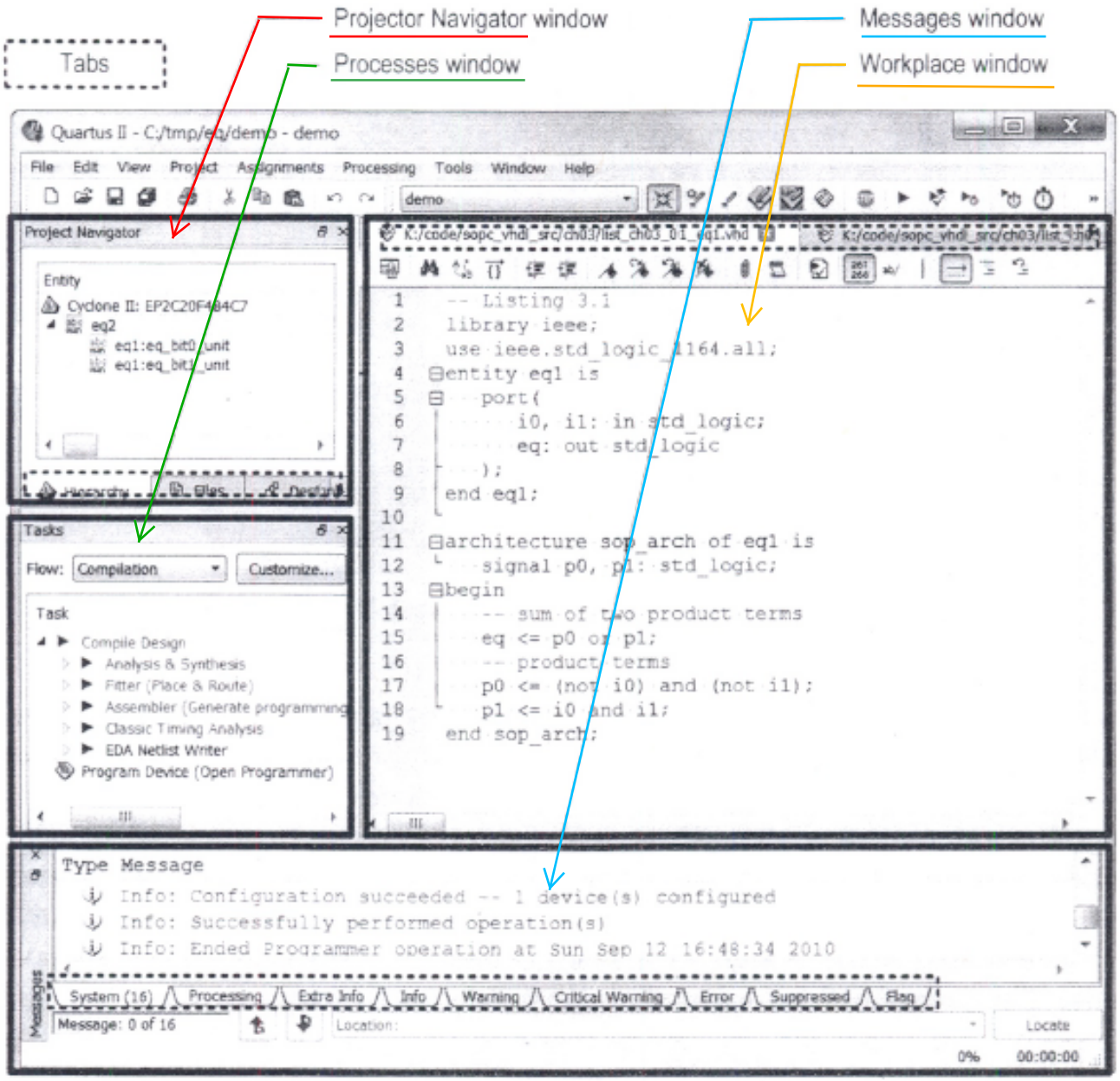

Figure 3.8 Typical Quartus II GUI window.

Checklist of Basic Development Steps (FPGA based design)

1. Create the Logic Design
    a. Create a project (workspace selection, device selection, EDA tools selection → set preferences)
    b. Create or add HDL files
    c. Check HDL syntax (analysis)

2. Create an HDL Test bench and perform RTL simulation

3. Synthesis and Implementation
    a. Create constrains (Pin Assignment, Timing, etc)
    b. Run the Synthesis tool and the fitter tool (P&R)
    c. Create and check design reports

4. Assemble and Program
    a. Connect the download cable (USB blaster)
    b. Run the assembler tool to generate the configuration file (a.k.a. bit file)
    c. Download the configuration file

The development board used in this class is ALTERA's DE2-115. The board provides the following hardware:

- Altera Cyclone IV EP4CE115F29C7 FPGA device
- Altera Serial Configuration device – EPCS64
- USB Blaster (on board) for programming; both JTAG and Active Serial (AS) programming modes are supported
- 2MB SRAM
- Two 64MB SDRAM
- 8MB Flash memory
- SD Card socket
- 4 Push-buttons
- 18 Slide switches
- 18 Red user LEDs
- 9 Green user LEDs
- 50MHz oscillator for clock sources
- 24-bit CD-quality audio CODEC with line-in, line-out, and microphone-in jacks
- VGA DAC (8-bit high-speed triple DACs) with VGA-out connector
- TV Decoder (NTSC/PAL/SECAM) and TV-in connector
- 2 Gigabit Ethernet PHY with RJ45 connectors
- USB Host/Slave Controller with USB type A and type B connectors
- RS-232 transceiver and 9-pin connector
- PS/2 mouse/keyboard connector
- IR Receiver
- 2 SMA connectors for external clock input/output
- One 40-pin Expansion Header with diode protection
- One High Speed Mezzanine Card (HSMC) connector
- 16x2 LCD module

Figure 2.1 and 2.2 shows the layout of the DE2-115 board.

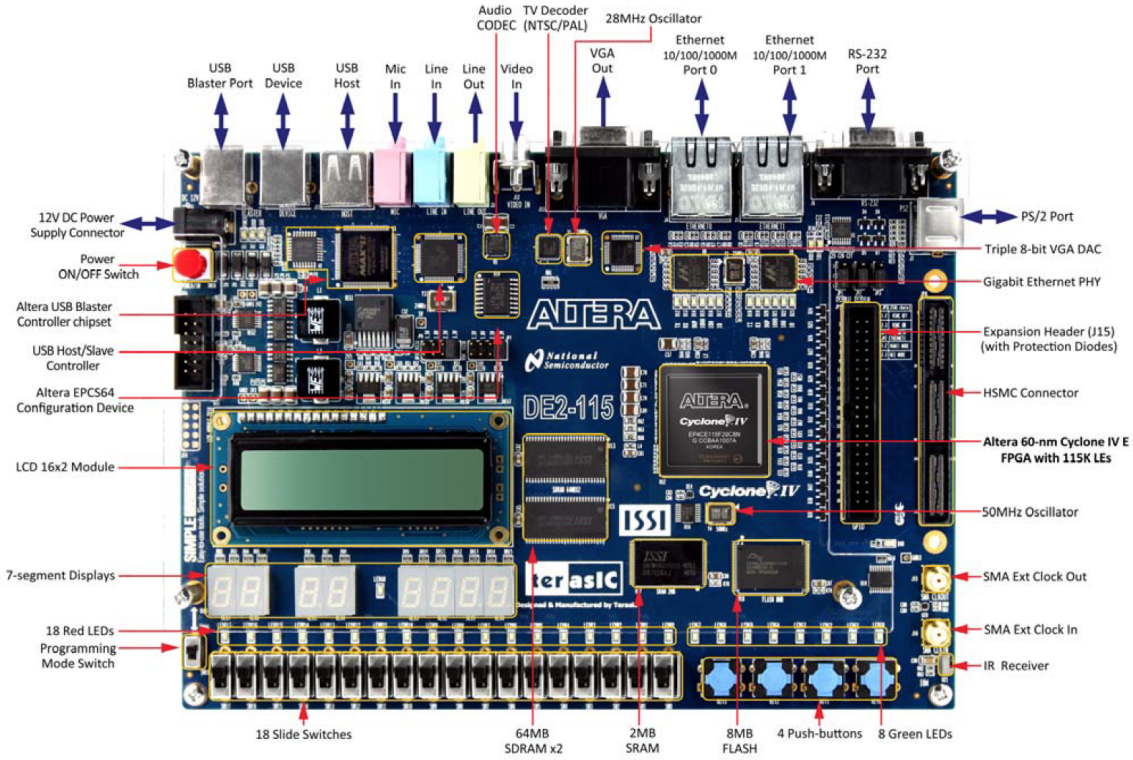

Figure 2-1 The DE2-115 board (top view)

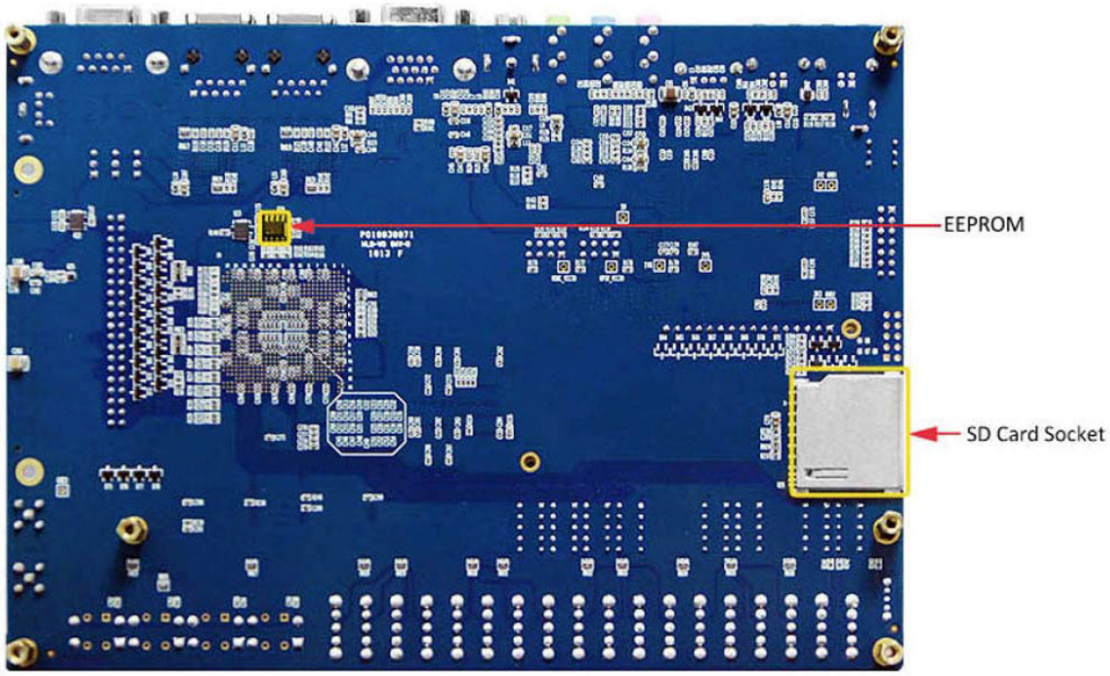

Figure 2-2 The DE2-115 board (bottom view)