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Designing Reliable Digital Systems

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Design only Synchronous Systems

- Asynchronous circuits may cause problems, especially when "glitch" prone combinational logic is used to clock or reset storage elements

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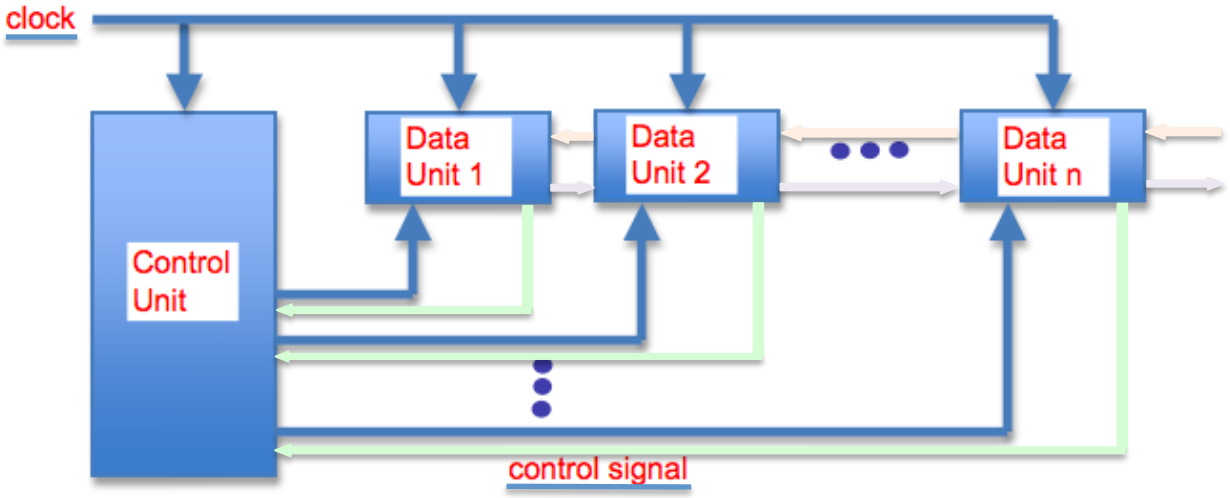
Synchronous Systems

- All clock inputs to flip flops, registers, counters, and FSMs are driven directly from the system clock
- All state changes occur immediately following the active edge of the clock signal
- All switching transients (glitches), and switching noise occur between clock pulses and have no effect on system functionality



We can think of any digital system as composed of a control section and a data path section.

No glitches in the control signals

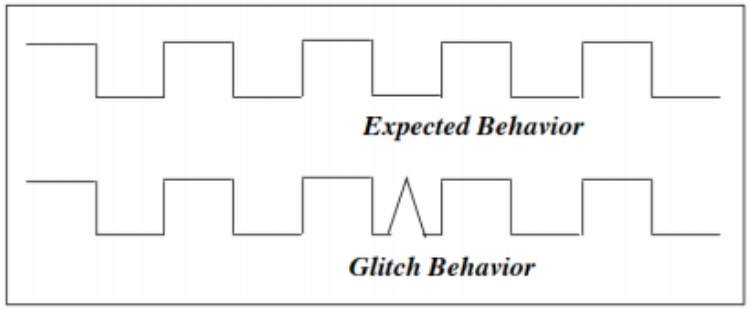


Figure 4.4
Glitch Behavior

Some circuits, such as the 2-to-1 multiplexer in Figure 4.5, invariably cause glitches.

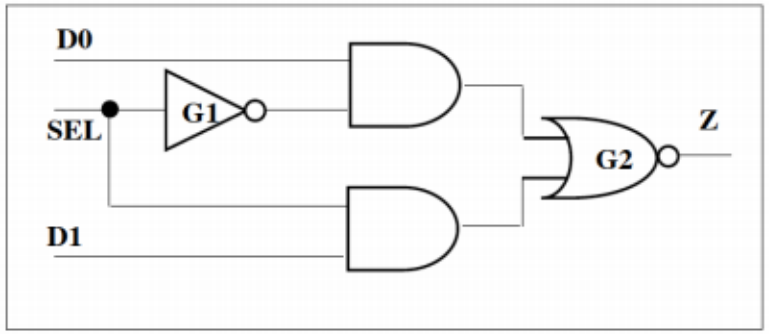


Figure 4.5
Glitch Generating Mux

However:

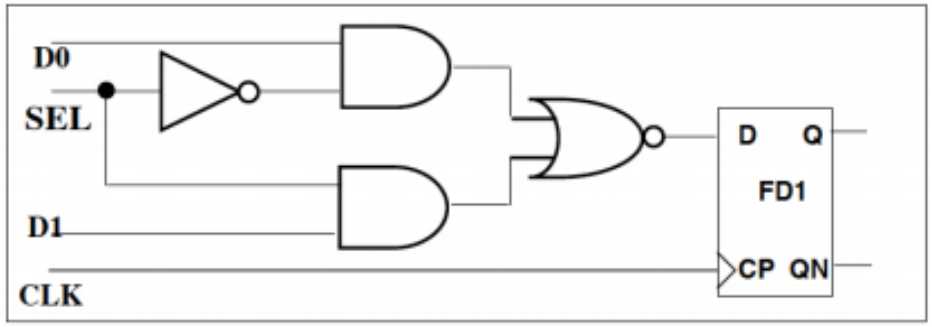


Figure 4.7
The Glitch Doesn't Matter Here

Avoid gated clocks

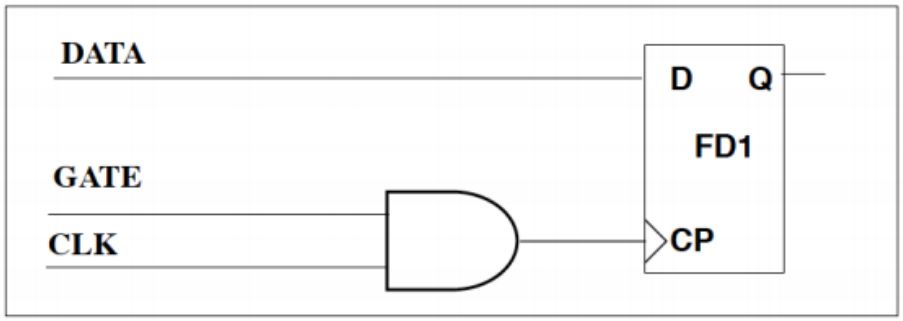


Figure 4.8
A Gated Clock

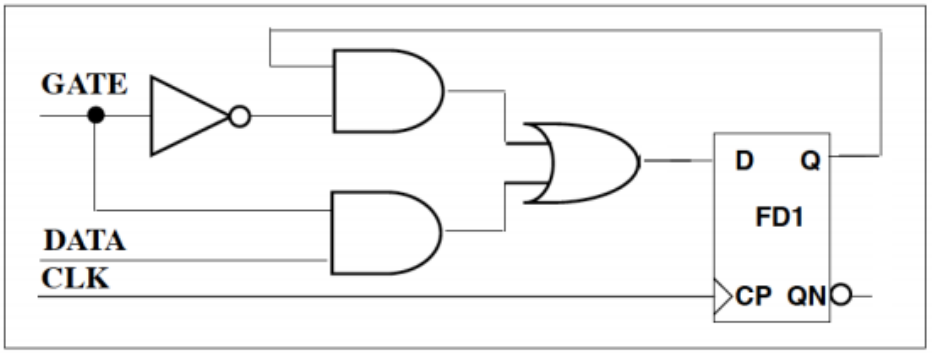


Fig. 4.9
Control the Data instead of gating the clock