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Introduction to FPGAs

Conceptual Structure of an FPGA Device

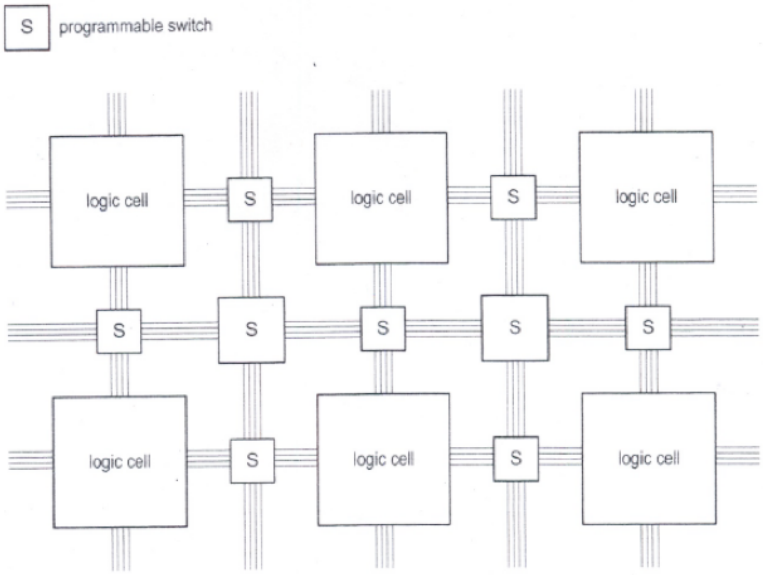
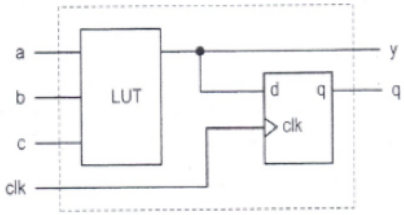


Figure 3.1 Conceptual structure of an FPGA device.

Logic Cell = Logic Element for Altera =
Configurable Logic Block for Xilinx



(a) Conceptual diagram

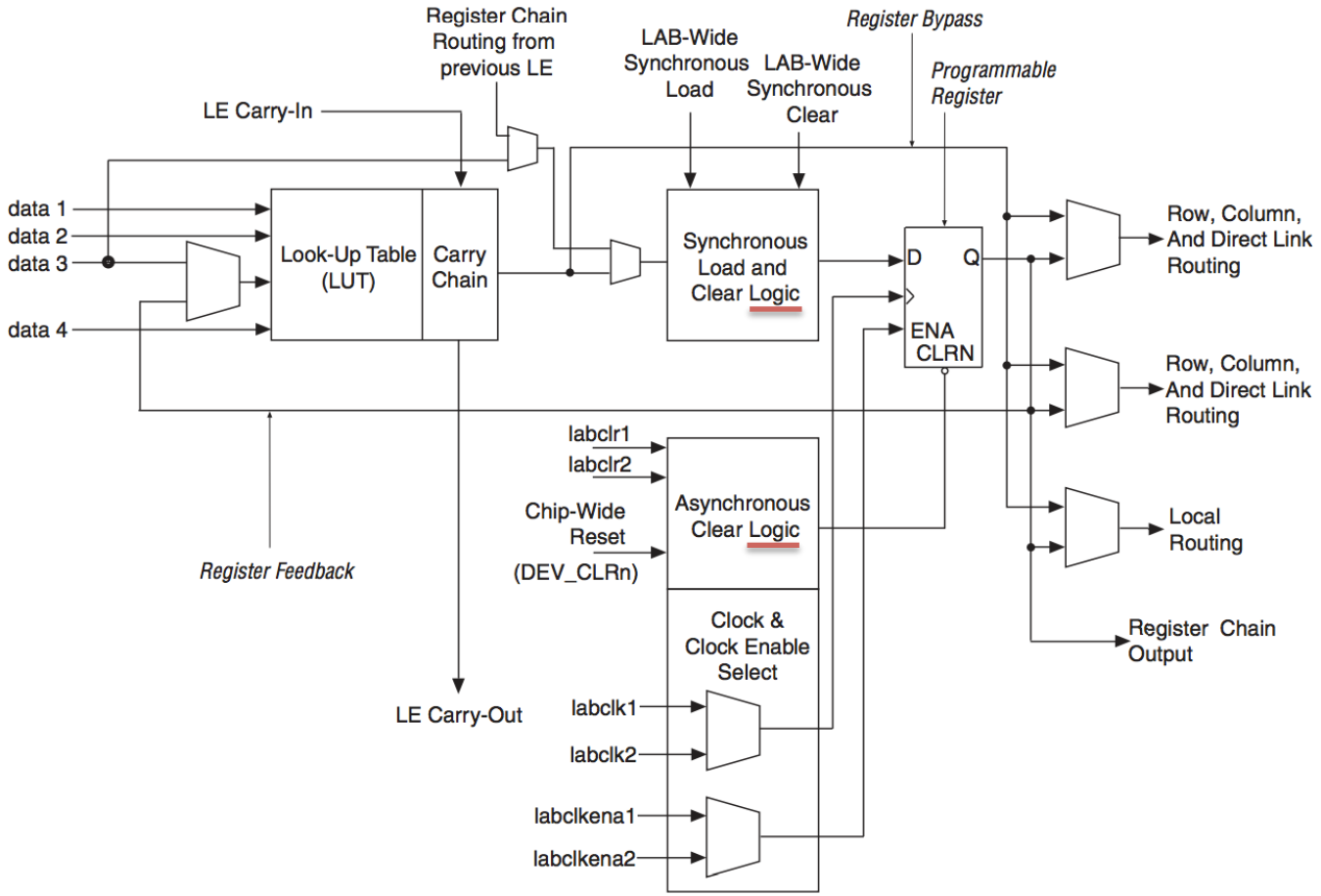
a b c	y
0 0 0	0
0 0 1	1
0 1 0	1
0 1 1	0
1 0 0	1
1 0 1	0
1 1 0	0
1 1 1	1

(b) Example table (XOR gate)

Figure 3.2 Three-input LUT-based logic cell.

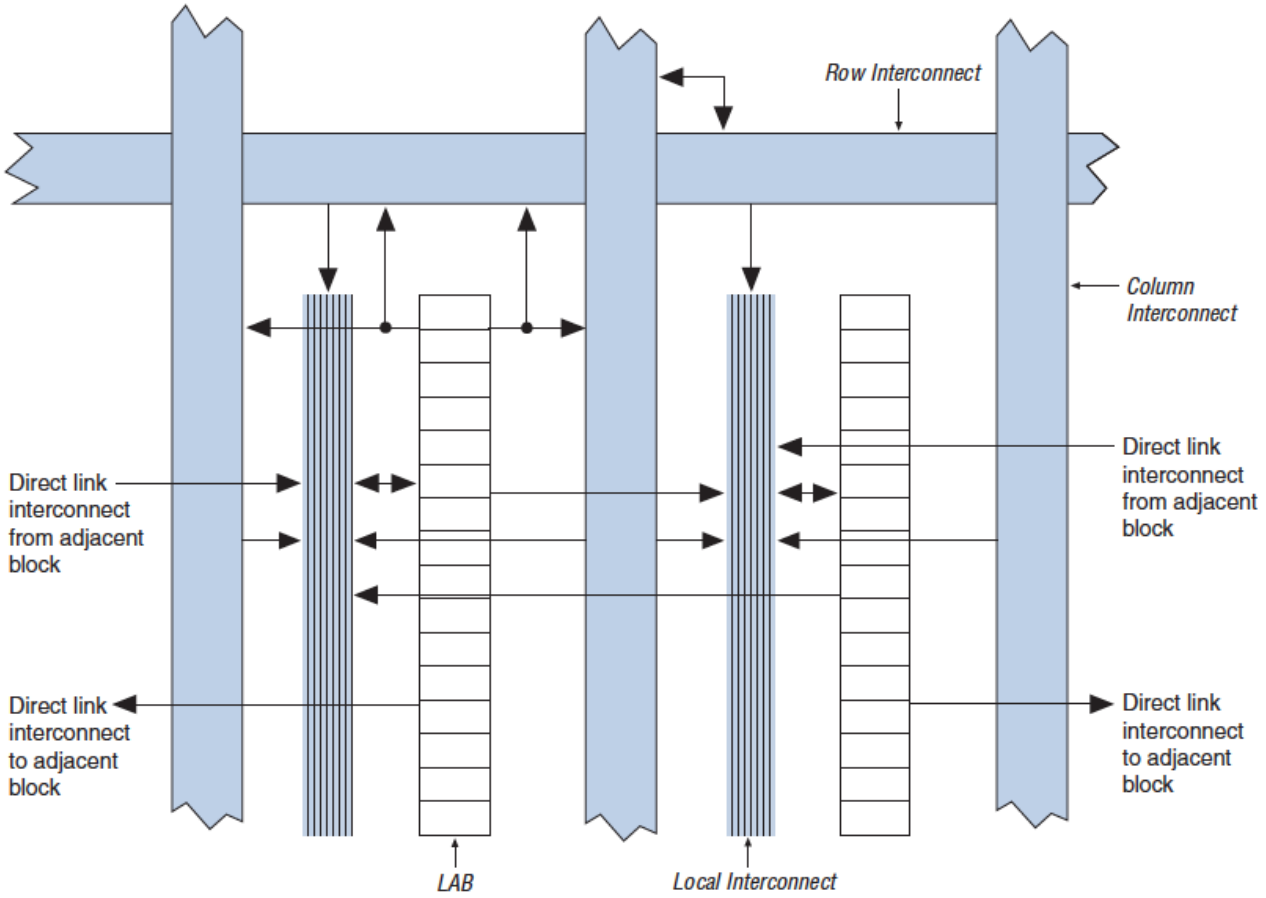
FPGA's Fabric

Figure 2–1. Cyclone IV Device LEs



FPGA's Fabric

Figure 2–4. Cyclone IV Device LAB Structure (LAB = Logic Array Block)



For the Cyclone IV family 1 LAB = 16 LEs

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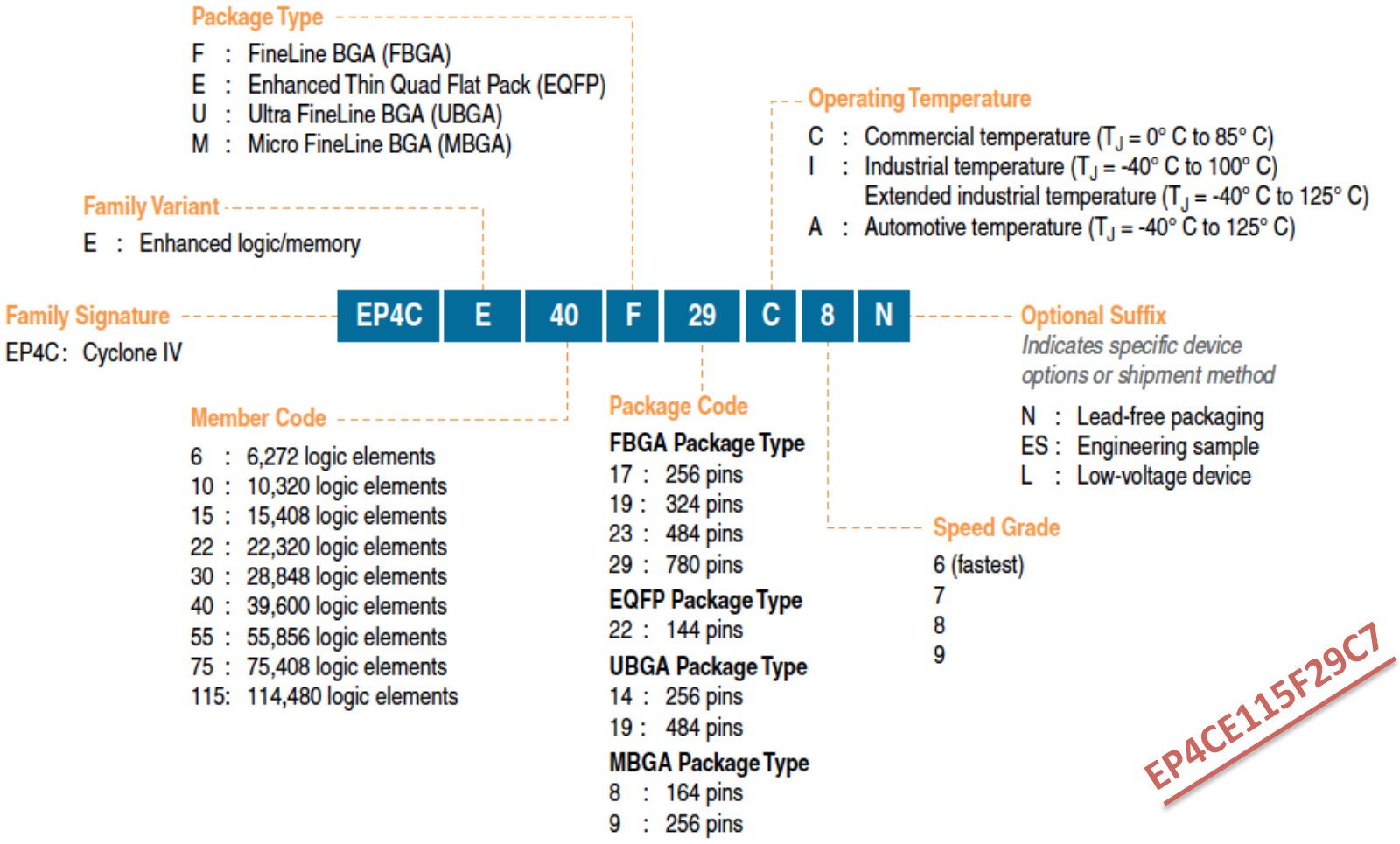
Altera Cyclone IV-E Family

Figure 1–3. Packaging Ordering Information for the Cyclone IV E Device



EP4CE115F29C7

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FPGA Device on the DE2-115 Board

- The DE2-115 board uses the following Device: EP4CE115F29C7 (supply voltage for internal logic is 1.2V typ.)

Table 1–1. Resources for the Cyclone IV E Device Family

Resources	EP4CE6	EP4CE10	EP4CE15	EP4CE22	EP4CE30	EP4CE40	EP4CE55	EP4CE75	EP4CE115
Logic elements (LEs)	6,272	10,320	15,408	22,320	28,848	39,600	55,856	75,408	114,480
Embedded memory (Kbits)	270	414	504	594	594	1,134	2,340	2,745	3,888
Embedded 18 × 18 multipliers	15	23	56	66	66	116	154	200	266
General-purpose PLLs	2	2	4	4	4	4	4	4	4
Global Clock Networks	10	10	20	20	20	20	20	20	20
User I/O Banks	8	8	8	8	8	8	8	8	8
Maximum user I/O (1)	179	179	343	153	532	532	374	426	528

Note to Table 1–1:

(1) The user I/Os count from pin-out files includes all general purpose I/O, dedicated clock pins, and dual purpose configuration pins. Transceiver pins and dedicated configuration pins are not included in the pin count.

- Cyclone IV-E devices are manufactured using the TSMC 60nm low-k dielectric process.

Released in 2009