
Hardware Description Languages (HDL)

Common HDLs

- Verilog
 - IEEE Standard 1364-2005
- VHDL = VHSIC HDL
 - IEEE Standard 1076-2008 ← First to be standardized
- System Verilog (SV)
 - IEEE Standard 1800-2012
- SpecC
- SystemC
 - IEEE Standard 1666-2011
- ...



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VHDL

V *Very High Speed Integrated Circuit*

H *Hardware*

D *Description*

L *Language*

HDLs vs. Software Languages

Concurrent (parallel) statements
vs.
Sequential statements

Role of HDLs

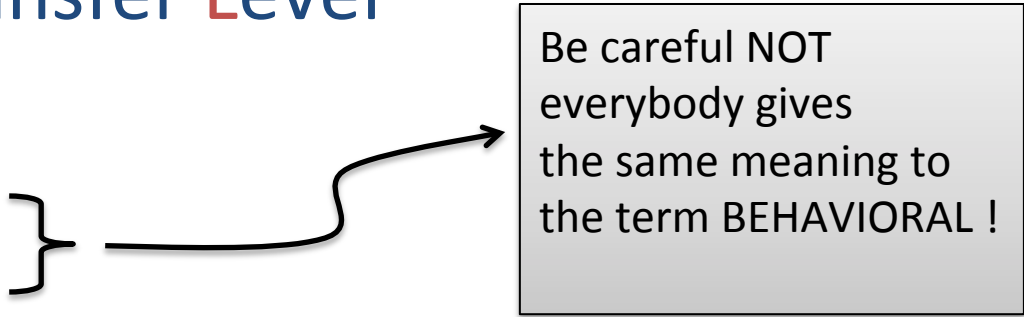
- **Design Description and Documentation**
 - unambiguous definition of components, functionality and interfaces
- **Design Simulation**
 - verify system/subsystem performance and functional correctness prior to design implementation
- **Design Synthesis**
 - automated generation of hardware circuit

HDL Benefits

- **Raising the design abstraction level** (hiding details)
 - The design task become simpler
 - The design is less error prone
 - Productivity is increased
- **Interoperability**: it is possible to combine models at multiple levels of abstraction
- **Technology independence**: models are portable
- **Design re-use** (faster design to market)
- **Cost reduction**

HDL coding styles

- Register Transfer Level
- Structural
- Behavioral }

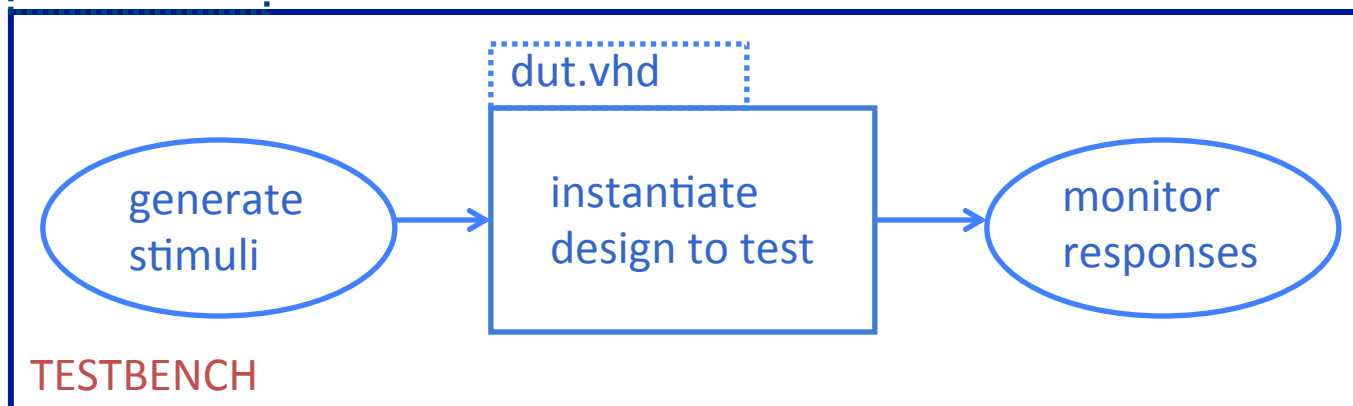


Be careful NOT everybody gives the same meaning to the term BEHAVIORAL !

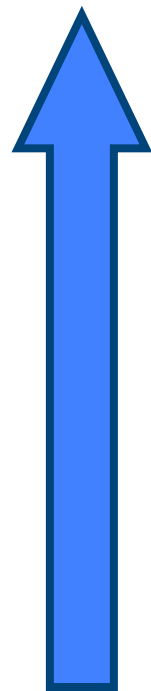
HDL Applications

- High Level Modeling (Behavioral style)
- Design Entry (Structural & RTL styles)
- Simulation (Behavioral style)
 - Validation by mean of a test bench

dut_tb.vhd



HDL coding styles vs. Abstraction



Behavioral

RTL

Structural

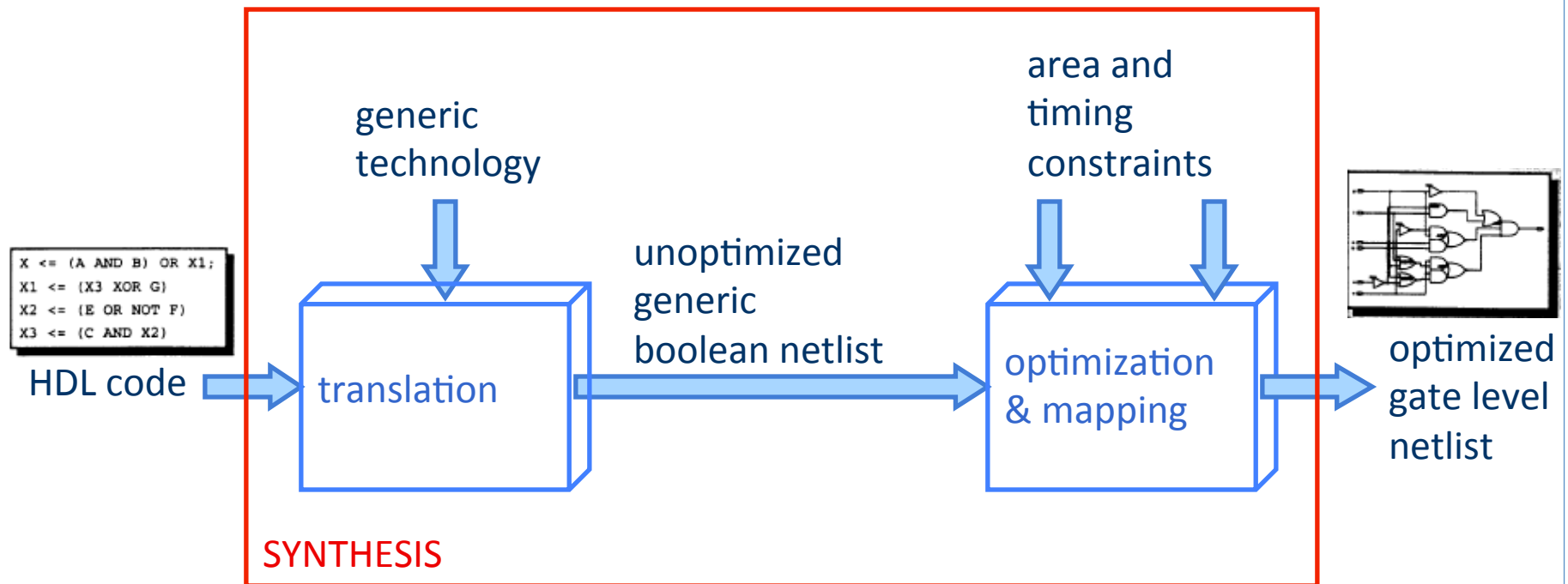
Behavioral coding

- Describe Behavior
 - functionality and performances
- All language features can be used



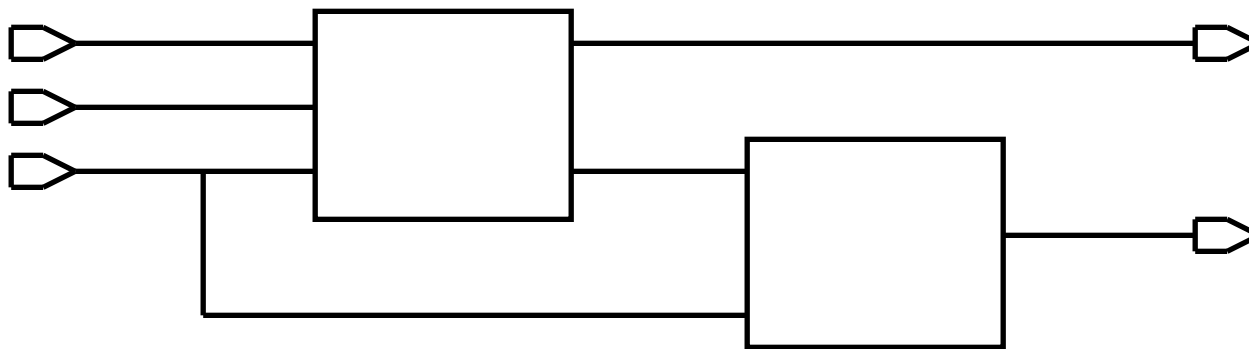
RTL coding

- Only a small subset of the Language statements can be mapped into “Silicon”.



Structural Level coding

- Sub-Modules interconnection
- Primitive cells interconnection (net-list)
- The code consists of a bunch of port mappings and components



VHDL Building Units

- **Entity**
the “symbol” interface (input/output ports)
- **Architecture**
one of the several possible implementation of the design
- **Configuration**
binding between the symbol and one of the many possible implementation.
It can be used to express hierarchy