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VHDL: Operators and Attributes

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VHDL Operators

- Assignment operators
- Logical operators
- Arithmetic operators
- Relational operators
- Concatenation operator
- Overloading

Very useful Tool especially in writing TBs
Same as in C++, Java, etc.

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Assignment operators

Assignment operators work on any type of data

<= Used to assign a value to a SIGNAL.

:= Used to assign a value to a VARIABLE, CONSTANT, or GENERIC. Used also for establishing initial values.

=> Used to assign values to individual vector elements or with OTHERS.

```
signal x : std_logic;
constant size_c : integer size := 7;
variable y: std_logic_vector (3 downto 0);
signal w: std_logic_vector (0 to size_c);

x <= '1';
y := "0000";
w <= "10000000";                    -- LSB is 1
w(0 to size_c) <= "10000000";  -- LSB is 1
w <= (0 => '1', others => '0');-- LSB is 1
```

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Logical operators

- The data must be of type bit, std_logic, std_ulogic (or the respective _vector version)

- NOT
- AND
- OR
- NAND
- NOR
- XOR
- XNOR

Precedence ? → Use parenthesis !!!

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Arithmetic operators

- Depending on the operator the data can be of type:
  - INTEGER (operators: +, −, *, /, **, MOD, REM, ABS)
  - SIGNED (operators: +, −, *, /, **, ABS)
  - UNSIGNED (operators: +, −, *, /, **, ABS)
  - REAL (operators: +, −, *, /, **, ABS) (not synthesizable)

+	Addition	synthesizable
−	Subtraction	
*	Multiplication	synthesizable with restrictions
/	Division	
**	Exponentiation	
MOD	Modulus	non synthesizable
REM	Remainder	
ABS	Absolute value	

Section 9.2 IEEE Std 1076-2008 Reference Manual

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Relational Operators

- Relational operators work on any data type

=	Equal to
/=	Not equal to
<	Less than
>	Greater than
<=	Less than or equal to
>=	Greater than or equal to

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Shift Operators

- Introduced in VHDL 93
  - SLL Shift Left Logical
  - SRL Shift Right Logical
  - SLA Shift Left Arithmetic
  - SRA Shift Right Arithmetic
  - ROL Rotate Left
  - ROR Rotate Right

- We can live without them !!

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Concatenation operator: &

- works on bit, std_logic, std_ulogic (and respective _vector extensions)

```
subtype byte_t is std_logic_vector (7 downto 0);
subtyte nibble_t is std_logic_vector (3 downto 0);
signal a : nibble_t;
signal b : nibble_t;
signal c : byte_t;
a    <= “0001”;
b(0) <= ‘0’;
b(3 downto 1) <= “111”; -- b <= “1110”
c <= a(3) & b(0) & a(2 downto 0) & b(3 downto 1); -- c <= “00001111”
```

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Common (predefined) Attributes

Table 4.2
Attributes.

Application	Attributes	Return value
For regular DATA	d'LOW	Lower array index
	d'HIGH	Upper array index
	d'LEFT	Leftmost array index
	d'RIGHT	Rightmost array index
	d'LENGTH	Vector size
	d'RANGE	Vector range
	d'REVERSE_RANGE	Reverse vector range
For enumerated DATA	d'VAL(pos)◆	Value in the position specified
	d'POS(value)◆	Position of the value specified
	d'LEFTOF(value)◆	Value in the position to the left of the value specified
	d'VAL(row, column)◆	Value in the position specified
For a SIGNAL	s'EVENT	True when an event occurs on s
	s'STABLE	True if no event has occurred on s
	s'ACTIVE◆	True if s is high

◆ Not Synthesizable

VHDL allows the construction of user defined attributes.
We can live without them !!!