GONZAGA UNIVERSITY

VHDL: Delay Models

GONZAGA UNIVERSITY

Delay Models in VHDL

- Inertial delay
  - Default delay model
  - Suitable for modeling delays through devices with inertia (e.g. logic gates)
  - Pulses shorter than a device's delay are not propagated to its output
- Transport delay
  - Model delays through elements with no inertia, e.g., wires
  - no inertia = all input events are propagated to output signals
  - Any pulse, no matter how short, is propagated
- Delta delay
  - What about models where no propagation delays are specified?
  - Infinitesimally small delay is automatically inserted (after 0ns) by the simulator to preserve correct ordering of events
  - The delta delay is a special case of inertial delay with delay infinitesimally small

GONZAGA UNIVERSITY

Inertial Delay Example

- General form:

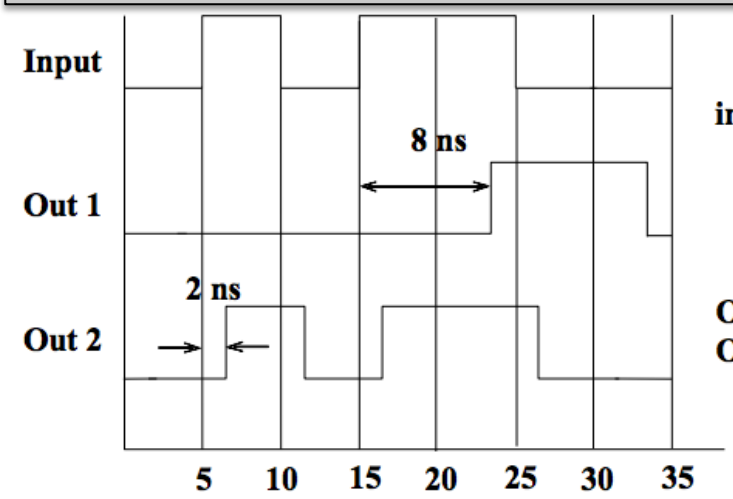
A pulse whose duration is shorter than the time limit specified in the reject clause will not be transmitted

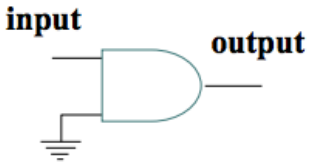
```
signal <= reject time-expression inertial value-expression
          after time-expression
```

```
Example:
Out_1 <= inertial Input after 8 ns;
Out_2 <= inertial Input after 2 ns;
```

The default time limit in the reject clause is given by the time in the after clause.
The default time in the after clause is a Δ delay

NOTE: it is an error if the pulse rejection limit is negative or smaller than the first delay_time





Out 1: gate propagation delay 8ns
Out 2: gate propagation delay 2ns

The following three assignments are equivalent to each other:

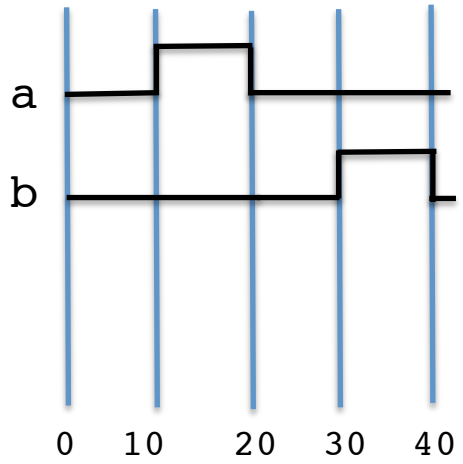
Out_2 <= Input **after** 2 ns;
Out_2 <= **inertial** Input **after** 2 ns;
Out_2 <= **reject** 2 ns **inertial** Input **after** 2 ns;

talarico@gonzaga.edu

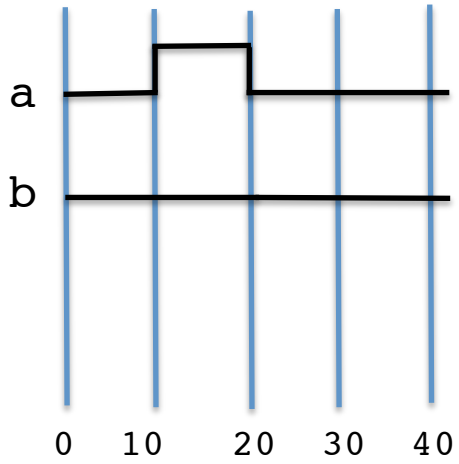
GONZAGA UNIVERSITY

Transport Delay Example

```
ARCHITECTURE beh OF delay_line
BEGIN
  b <= TRANSPORT a AFTER 20 ns;
END beh;
```



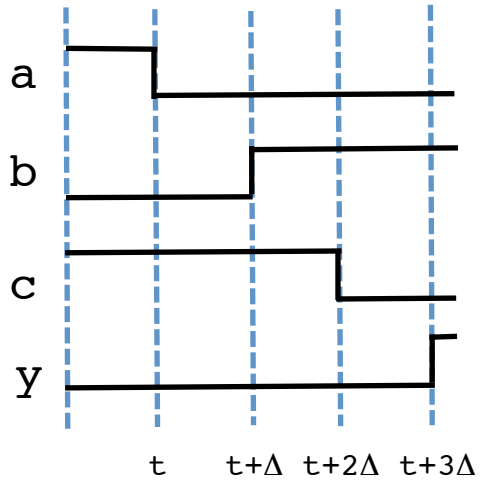

```
ARCHITECTURE beh OF buf
BEGIN
  b <= a AFTER 20 ns;
END beh;
```

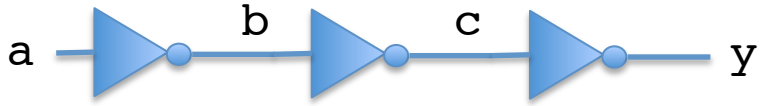


Transport vs. Inertial

Delta Delays Example

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.all;
ENTITY inv_chain is
  PORT(a : IN  STD_LOGIC;
       y : OUT STD_LOGIC);
END;
ARCHITECTURE conc OF inv_chain
SIGNAL  b,c: std_logic;
BEGIN
  y <= NOT c;
  c <= NOT b;
  b <= NOT a;
END conc;
```





GONZAGA UNIVERSITY

Delay Models: Summary

- Inertial
  - For devices with inertia (i.e. any physical device)
  - Pulses shorter than the modeled device's delay are not propagated
  - VHDL 1993 supports pulse rejection widths
- Transport
  - Ensures propagation of all events (any pulse, no matter how short, is propagated)
  - Typically used to model elements such as ideal wires
- Delta
  - Automatically inserted to ensure functional correctness of code that do not specify timing
  - Enforces the data dependencies specified in the code
  - This is the delay model to use for synthesizable code