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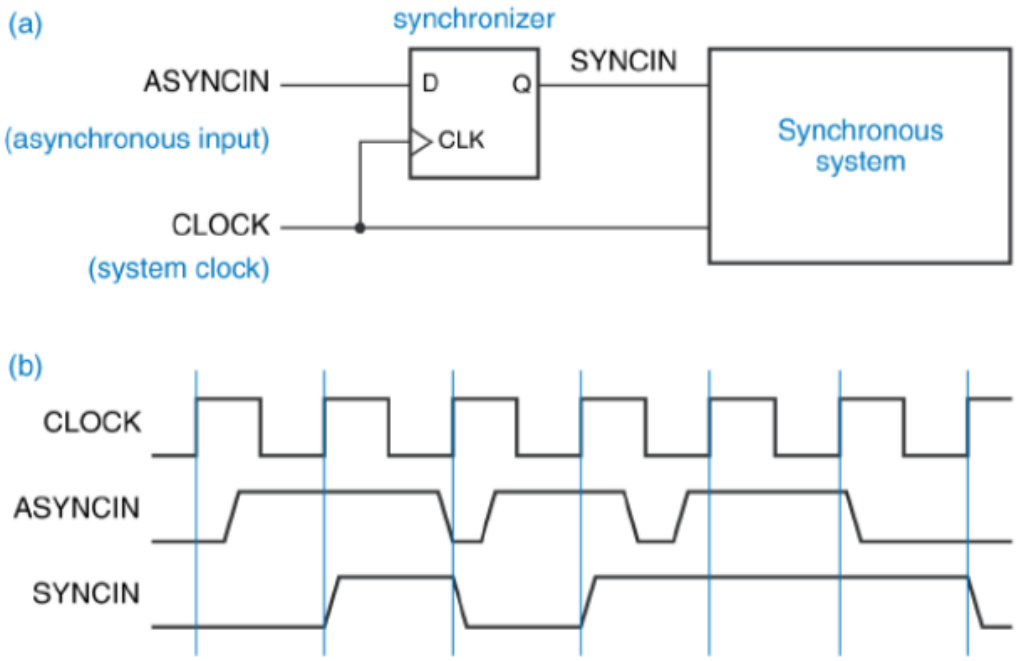
Metastability

Asynchronous Inputs

- Synchronous circuits can have asynchronous inputs
  - Even a supposedly synchronous circuit like the D flip flop can have asynchronous inputs such as preset and clear
  - In this case glitches makes asynchronous inputs extremely dangerous and should be avoided
- Sometimes asynchronous inputs come from signals that must pass from the outside world into the synchronous system
- In this case it is metastability to become an issue

Handling asynchronous inputs

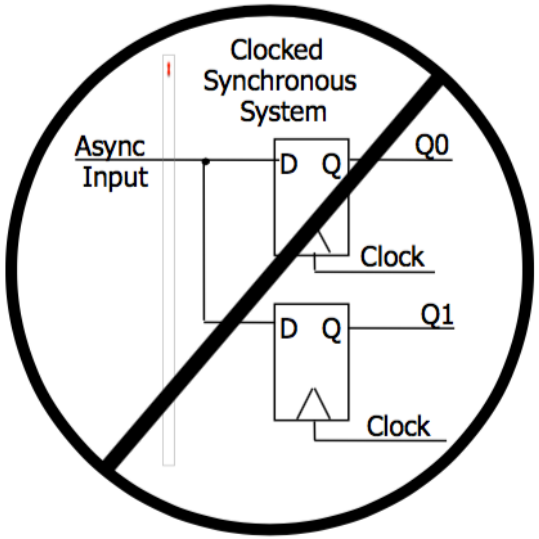
- The best way to deal with asynchronous signals is to synchronize them to the clocked system

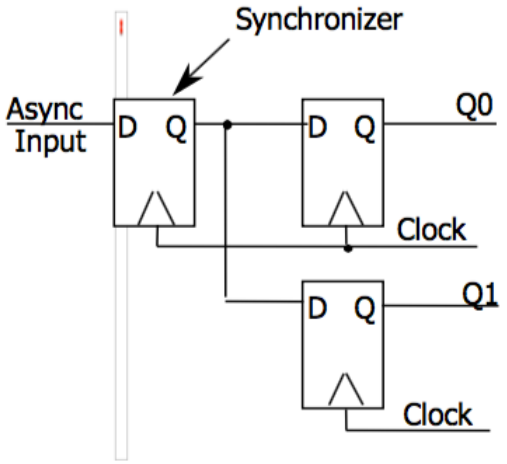


A single, simple synchronizer: (a) logic diagram; (b) timing.

Handling asynchronous inputs (cont'd)

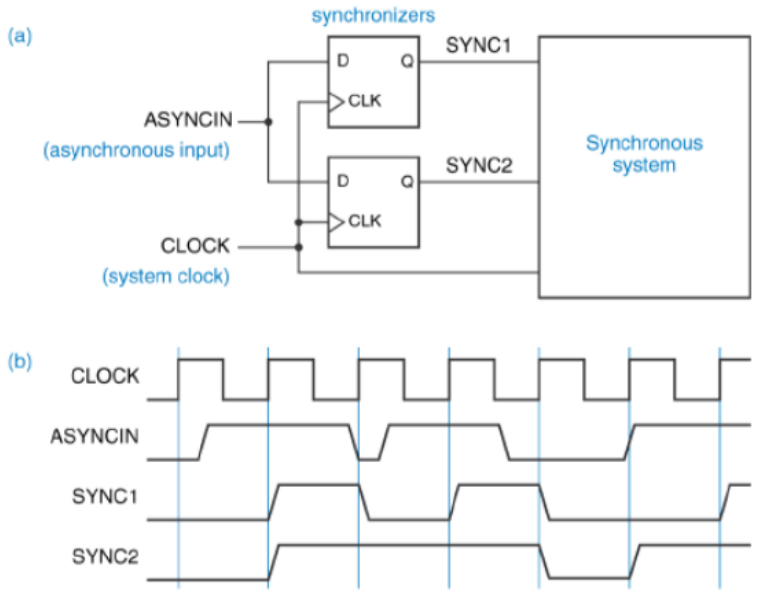
- It is essential for asynchronous inputs to be synchronized at only one place in a system and as soon as possible
  - Never allow asynchronous inputs to fan-out to more than one flip-flop
  - Synchronize as soon as possible and then treat as synchronous signal





Handling asynchronous inputs (cont'd)

- Possible problem occurring when synchronizing at more than one place



SYNC1 and SYNC2 were supposed to be the same

Two synchronizers for the same asynchronous input: (a) logic diagram; (b) possible timing.

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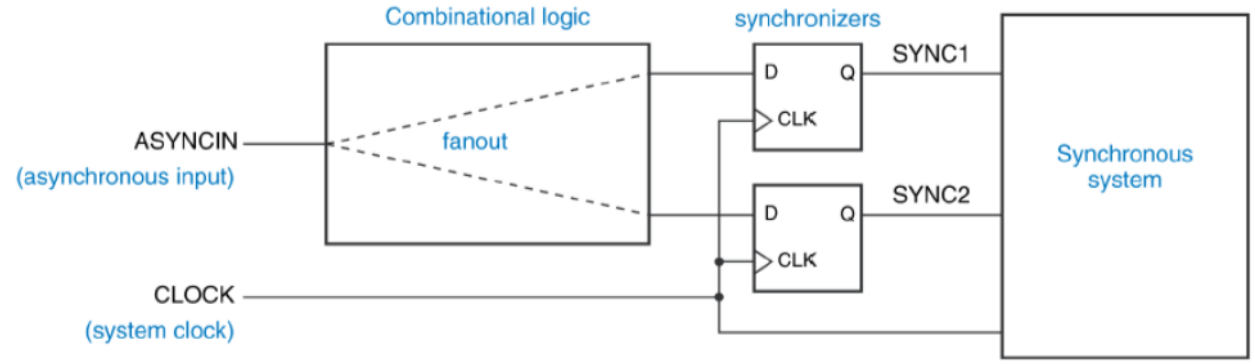
Handling asynchronous inputs (cont'd)

- Possible problem with procrastinating synchronization
- Example of combinational logic hiding the fact that there are two synchronizers. Since different paths through combinational logic will have different delays, the likelihood of an inconsistent result is even greater



An asynchronous input driving two synchronizers through combinational logic.

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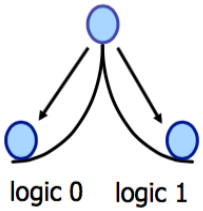
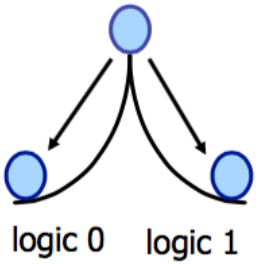
Synchronization Failure

- What if the asynchronous input to the synchronizer FF changes too close to clock edge
  - the FF may enter a metastable state – neither a logic 0 nor 1
  - it may stay in this state an indefinite amount of time (this is not likely in practice due to noise and other disturbances)

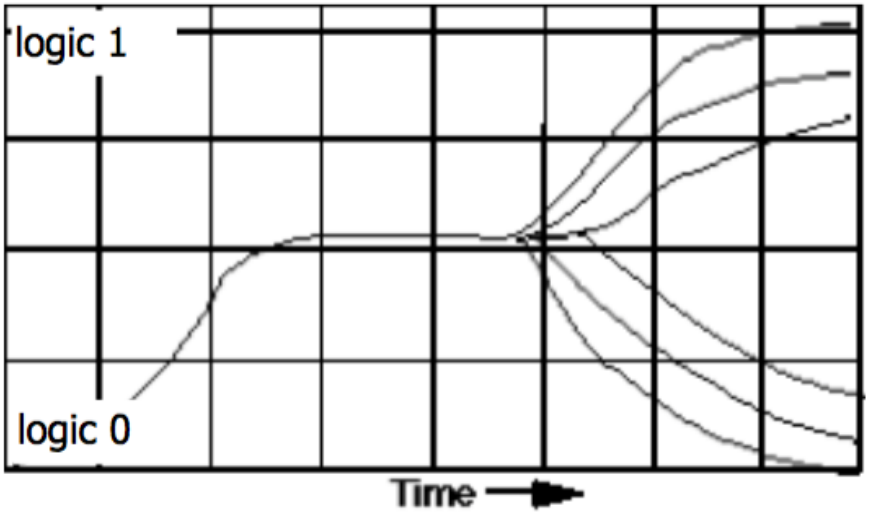


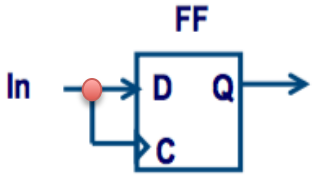
- **Synchronization failure** is said to occur if a system uses a synchronizer output while the output is still in metastable state.
- The only way to recover from synchronization failure is to reset the entire circuit
- While **the probability of synchronizer failure** can be made small, it **can never be eliminated** as long as there are asynchronous inputs

Synchronization Failure (cont'd)



small, but non-zero probability that the FF output will get stuck in an in-between state



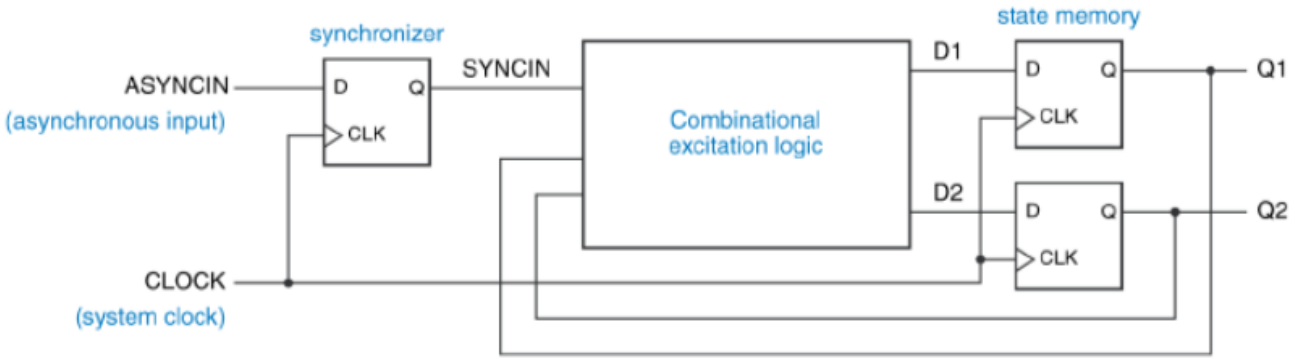


oscilloscope traces demonstrating synchronizer failure and eventual decay to steady state

- There are two ways to get a flip flop out the metastable state:
  - Force the flip flop into a valid logic state using input signals that meet the specifications for minimum pulse width, setup and hold time
  - Wait "long enough", so the flip flop comes out of metastability on its own

Metastability Resolution Time (tr)

- Maximum time that the output can remain metastable without causing synchronizer (and system) failure

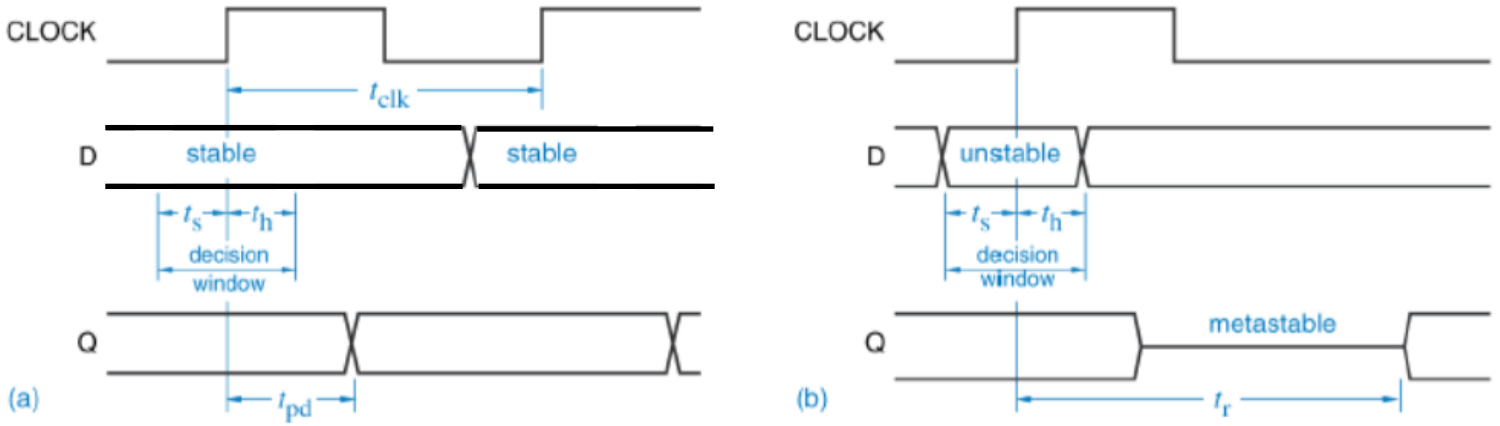


$$t_r = T_{clk} - t_{comb} - t_{su}$$

Reducing the chance of Synchronizer Failure

- One way to reduce the probability of synchronizer failure is to use faster flip flops and lengthen the system's clock period. This gives the synchronizer flip-flop more time to enter a stable state.
- A second strategy is to place two FFs in series. Both flip- flop must be metastable before the synchronization fails (an event with lower probability)

Analysis of Metastable timing



Timing parameters for metastability analysis: (a) normal flip-flop operation; (b) metastable behavior.

$$t_r = T_{clk} - t_{comb} - t_{su}$$

Analysis of Metastable timing

$$MTBF = \frac{e^{t_r/\tau_u}}{T_0 \cdot F_{clk} \cdot \alpha}$$

- MTBF = **M**ean **T**ime **B**etween **F**ailures

- t_r = resolution time
- F_{clk} = frequency of the flip-flop clock
- α = number of asynchronous input changes per second applied to the D input of the FF (asynchronous activity rate)
- T_0 = constants that depends on the electric characteristics of the FF
- τ_u = constants that depends on the electric characteristics of the FF

Example: Metastability in 5-V Logic Circuits

- Texas Instruments, *Metastable Response in 5-V logic Circuits*

$$MTBF = \frac{\exp\ (T \times t_x)}{f_{clk} \times f_{in} \times T_O}$$

To produce the worst case during a test, that is, the setup-and-hold timing conditions are violated as often as possible, the frequency (fin) of the input signal is, chosen to be one-half the clock frequency (fin = 0.5 fclk)

$$MTBF = \frac{\exp\ (T \times t_x)}{0.5 \times f_{clk}^2 \times T_O}$$

t_x = settling time
= resolution time
= time that the second flip-flop has for stabilization

$T = 1/\tau_u$

Table 1. Constants Describing the Metastable Behavior

Family	T (1/ns)	T_O (s)
Std-TTL	0.74	2.9×10^{-4}
LS	0.74	4.8×10^{-3}
S	0.36	1.3×10^{-9}
ALS	1.0	8.7×10^{-6}
AS	4.0	1.4×10^{3}
F	9.2	1.9×10^{8}
BCT	1.51	1.14×10^{-6}
ABT	3.61	33×10^{-3}
HC	0.55	1.46×10^{-6}
AC	2.8	1.1×10^{-4}

Example: Metastability in 5-V Logic Circuits (cont'd)

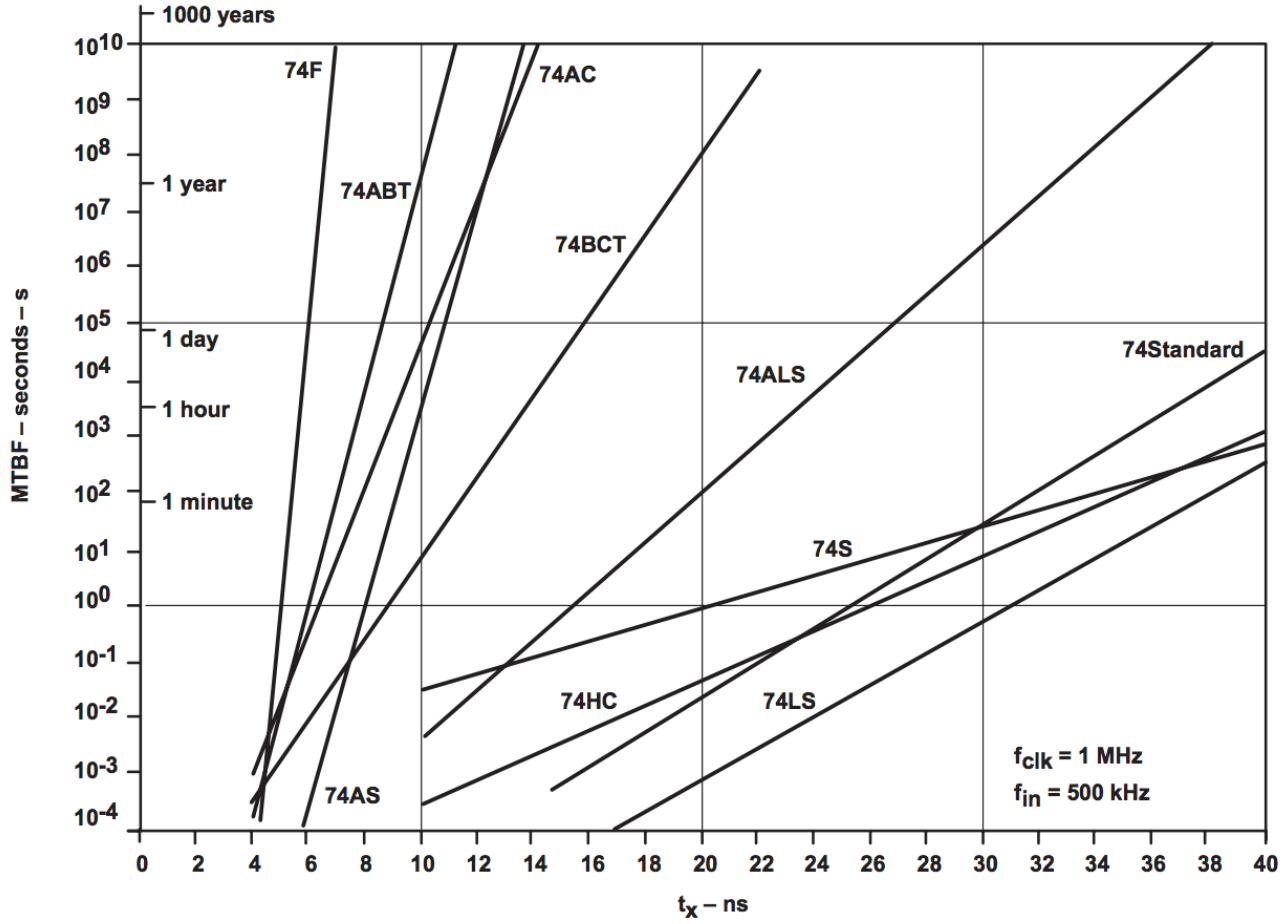
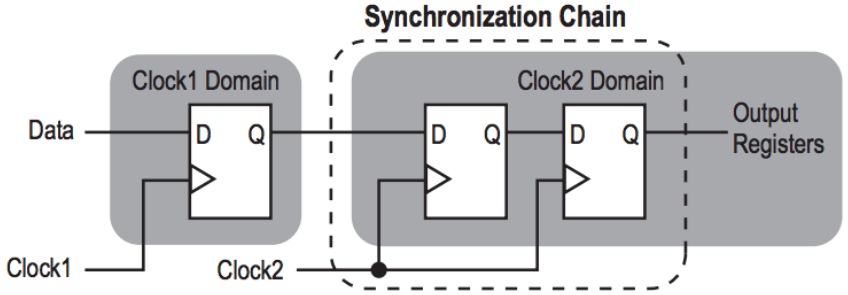


Figure 8. Metastable Characteristic of Logic Circuits

Example: Metastability in FPGAs

- ALTERA: *Understanding Metastability in FPGAs*

Figure 3. Sample Synchronization Register Chain



$$MTBF = \frac{e^{t_{MET}/C_2}}{C_1 \cdot f_{CLK} \cdot f_{DATA}}$$

$$failure\_rate_{design} = \frac{1}{MTBF_{design}} = \sum_{i=1}^{number\ of\ chains} \frac{1}{MTBF_i}$$

- The C_1 and C_2 constants depend on the device process and operating conditions
- The t_{MET} is the available metastability settling time, (timing slack available beyond the register's t_{CO}, for a potentially metastable signal to resolve to a known value).
- The f_{CLK} and f_{DATA} parameters depend on the design specifications:
  - f_{CLK} is the clock frequency of the clock domain receiving the asynchronous signal and
  - f_{DATA} is the toggling frequency of the asynchronous input data signal.
  - Faster clock frequencies and faster-toggling data reduce (that is worsen) the MTBF.

Metastability in Altera Devices

Figure 3. MTBF vs. t_{MET}

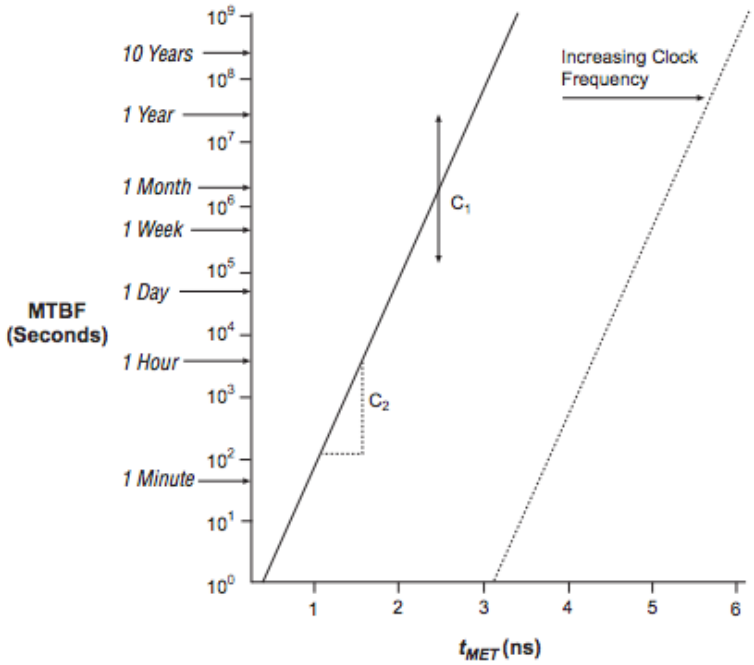


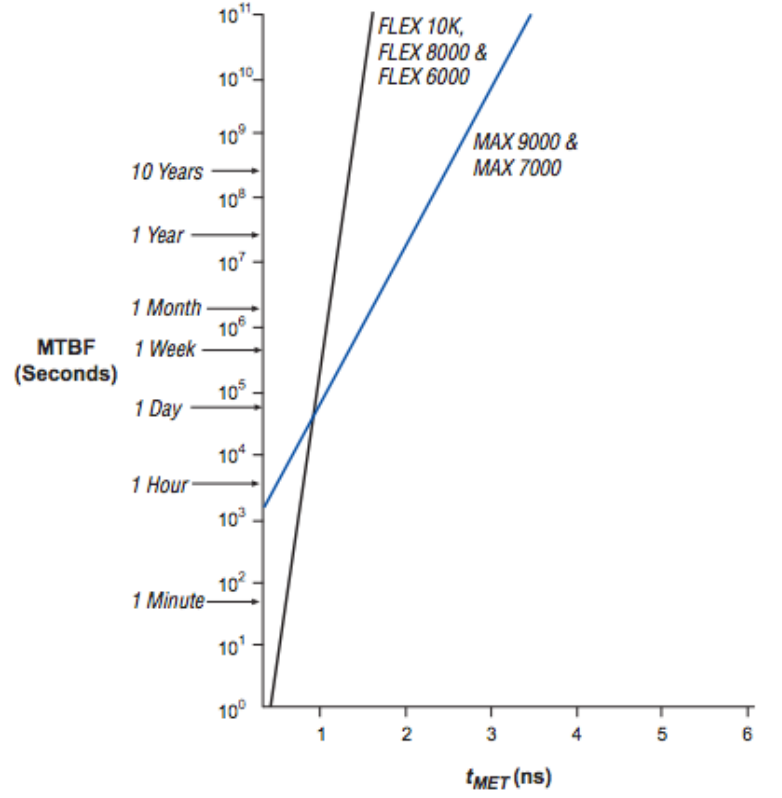
Table 1. Metastability Equation Constants

Device	C_1	C_2
FLEX 10K	1.01×10^{-13}	1.268×10^{10}
FLEX 8000	1.01×10^{-13}	1.268×10^{10}
FLEX 6000	1.01×10^{-13}	1.268×10^{10}
MAX 9000	2.98×10^{-17}	5.023×10^{9}
MAX 7000	2.98×10^{-17}	5.023×10^{9}

same process

same process

Figure 5. Metastability Characteristics of Altera Devices



Metastability in ALTERA Devices (cont'd)

Figure 6. FLEX 10K, FLEX 8000 & FLEX 6000 MTBF Values

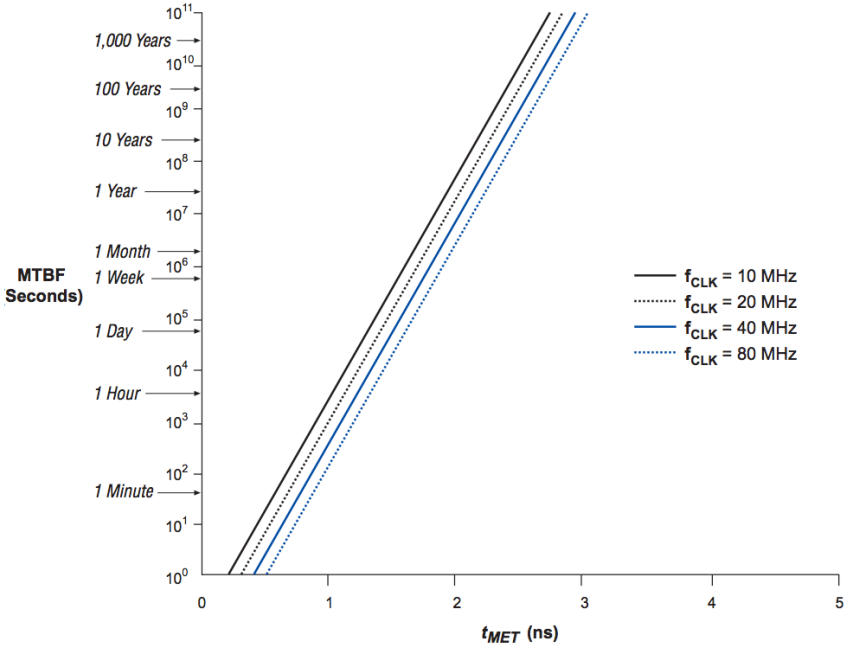
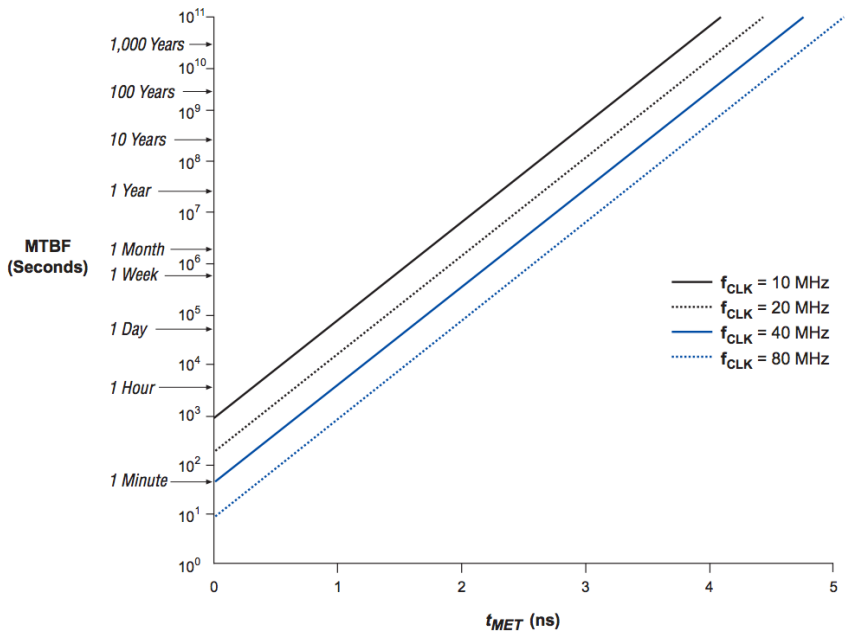
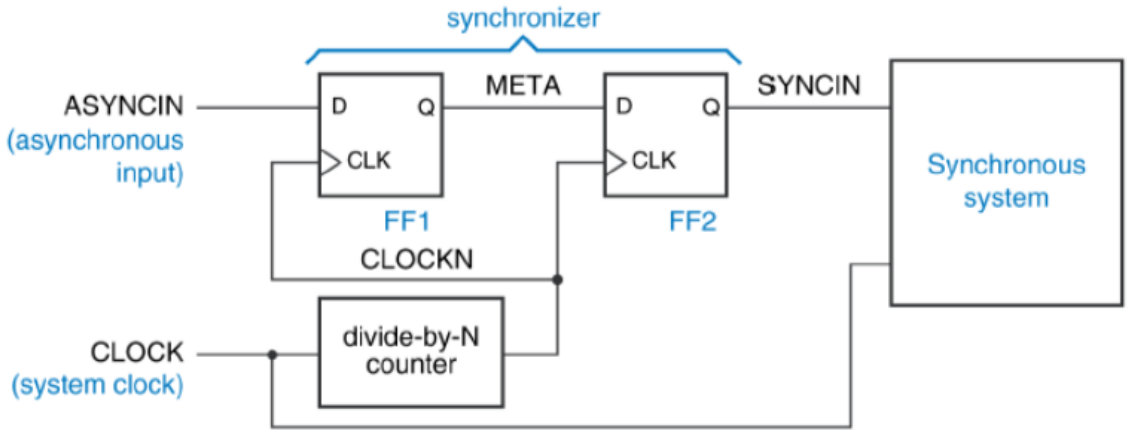


Figure 7. MAX 9000 & MAX 7000 MTBF Values



Better Synchronizers

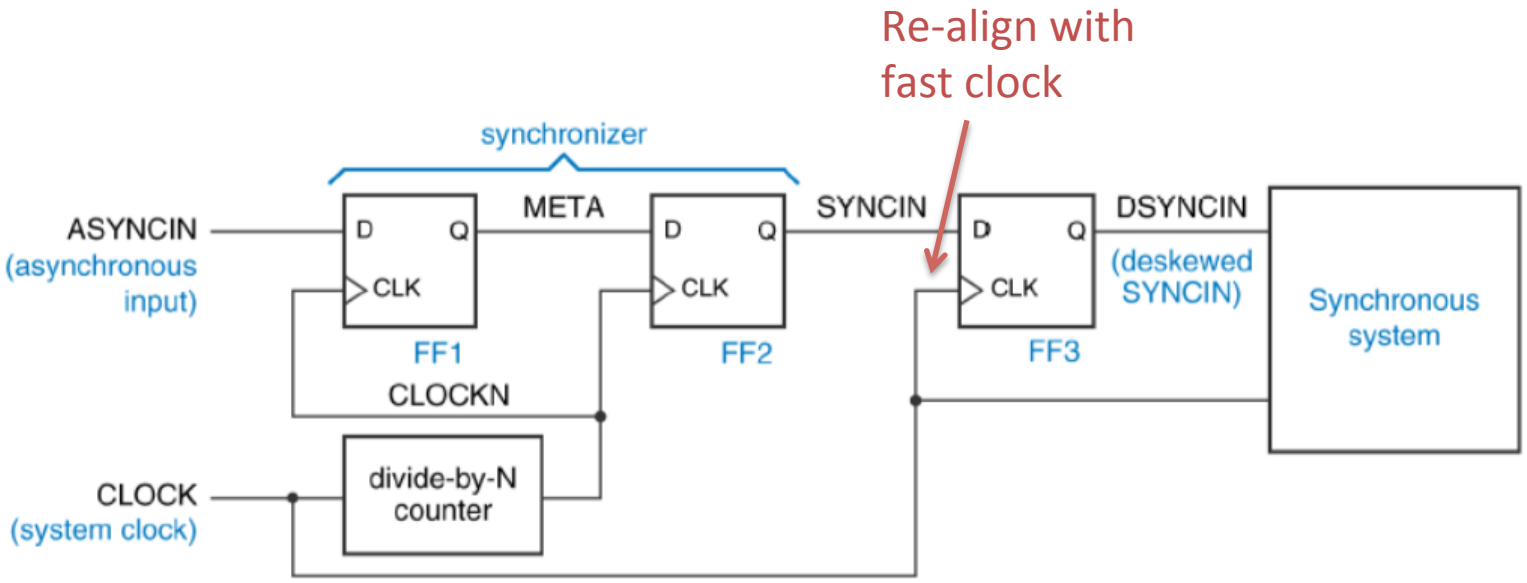
- A way to improve the MTBF is to lengthen the clock applied to the synchronizer circuit ($n \cdot T_{clk}$)



Multiple-cycle synchronizer.

CLOCKN is n times slower than CLOCK

Better Synchronizers (cont'd)

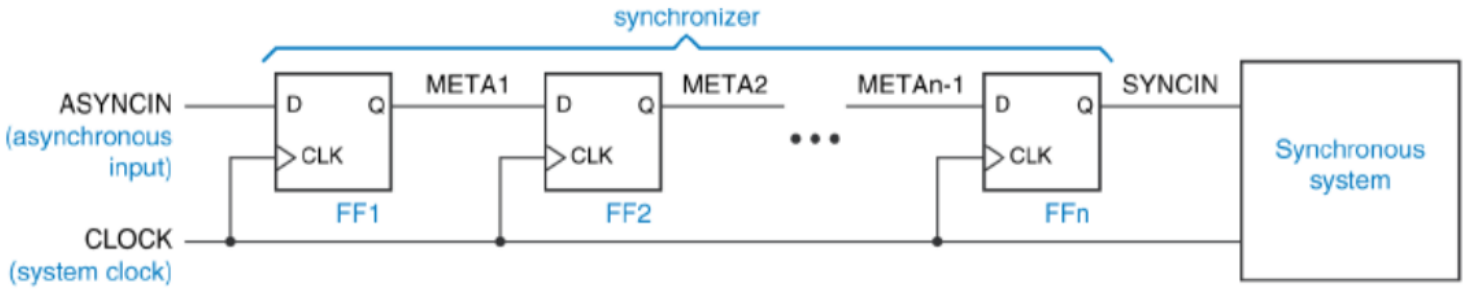


Multiple-cycle synchronizer with deskewing.

CLOCKN is n times slower than CLOCK

Better Synchronizers (cont'd)

- At very high frequency, the feasibility of the multi-cycle synchronizers is limited by the clock skew



Cascaded synchronizer.

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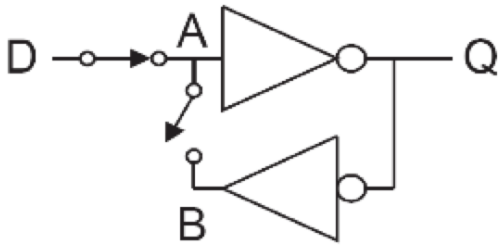
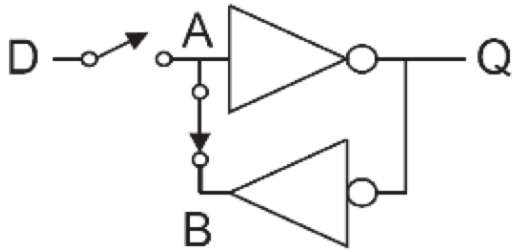
Understanding Metastability

- a



Latch in Transparent Mode



Latch in Opaque Mode

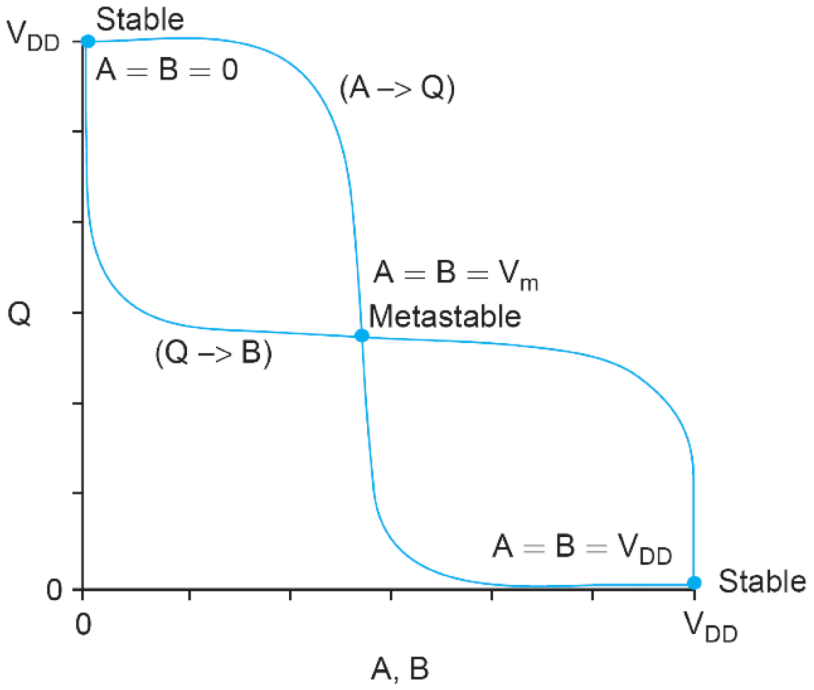
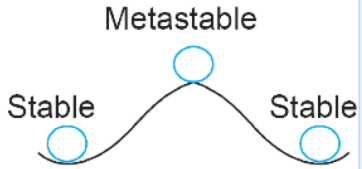


FIGURE 10.42 Metastable state in static latch



Understanding Metastability (cont'd)

- Assume the initial voltage at node A when the latch become opaque (at t=0) is:

$$V_A(0) = V_m + v(0)$$

Small signal offset from the metastable point

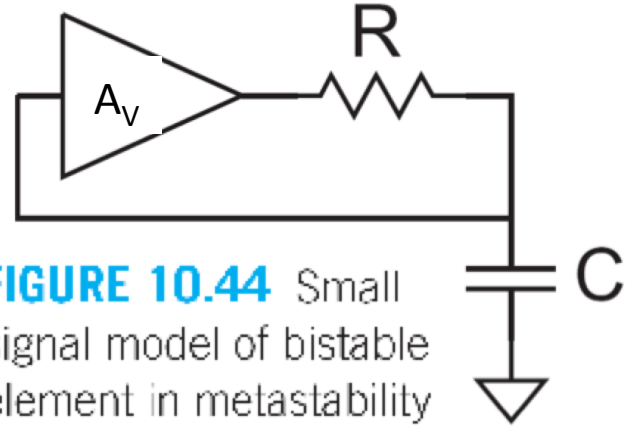


FIGURE 10.44 Small signal model of bistable element in metastability

- Small signal behavior after time t=0 is given by:

$$\frac{A_V v(t) - v(t)}{R} = C\frac{dv(t)}{dt} \Leftrightarrow \frac{A_V - 1}{RC}dt = \frac{dv}{v} \Leftrightarrow \frac{A_V}{RC}dt \cong \frac{dv}{v} \Leftrightarrow$$

$$\underbrace{GBW}_{\omega_U} \cdot \int_0^t dt = \int_{v(0)}^{v(t)} \frac{dv}{v} \Leftrightarrow \frac{t}{\tau_u} = \ln\left[\frac{v(t)}{v(0)}\right] \Leftrightarrow v(t) = v(0)\cdot\exp\left(\frac{t}{\tau_u}\right)$$

Understanding Metastability (cont'd)

$$v(t) = v(0) \cdot \exp\left(\frac{t}{\tau_u}\right)$$

The node A is defined to reach a legal logic level when |v(t)| exceed some deviation ΔV. The time to reach this level is:

$$t_{D-Q} = \tau_u \cdot \left(\ln \Delta V - \ln v(0)\right)$$

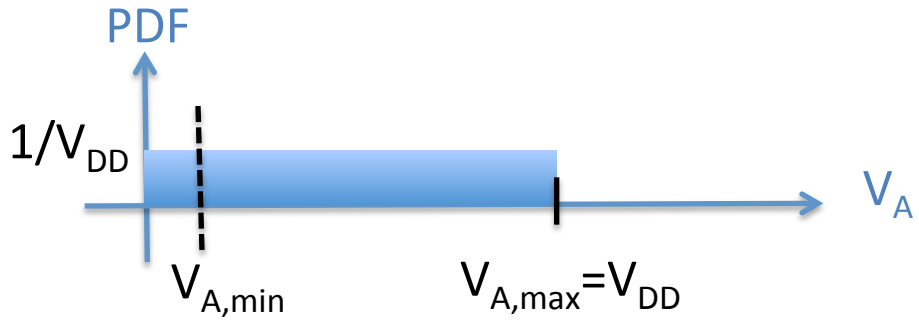
If v(0) approaches 0 (that is $V_A(0)$ approaches the metastable point), the delay approaches infinity (at least theoretically: in practice this can never happen because of noise).

There is an upper to the time we can wait for the signal to become valid ($t_R = T_{clk} - t_{setup}$). This time is usually called resolution time or settling time.

Understanding Metastability (cont'd)

- Designers need to know what is the probability that the latch propagation delay exceed the resolution time (that is what is the probability of error when the input changes during the aperture window):

$$P(error) = P(t_{DQ} > t_r) = P(V_A(0) < V_{A,\min}) = \frac{V_{A,\min}}{V_{A,\max}}$$



Understanding Metastability (cont'd)

- Since we need to reach an adequate voltage level for a transition between logic levels to be successful we must wait for the amplifier to respond "completely" before declaring its latching operation complete:

$$V_A(0)\cdot\exp\left(\frac{t_r}{\tau_u}\right)=V_{DD}\Leftrightarrow V_A(0)=\frac{V_{DD}}{\exp\left(\frac{t_r}{\tau_u}\right)}$$

- Assuming the data signal $V_A(t)$ is a ramp with rise time $T_{10\text{-}90}$ in order to go from $V_A(0)$ to V_{DD} it takes:

$$T_W=\frac{V_A(0)}{V_{DD}}\cdot T_{10-90}=T_{10-90}\cdot\exp\left(-\frac{t_r}{\tau_u}\right)$$

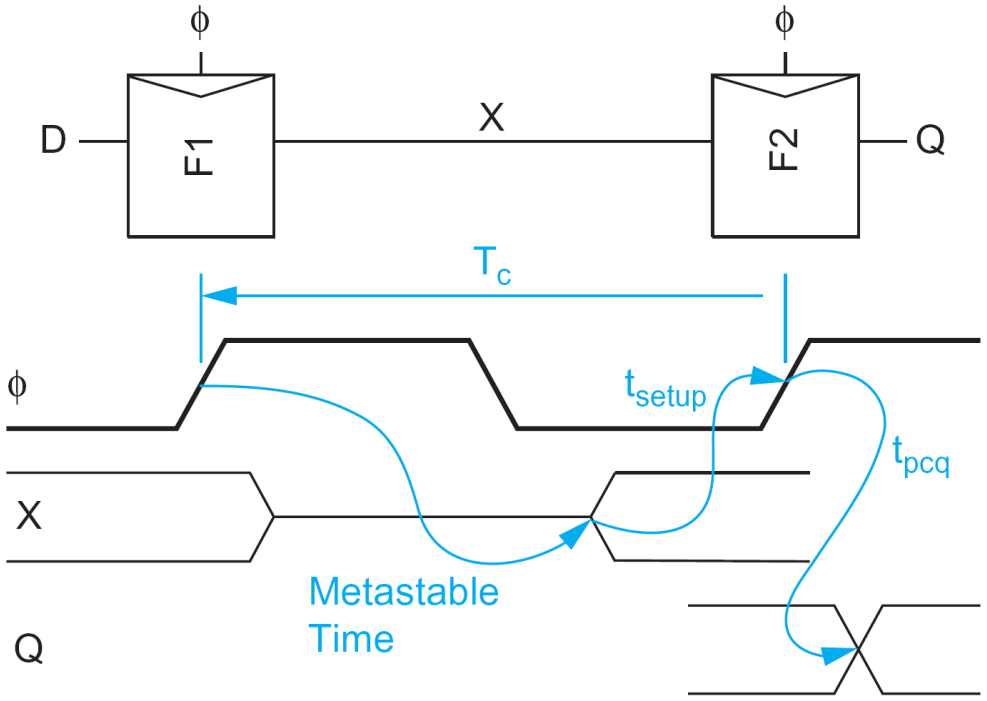
Understanding Metastability (cont'd)

- The probability of hitting within T_W, out of the total clock cycle T_{clk} is the P(error)

$$P(error) = \frac{T_W}{T_{clk}} = \frac{T_{10-90}}{T_{clk}} \cdot \exp\left(-\frac{t_r}{\tau_u}\right)$$

$$T_O \equiv T_{10-90} = rise\,time\,of\,inverter \cong 2.2 \cdot RC$$

Simple Synchronizer Revisited



$$t_r = T_{clk} - T_{setup}$$

$$MTBF = \frac{1}{P(error)\cdot\alpha} = \frac{e^{t_r/\tau_u}}{T_0 \cdot F_{clk} \cdot \alpha}$$