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Synthesis: Design Objects

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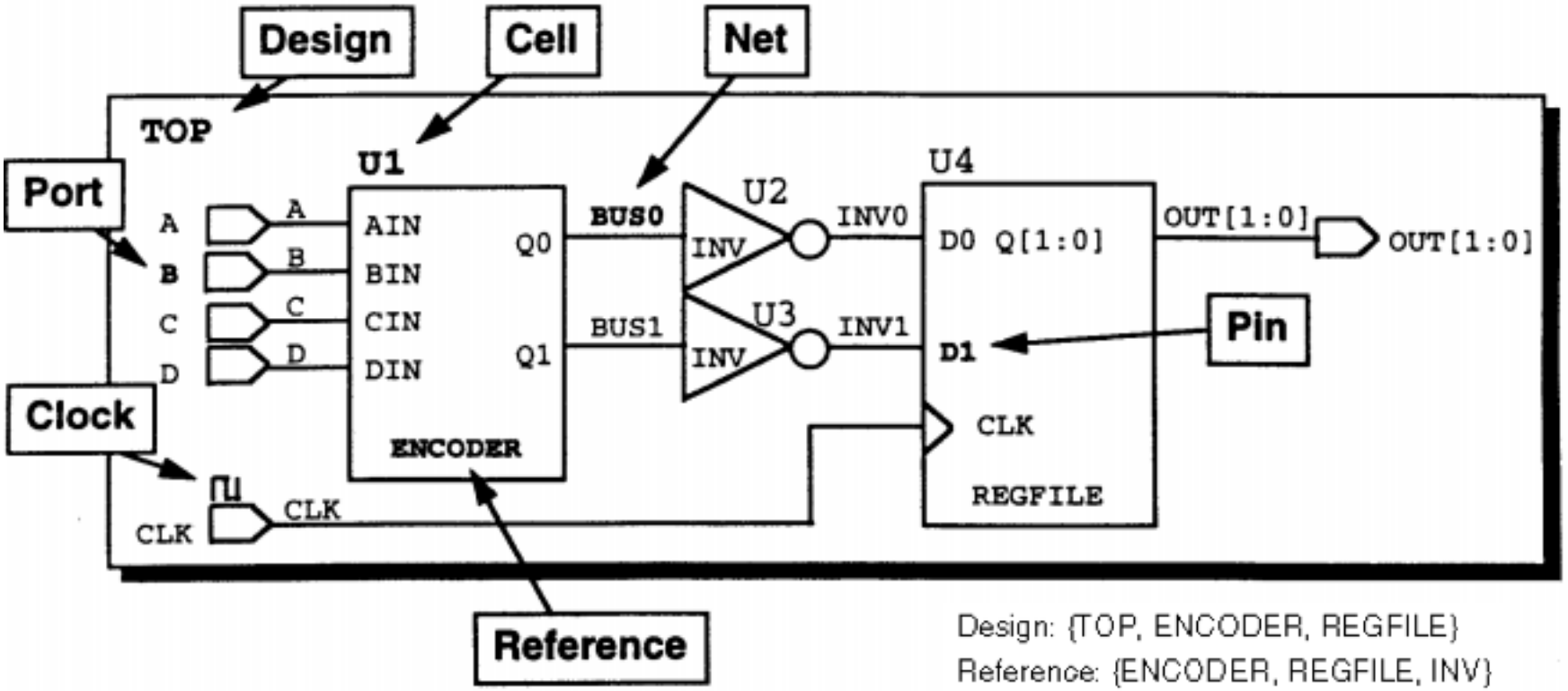
Design Objects

A design consists of instances (a.k.a. cells), nets, ports, and pins and it can contain sub-designs and library cells



Design: {TOP, ENCODER, REGFILE}
Reference: {ENCODER, REGFILE, INV}
Instance: {U1, U2, U3, U4}

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Design Objects

Design: A circuit description that performs one or more logical functions.

Cell: An instantiation of a design within another design (aka *instance*).

Reference: The original design that a cell "points to" (uses as a basis).

Port: The input or output of a design.

Pin: The input or output of a cell.

Net: The wire that connects ports to pins and/or pins to each other.

Clock: Port or pin of a design explicitly identified as a clock source.

Collection of Objects

Table. SDC Collection Commands

Command	Description of the collection returned
`all_clocks`	All clocks in the design.
`all_inputs`	All input ports in the design.
`all_outputs`	All output ports in the design.
`all_registers`	All registers in the design.
`get_cells`	Cells in the design. All cell names in the collection match the specified pattern. Wildcards can be used to select multiple cells at the same time.
`get_clocks`	Clocks in the design. When used as an argument to another command, such as the `-from` or `-to` of `set_multicycle_path`, each node in the clock represents all nodes clocked by the clocks in the collection. The default uses the specific node (even if it is a clock) as the target of a command.
`get_nets`	Nets in the design. All net names in the collection match the specified pattern. You can use wildcards to select multiple nets at the same time.
`get_pins`	Pins in the design. All pin names in the collection match the specified pattern. You can use wildcards to select multiple pins at the same time.
`get_ports`	Ports (design inputs and outputs) in the design.