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Synthesis Process

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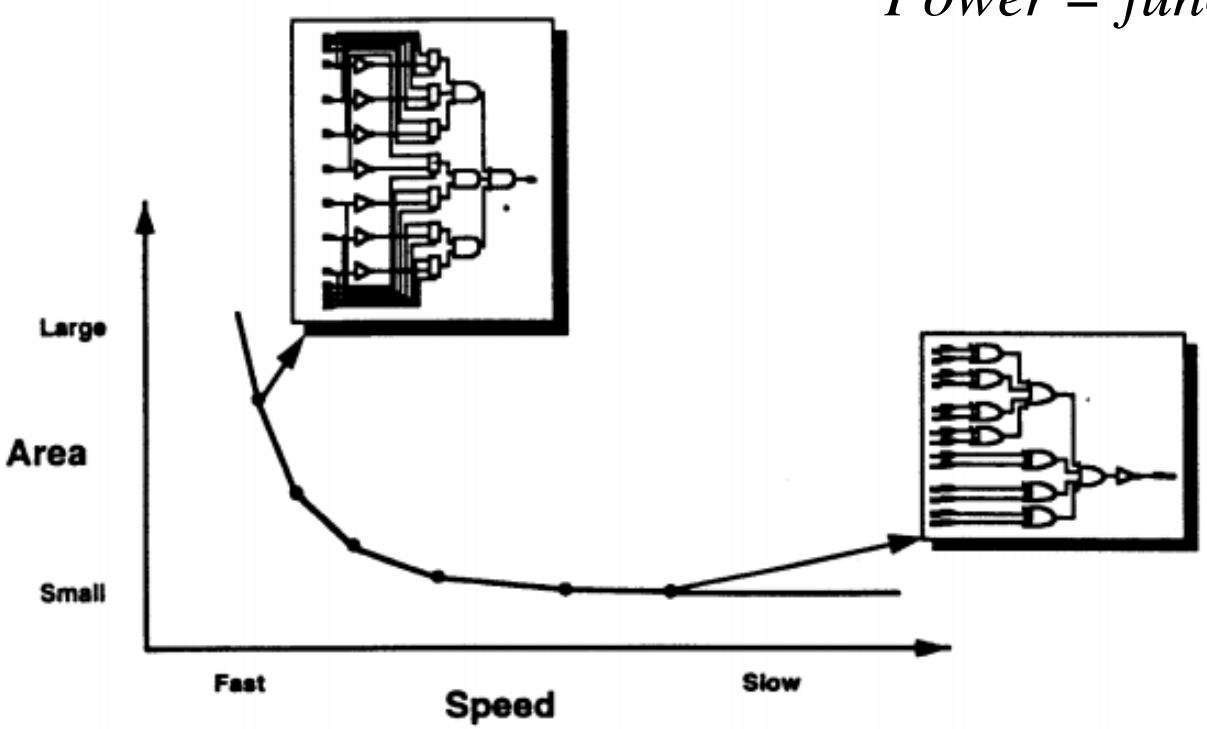
Synthesis Process

- Synthesis is:
  - Constraint-Driven
  - Path-Driven

Synthesis is Constraint-Driven

$$Power = function(Area, Speed)$$



Designer explores tradeoffs varying constraints

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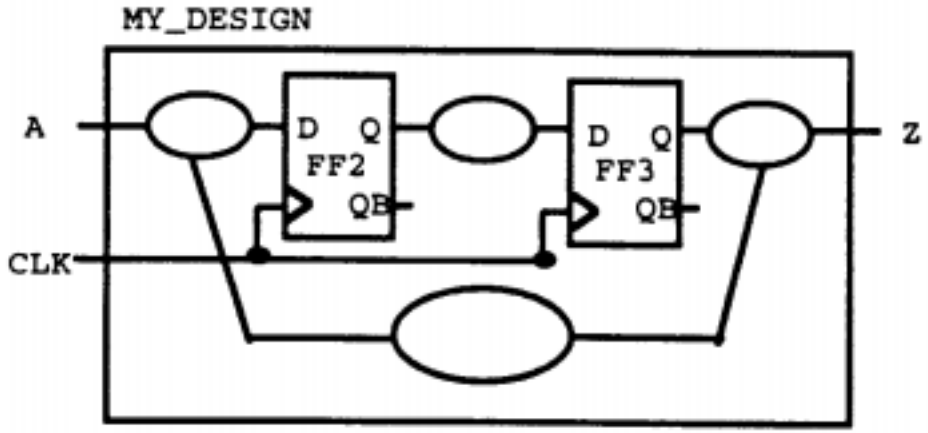
Synthesis is Path-Driven



- Synthesis parses a design into a bunch of paths
- The paths are sorted by which clock captures the path's data

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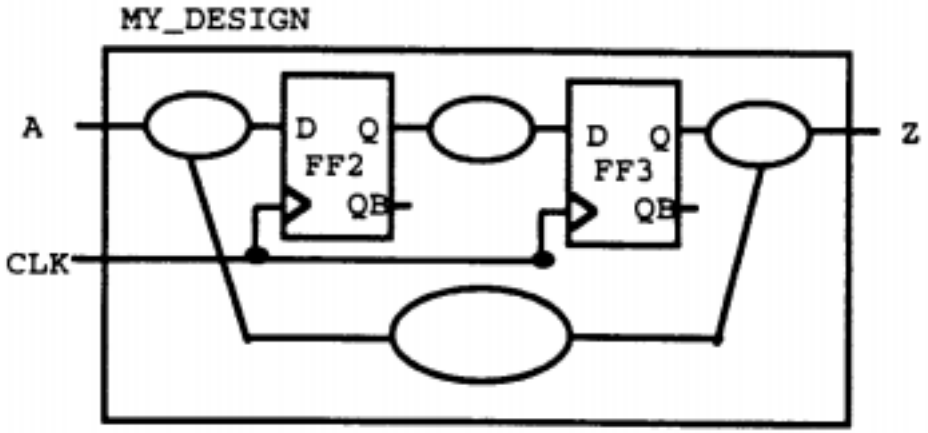
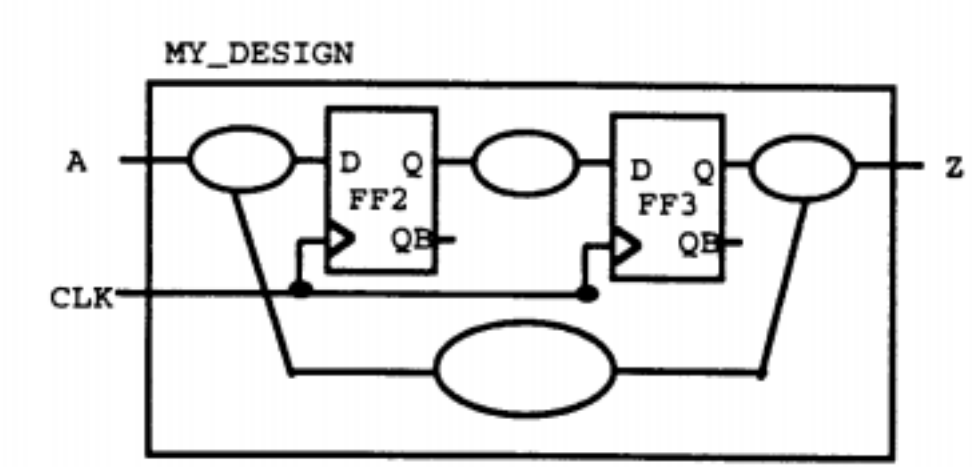
Synthesis is Path-Driven



Paths:

- inputs to data pin registers
- inputs to outputs
- clocks to data pin registers
- clocks to outputs

Synthesis is Path-Driven



Start points:

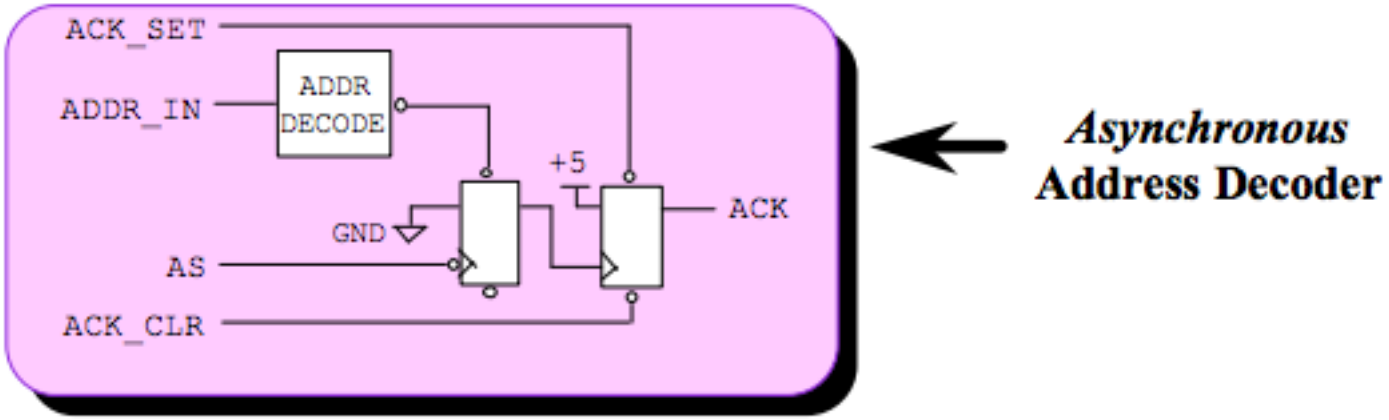
- Inputs
- Clocks

End points:

- Outputs
- Data pin of registers

Think Synchronous Hardware !!

- Synchronous designs run smoothly through synthesis, test, simulation and layout
- Asynchronous designs require hand instantiation and simulation to verify.
  - Isolate necessary asynchronous logic and put into separate blocks



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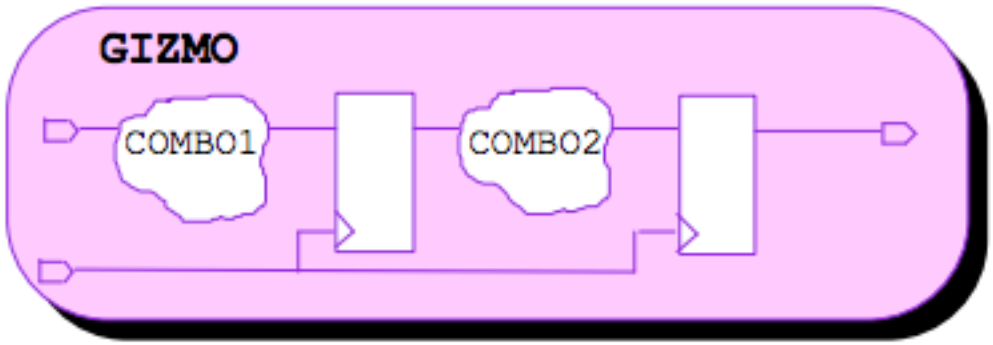
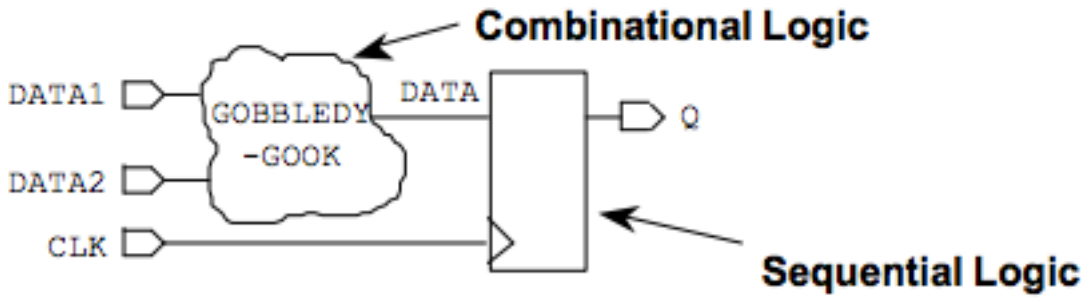
Think RTL !!

- Describe the circuit in terms of their register-to-register functionality (i.e., describe the circuit in terms of its registers and the combinational logic between registers)



RTL Coding Guidelines

- Separate combinational logic and sequential logic
  - code combinational logic and sequential logic into separate processes



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Chip Specification

- Begin with:
  - Operating frequency
  - Operating conditions / environment
  - Functionality
  - I/Os
  - Test Requirements
  - …

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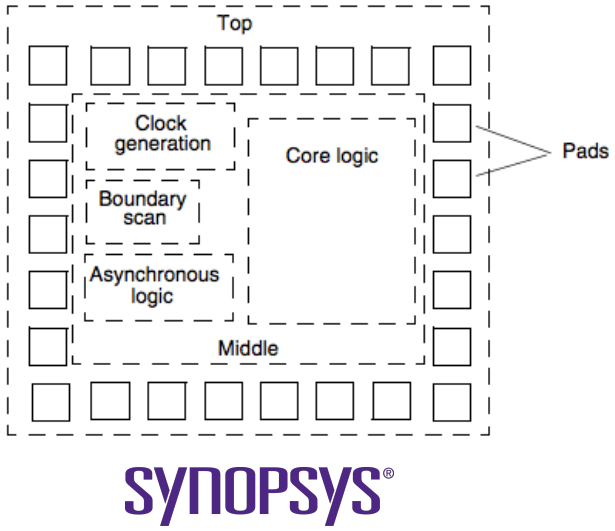
Chip Synthesis – Tasks List

- **Chip Specification**
- **Draw Block Diagram / Partition Chip**
- **Code Each Block** -> Simulate -> Fix Problems -> Recode
- **Chip Level Model** -> Simulate -> Fix Problems -> Recode
- **Synthesize Blocks** -> Meet Constraints? -> Recode -> Re-synthesize
- **Check Each Block For Testability** -> Fix Problems -> Recode -> Re-synthesize
- **Integrate Blocks to Build Chip Hierarchy** -> Check Timing -> Re-optimize
- **Check Chip For Testability** -> Fix Problems -> Recode -> Re-synthesize
- **Insert Test Structures (Internal Scan and JTAG)** -> Check -> Re-optimize
- **Insert I/O Pads** -> Check Timing -> Re-optimize
- **Floorplan Chip** -> Back Annotate -> Check Constraints -> Re-optimize
- **Place and Route (Layout) Chip** - Back Annotate -> Check -> Re-optimize
- **Run ATPG** -> Fault Coverage
- **Perform Final Verification** -> Timing / Simulation



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