

Synthesis Design Constraints and Timing Reports

Example - timing.vhd

```
--
-- author:   Claudio Talarico
-- file:     timing.vhd
-- comment:  example to learn how to read
--           timing reports
--
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity timing is
port (
    clk      : in std_logic;
    sin      : in std_logic_vector(1 downto 0);
    sout     : out std_logic
);
end timing ;

architecture rtl of timing is
    signal regi    : std_logic;
    signal rego    : std_logic;
    signal regi_d  : std_logic;
    signal rego_d  : std_logic;
begin

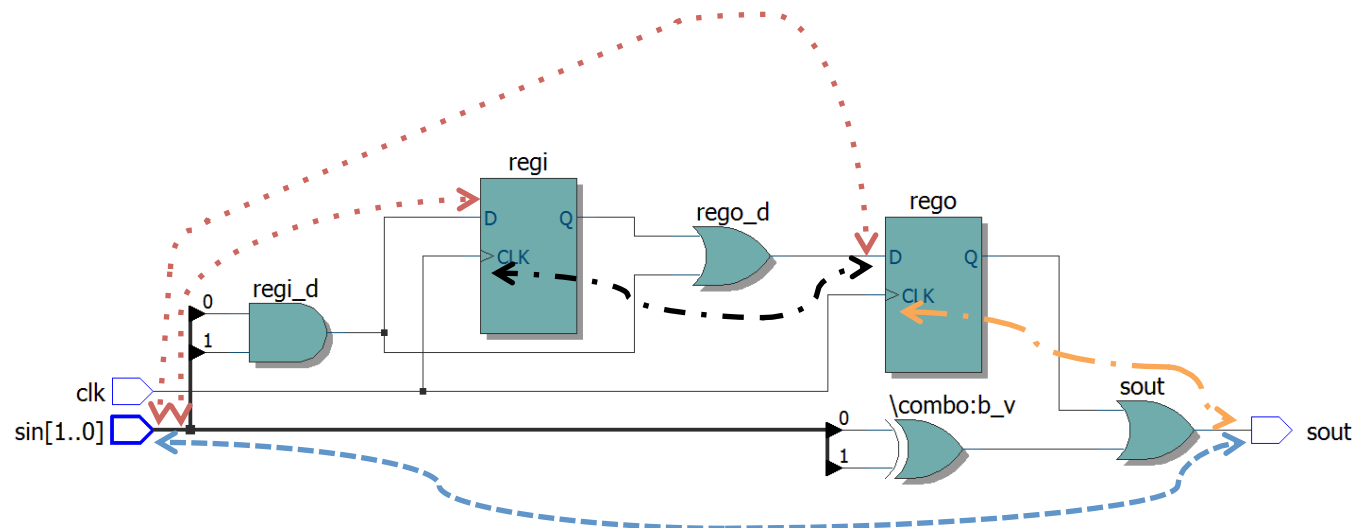
    combo: process(sin,regi,rego)
        variable a_v : std_logic;
        variable b_v : std_logic;
    begin
        a_v := sin(1) and sin(0);
        b_v := sin(1) xor sin(0);
        regi_d <= a_v;
        rego_d <= regi or a_v;
        sout   <= rego or b_v;
    end process combo;

    regs: process(clk)
    begin
        if (clk='1' and clk'event) then
            regi<= regi_d;
            rego<= rego_d;
        end if;
    end process regs;

end rtl;
```

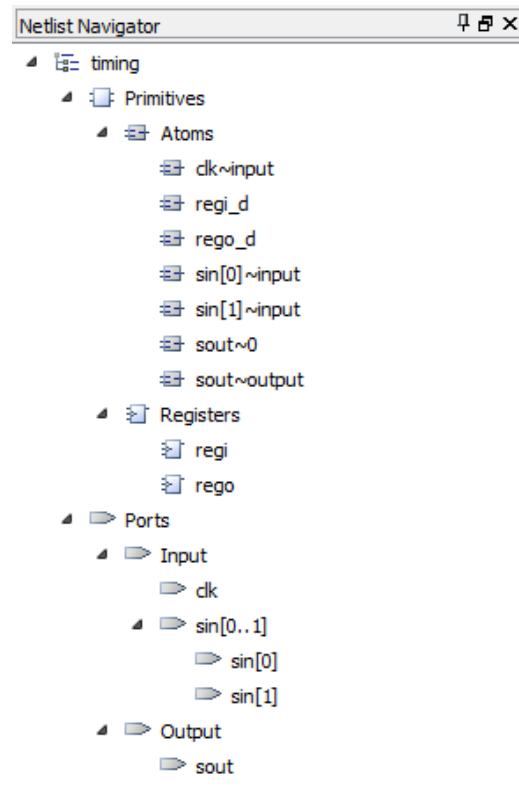
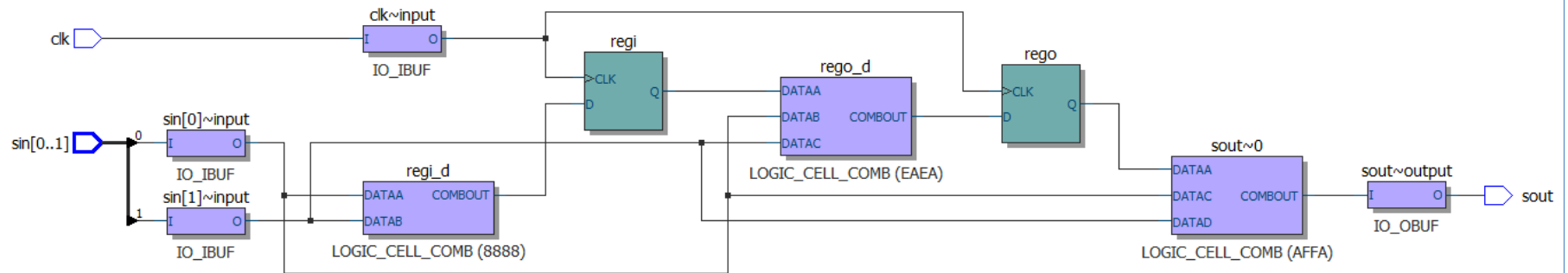
RTL view

- ▲ timing
 - ▲ Primitives
 - ▲ Logics
 - \combo:b_v
 - regi_d
 - rego_d
 - sout
 - ▲ Registers
 - regi
 - rego
 - ▲ Ports
 - ▲ Input
 - clk
 - sin[1..0]
 - ▲ Output
 - sout



- < · · · > INREG paths
- < - - - > INOUT paths
- < · · > CLK paths
- < · · > REGOUT paths

Mapping



timing.sdc and timing.tcl

- Add synopsys design constraints (sdc) file to the project
 - Assignments > Settings
 - TimeQuest Timing Analyzer > timing.sdc
- Add TCL script for customizing reports
 - Assignments > Settings
 - TimeQuest Timing Analyzer > timing.tcl

timing.sdc

```
## SDC file: "timing.sdc"

# Make sure to start "clean" (remove all assignments in memory)
reset_design

# Specify time units
set_time_format -unit ns -decimal_places 3

# Specify the clock period and other common parameters
set period 20.000
set input_del_max 4.000
set input_del_min 3.000
set output_del_max 3.000
set output_del_min 2.000

# Design Constraints File Organization:
# 1. Clock Constraints
# 2. Derived Constraints
# 3. Input and Output Delays
# 4. Timing Exceptions
# 5. Reports (optional)

#####
# 1. Clock Constraints

# Create Clock
create_clock -name "clock" -period $period -waveform {0 10} [get_ports clk]

# Set Clock Groups

# Set Clock Latency
set_clock_latency -source 0.02 [get_clocks clock]

# Set Clock Uncertainty
# set_clock_uncertainty 0.04 -to [get_clocks clock] -setup
# set_clock_uncertainty 0.04 -to [get_clocks clock] -hold

#####
# 2. Derived Constraints

# Create Generated Clock
# automatically apply a generate clock on the output of phase-locked loops (PLLs)
# this command can be safely left in the SDC even if no PLLs exist in the design
derive_pll_clocks

# Derived Uncertainty (using more pessimistic set_clock_uncertainty)
derive_clock_uncertainty

#####

#####
# 3. Input and Output Delays

# Set Input Delay
set_input_delay -clock "clock" -max $input_del_max [remove_from_collection [all_inputs] [get_ports {clk}]]
set_input_delay -clock "clock" -min $input_del_min [remove_from_collection [all_inputs] [get_ports {clk}]]
set_input_delay -clock "clock" 0 [get_ports {clk}]

# Set Output Delay
set_output_delay -clock "clock" -max $output_del_max [all_outputs]
set_output_delay -clock "clock" -min $output_del_min [all_outputs]

#####

#####
# 4. Timing Exceptions:

# Set False Path

# Set Multicycle Path

# Set Maximum Delay

# Set Minimum Delay
```

timing.tcl

```
# timing.tcl

# Check that the right project is open
if {[is_project_open]} {
    if {[string compare $quartus(project) "timingPrj"]} {
        puts "Project timingPrj is not open"
    }
} else {
    # Only open if not already open
    if {[project_exists timingPrj]} {
        project_open -revision top timing
    } else {
        project_new -revision top timing
    }
}

# define name for the reports
set chk_name "diagnostic.rpt"
set rpt_name "timing.rpt"

# Worst case operating condition
set_operating_conditions 7_slow_1200mv_85c
read_sdc
update_timing_netlist

# diagnostic test
report_clocks -file $chk_name
report_clock_transfers -file $chk_name -append
report_ucp -file $chk_name -append
report_sdc -file $chk_name -append
report_sdc -ignored -append -file $chk_name

# Timing (worst case operating condition)
report_timing -false_path -setup -npaths 0 -detail full_path -panel_name {Report False Path} -file $rpt_name
report_exceptions -setup -npaths 0 -detail full_path -panel_name {Report Exceptions} -file $rpt_name -append
report_path -npaths 0 -panel_name {Report Path} -file $rpt_name -append
report_timing -from_clock { clock } -setup -npaths 2 -detail full_path -panel_name {Report Timing} -file $rpt_name -append

# Best case operating condition
set_operating_conditions MIN_fast_1200mv_0c
read_sdc
update_timing_netlist

# Timing (best case operating condition)
report_timing -false_path -hold -npaths 0 -detail full_path -panel_name {Report False Path} -file $rpt_name -append
report_exceptions -hold -npaths 0 -detail full_path -panel_name {Report Exceptions} -file $rpt_name -append
report_path -npaths 0 -panel_name {Report Path} -file $rpt_name -append
report_timing -from_clock { clock } -hold -npaths 2 -detail full_path -panel_name {Report Timing} -file $rpt_name -append
```

diagnostics.rpt (1)

```

+-----+
; Unconstrained Paths ;
+-----+
+-----+
; Unconstrained Paths Summary ;
+-----+
; Property ; Setup ; Hold ;
+-----+
; Illegal Clocks ; 0 ; 0 ;
; Unconstrained Clocks ; 0 ; 0 ;
; Unconstrained Input Ports ; 0 ; 0 ;
; Unconstrained Input Port Paths ; 0 ; 0 ;
; Unconstrained Output Ports ; 0 ; 0 ;
; Unconstrained Output Port Paths ; 0 ; 0 ;
+-----+

```

```

+-----+
; Create Clock ;
+-----+
; SDC Command ; Name ; Period ; Waveform ; Targets ; Add Clock ; Location ; Comments ;
+-----+
; create_clock ; clock ; 20.000 ; { 0.000 10.000 } ; [get_ports {clk}] ; ; timing.sdc:27 ; ;
+-----+

```

```

+-----+
; Set Clock Uncertainty ;
+-----+
; SDC Command ; Flags ; From Flags ; From ; To Flags ; To ; Uncertainty ; Source ; Comments ;
+-----+
; set_clock_uncertainty ; ; -rise_from ; [get_clocks {clock}] ; -rise_to ; [get_clocks {clock}] ; 0.020 ; Generated ; ;
; set_clock_uncertainty ; ; -rise_from ; [get_clocks {clock}] ; -fall_to ; [get_clocks {clock}] ; 0.020 ; Generated ; ;
; set_clock_uncertainty ; ; -fall_from ; [get_clocks {clock}] ; -rise_to ; [get_clocks {clock}] ; 0.020 ; Generated ; ;
; set_clock_uncertainty ; ; -fall_from ; [get_clocks {clock}] ; -fall_to ; [get_clocks {clock}] ; 0.020 ; Generated ; ;
+-----+

```


diagnostics.rpt (2)

```

-----+
; Set Input Delay
-----+
; SDC Command ; Add Delay ; Source Latency Included ; Clock Fall ; Flags ; Clock Name ; Reference Pin ; Delay ; Ports ; Location ; Comments ;
-----+
; set_input_delay ; -add_delay ; ; ; ; [get_clocks clock] ; ; 0.000 ; [get_ports clk] ; timing.sdc:59 ; ;
; set_input_delay ; -add_delay ; ; ; ; -max ; [get_clocks clock] ; ; 4.000 ; [get_ports sin[0]] ; timing.sdc:58 ; ;
; set_input_delay ; -add_delay ; ; ; ; -min ; [get_clocks clock] ; ; 3.000 ; [get_ports sin[0]] ; timing.sdc:58 ; ;
; set_input_delay ; -add_delay ; ; ; ; -max ; [get_clocks clock] ; ; 4.000 ; [get_ports sin[1]] ; timing.sdc:58 ; ;
; set_input_delay ; -add_delay ; ; ; ; -min ; [get_clocks clock] ; ; 3.000 ; [get_ports sin[1]] ; timing.sdc:58 ; ;
-----+

-----+
; Set Output Delay
-----+
; SDC Command ; Add Delay ; Source Latency Included ; Clock Fall ; Flags ; Clock Name ; Reference Pin ; Delay ; Ports ; Location ; Comments ;
-----+
; set_output_delay ; -add_delay ; ; ; ; -max ; [get_clocks clock] ; ; 3.000 ; [get_ports sout] ; timing.sdc:63 ; ;
; set_output_delay ; -add_delay ; ; ; ; -min ; [get_clocks clock] ; ; 2.000 ; [get_ports sout] ; timing.sdc:63 ; ;
-----+

-----+
; SDC Ignored Assignments ;
-----+
No constraints were ignored.

```

WOC - timing.rpt (1)

```
-----  
; Report False Path ;  
-----
```

```
Nothing to report.  
-----
```

```
; Report Exceptions ;  
-----
```

```
No exceptions were found. Please note that an exception is one of: set_false_path, set_multicycle_path, set_min_delay, or set_max_delay
```

```
-----  
; Command Info ;  
-----
```

```
Report Path: Found 10 paths. Longest delay is 5.254
```

```
Tcl Command:
```

```
report_path -append -file timing.rpt -panel_name {Report Path} -npaths 0
```

```
Options:
```

```
-npaths 0  
-panel_name "Report Path"  
-file_name "timing.rpt"  
-append
```

```
Delay Model:
```

```
Slow 1200mV 85C Model
```

```
+-----+  
; Summary of Paths ;  
+-----+-----+  
; Delay ; From Node ; To Node ;  
+-----+-----+  
; 5.254 ; sin[0] ; sout ;  
; 5.156 ; sin[1] ; sout ;  
; 4.607 ; sin[0] ; regi ;  
; 4.582 ; sin[0] ; rego ;  
; 4.425 ; sin[1] ; regi ;  
; 4.422 ; sin[1] ; rego ;  
; 4.098 ; rego ; sout ;  
; 3.143 ; clk ; rego ;  
; 3.143 ; clk ; regi ;  
; 0.909 ; regi ; rego ;  
+-----+-----+
```

timing.rpt (2)

Path #1: Delay is 5.254

```

+-----+
; Path Summary ;
+-----+
; Property ; Value ;
+-----+
; From Node ; sin[0] ;
; To Node ; sout ;
; Delay ; 5.254 ;
+-----+

```

```

+-----+
; Statistics ;
+-----+
; Property ; Value ; Count ; Total Delay ; % of Total ; Min ; Max ;
+-----+
; Data Delay ; 5.254 ; ; ; ; ; ;
; Number of Logic Levels ; 2 ; ; ; ; ;
; Physical Delays ; ; ; ; ; ;
; IC ; 3 ; 1.361 ; 25 ; 0.000 ; 0.834 ;
; Cell ; 4 ; 3.893 ; 74 ; 0.000 ; 2.858 ;
+-----+

```

Note: Negative delays are omitted from totals when calculating percentages

```

+-----+
; Data Arrival Path ;
+-----+
; Total ; Incr ; RF ; Type ; Fanout ; Location ; Element ;
+-----+
; 5.254 ; 5.254 ; ; ; ; ; data path ;
; 0.000 ; 0.000 ; ; ; 1 ; PIN_E8 ; sin[0] ;
; 0.000 ; 0.000 ; FF ; IC ; 1 ; IOIBUF_X11_Y73_N1 ; sin[0]~input|i ;
; 0.775 ; 0.775 ; FF ; CELL ; 3 ; IOIBUF_X11_Y73_N1 ; sin[0]~input|o ;
; 1.609 ; 0.834 ; FF ; IC ; 1 ; LCCOMB_X11_Y72_N2 ; sout~0|datac ;
; 1.869 ; 0.260 ; FR ; CELL ; 1 ; LCCOMB_X11_Y72_N2 ; sout~0|combout ;
; 2.396 ; 0.527 ; RR ; IC ; 1 ; IOOBUF_X11_Y73_N16 ; sout~output|i ;
; 5.254 ; 2.858 ; RR ; CELL ; 1 ; IOOBUF_X11_Y73_N16 ; sout~output|o ;
; 5.254 ; 0.000 ; RR ; CELL ; 0 ; PIN_G8 ; sout ;
+-----+

```

...

timing.rpt (3)

we asked only for the worst 2 !!

```
-----
; Command Info ;
-----
Report Timing: Found 2 setup paths (0 violated). Worst case slack is 7.726

Tcl Command:
  report_timing -append -setup -file timing.rpt -panel_name {Report Timing} -from_clock [get_clocks { clock }] -npaths
2 -detail full_path

Options:
  -from_clock [get_clocks { clock }]
  -setup
  -npaths 2
  -detail full_path
  -panel_name {Report Timing}
  -file {timing.rpt}
  -append

Delay Model:
  Slow 1200mV 85C Model

-----+-----
; Summary of Paths ;
-----+-----
; Slack ; From Node ; To Node ; Launch Clock ; Latch Clock ; Relationship ; Clock Skew ; Data Delay ;
-----+-----+-----+-----+-----+-----+-----+-----+-----+
; 7.726 ; sin[0] ; sout ; clock ; clock ; 20.000 ; 0.000 ; 5.254 ;
; 7.824 ; sin[1] ; sout ; clock ; clock ; 20.000 ; 0.000 ; 5.156 ;
-----+-----+-----+-----+-----+-----+-----+-----+-----+
```

timing.rpt (4)

Path #1: Setup slack is 7.726

```

=====
+-----+
; Path Summary ;
+-----+
; Property ; Value ;
+-----+
; From Node ; sin[0] ;
; To Node ; sout ;
; Launch Clock ; clock ;
; Latch Clock ; clock ;
; Data Arrival Time ; 9.254 ;
; Data Required Time ; 16.980 ;
; Slack ; 7.726 ;
+-----+

```

```

+-----+
; Statistics ;
+-----+
; Property ; Value ; Count ; Total Delay ; % of Total ; Min ; Max ;
+-----+
; Setup Relationship ; 20.000 ; ; ; ; ; ;
; Clock Skew ; 0.000 ; ; ; ; ; ;
; Data Delay ; 5.254 ; ; ; ; ; ;
; Number of Logic Levels ; ; 2 ; ; ; ; ;
; Physical Delays ; ; ; ; ; ; ;
; Arrival Path ; ; ; ; ; ; ;
; Clock ; ; ; ; ; ; ;
; Clock Network (Lumped) ; ; 1 ; 0.000 ; ; 0.000 ; 0.000 ;
; Data ; ; ; ; ; ; ;
; IC ; ; 3 ; 1.361 ; 25 ; 0.000 ; 0.834 ;
; Cell ; ; 4 ; 3.893 ; 74 ; 0.000 ; 2.858 ;
; Required Path ; ; ; ; ; ; ;
; Clock ; ; ; ; ; ; ;
; Clock Network (Lumped) ; ; 1 ; 0.000 ; ; 0.000 ; 0.000 ;
+-----+

```

Note: Negative delays are omitted from totals when calculating percentages

timing.rpt (5)

```

-----+
; Data Arrival Path ;
-----+-----+-----+-----+-----+-----+-----+
; Total ; Incr ; RF ; Type ; Fanout ; Location ; Element ;
-----+-----+-----+-----+-----+-----+-----+
; 0.000 ; 0.000 ; ; ; ; ; ; launch edge time ;
; 0.000 ; 0.000 ; ; ; ; ; ; clock path ;
; 0.000 ; 0.000 ; R ; ; ; ; ; clock network delay ;
; 4.000 ; 4.000 ; F ; iExt ; 1 ; PIN_E8 ; sin[0] ;
; 9.254 ; 5.254 ; ; ; ; ; ; data path ;
; 4.000 ; 0.000 ; FF ; IC ; 1 ; IOIBUF_X11_Y73_N1 ; sin[0]~input|i ;
; 4.775 ; 0.775 ; FF ; CELL ; 3 ; IOIBUF_X11_Y73_N1 ; sin[0]~input|o ;
; 5.609 ; 0.834 ; FF ; IC ; 1 ; LCCOMB_X11_Y72_N2 ; sout~0|datac ;
; 5.869 ; 0.260 ; FR ; CELL ; 1 ; LCCOMB_X11_Y72_N2 ; sout~0|combout ;
; 6.396 ; 0.527 ; RR ; IC ; 1 ; IOOBUF_X11_Y73_N16 ; sout~output|i ;
; 9.254 ; 2.858 ; RR ; CELL ; 1 ; IOOBUF_X11_Y73_N16 ; sout~output|o ;
; 9.254 ; 0.000 ; RR ; CELL ; 0 ; PIN_G8 ; sout ;
-----+-----+-----+-----+-----+-----+-----+

```

```

-----+
; Data Required Path ;
-----+-----+-----+-----+-----+-----+-----+
; Total ; Incr ; RF ; Type ; Fanout ; Location ; Element ;
-----+-----+-----+-----+-----+-----+-----+
; 20.000 ; 20.000 ; ; ; ; ; ; latch edge time ;
; 20.000 ; 0.000 ; ; ; ; ; ; clock path ;
; 20.000 ; 0.000 ; R ; ; ; ; ; clock network delay ;
; 19.980 ; -0.020 ; ; ; ; ; ; clock uncertainty ;
; 16.980 ; -3.000 ; R ; oExt ; 0 ; PIN_G8 ; sout ;
-----+-----+-----+-----+-----+-----+-----+

```

...

BOC - timing.rpt (6)

```

-----
; Report False Path ;
-----
Nothing to report.
-----
; Report Exceptions ;
-----
No exceptions were found. Please note that an exception is one of: set_false_path, set_multicycle_path, set_min_delay, or set_max_delay

-----
; Command Info ;
-----
Report Path: Found 10 paths. Longest delay is 3.102

Tcl Command:
  report_path -append -file timing.rpt -panel_name {Report Path} -npaths 0

Options:
  -npaths 0
  -panel_name "Report Path"
  -file_name "timing.rpt"
  -append

Delay Model:
  Fast 1200mV 0C Model

+-----+
; Summary of Paths ;
+-----+-----+-----+
; Delay ; From Node ; To Node ;
+-----+-----+-----+
; 3.102 ; sin[0] ; sout ;
; 3.029 ; sin[1] ; sout ;
; 2.736 ; sin[0] ; regi ;
; 2.720 ; sin[0] ; rego ;
; 2.629 ; sin[1] ; regi ;
; 2.625 ; sin[1] ; rego ;
; 2.217 ; rego ; sout ;
; 2.037 ; clk ; rego ;
; 2.037 ; clk ; regi ;
; 0.438 ; regi ; rego ;
+-----+-----+-----+

```

timing.rpt (7)

Path #1: Delay is 3.102

```

=====
+-----+
; Path Summary ;
+-----+
; Property ; Value ;
+-----+
; From Node ; sin[0] ;
; To Node ; sout ;
; Delay ; 3.102 ;
+-----+

```

```

=====
; Statistics ;
+-----+
; Property ; Value ; Count ; Total Delay ; % of Total ; Min ; Max ;
+-----+
; Data Delay ; 3.102 ; ; ; ; ; ;
; Number of Logic Levels ; ; 2 ; ; ; ; ;
; Physical Delays ; ; ; ; ; ; ;
; IC ; ; 3 ; 0.697 ; 22 ; 0.000 ; 0.452 ;
; Cell ; ; 4 ; 2.405 ; 77 ; 0.000 ; 1.585 ;
+-----+

```

Note: Negative delays are omitted from totals when calculating percentages

```

=====
; Data Arrival Path ;
+-----+
; Total ; Incr ; RF ; Type ; Fanout ; Location ; Element ;
+-----+
; 3.102 ; 3.102 ; ; ; ; ; data path ;
; 0.000 ; 0.000 ; ; ; 1 ; PIN_E8 ; sin[0] ;
; 0.000 ; 0.000 ; FF ; IC ; 1 ; IOIBUF_X11_Y73_N1 ; sin[0]~input|i ;
; 0.687 ; 0.687 ; FF ; CELL ; 3 ; IOIBUF_X11_Y73_N1 ; sin[0]~input|o ;
; 1.139 ; 0.452 ; FF ; IC ; 1 ; LCCOMB_X11_Y72_N2 ; sout~0|datac ;
; 1.272 ; 0.133 ; FF ; CELL ; 1 ; LCCOMB_X11_Y72_N2 ; sout~0|combout ;
; 1.517 ; 0.245 ; FF ; IC ; 1 ; IOOBUF_X11_Y73_N16 ; sout~output|i ;
; 3.102 ; 1.585 ; FF ; CELL ; 1 ; IOOBUF_X11_Y73_N16 ; sout~output|o ;
; 3.102 ; 0.000 ; FF ; CELL ; 0 ; PIN_G8 ; sout ;
+-----+

```


timing.rpt (8)

we asked only for the worst 2 paths !!



```
-----
; Command Info ;
-----
Report Timing: Found 2 hold paths (0 violated).  Worst case slack is 0.289

Tcl Command:
  report_timing -append -hold -file timing.rpt -panel_name {Report Timing} -from_clock [get_clocks { clock }] -npaths 2 -detail full_path

Options:
  -from_clock [get_clocks { clock }]
  -hold
  -npaths 2
  -detail full_path
  -panel_name {Report Timing}
  -file {timing.rpt}
  -append

Delay Model:
  Fast 1200mV 0C Model

-----+
; Summary of Paths ;
-----+
; Slack ; From Node ; To Node ; Launch Clock ; Latch Clock ; Relationship ; Clock Skew ; Data Delay ;
-----+
; 0.289 ; regi ; rego ; clock ; clock ; 0.000 ; 0.042 ; 0.415 ;
; 3.224 ; sin[1] ; rego ; clock ; clock ; 0.000 ; 1.659 ; 1.967 ;
-----+
```

timing.rpt (9)

Path #1: Hold slack is 0.289

```

=====
+-----+
; Path Summary ;
+-----+
; Property ; Value ;
+-----+
; From Node ; regi ;
; To Node ; rego ;
; Launch Clock ; clock ;
; Latch Clock ; clock ;
; Data Arrival Time ; 2.012 ;
; Data Required Time ; 1.723 ;
; Slack ; 0.289 ;
+-----+

+-----+
; Statistics ;
+-----+
; Property ; Value ; Count ; Total Delay ; % of Total ; Min ; Max ;
+-----+
; Hold Relationship ; 0.000 ; ; ; ; ; ;
; Clock Skew ; 0.042 ; ; ; ; ; ;
; Data Delay ; 0.415 ; ; ; ; ; ;
; Number of Logic Levels ; ; 1 ; ; ; ;
; Physical Delays ; ; ; ; ; ;
; Arrival Path ; ; ; ; ; ;
; Clock ; ; ; ; ; ;
; IC ; ; 3 ; 0.956 ; 59 ; 0.000 ; 0.861 ;
; Cell ; ; 3 ; 0.641 ; 40 ; 0.000 ; 0.368 ;
; Data ; ; ; ; ; ;
; IC ; ; 2 ; 0.127 ; 30 ; 0.000 ; 0.127 ;
; Cell ; ; 3 ; 0.183 ; 44 ; 0.000 ; 0.152 ;
; uTco ; ; 1 ; 0.105 ; 25 ; 0.105 ; 0.105 ;
; Required Path ; ; ; ; ; ;
; Clock ; ; ; ; ; ;
; IC ; ; 3 ; 0.996 ; 60 ; 0.000 ; 0.897 ;
; Cell ; ; 3 ; 0.663 ; 39 ; 0.000 ; 0.368 ;
+-----+

```

Note: Negative delays are omitted from totals when calculating percentages

timing.rpt (10)

```

-----+-----+-----+-----+-----+-----+-----+-----+
; Data Arrival Path
-----+-----+-----+-----+-----+-----+-----+-----+
; Total ; Incr ; RF ; Type ; Fanout ; Location ; Element ;
-----+-----+-----+-----+-----+-----+-----+-----+
; 0.000 ; 0.000 ; ; ; ; ; ; launch edge time ;
; 1.597 ; 1.597 ; ; ; ; ; ; clock path ;
; 0.000 ; 0.000 ; ; ; ; ; ; source latency ;
; 0.000 ; 0.000 ; ; ; ; 1 ; PIN_J1 ; clk ;
; 0.000 ; 0.000 ; RR ; IC ; 1 ; IOIBUF_X0_Y36_N8 ; clk~input|i ;
; 0.368 ; 0.368 ; RR ; CELL ; 1 ; IOIBUF_X0_Y36_N8 ; clk~input|o ;
; 0.463 ; 0.095 ; RR ; IC ; 1 ; CLKCTRL_G2 ; clk~inputclkctrl|inclk[0] ;
; 0.463 ; 0.000 ; RR ; CELL ; 2 ; CLKCTRL_G2 ; clk~inputclkctrl|outclk ;
; 1.324 ; 0.861 ; RR ; IC ; 1 ; FF_X11_Y72_N13 ; regi|clk ;
; 1.597 ; 0.273 ; RR ; CELL ; 1 ; FF_X11_Y72_N13 ; regi ;
; 2.012 ; 0.415 ; ; ; ; ; ; data path ;
; 1.702 ; 0.105 ; ; ; uTco ; 1 ; FF_X11_Y72_N13 ; regi ;
; 1.702 ; 0.000 ; RR ; CELL ; 1 ; FF_X11_Y72_N13 ; regi|q ;
; 1.829 ; 0.127 ; RR ; IC ; 1 ; LCCOMB_X11_Y72_N24 ; rego_d|dataa ;
; 1.981 ; 0.152 ; RR ; CELL ; 1 ; LCCOMB_X11_Y72_N24 ; rego_d|combout ;
; 1.981 ; 0.000 ; RR ; IC ; 1 ; FF_X11_Y72_N25 ; rego|d ;
; 2.012 ; 0.031 ; RR ; CELL ; 1 ; FF_X11_Y72_N25 ; rego ;
-----+-----+-----+-----+-----+-----+-----+-----+

```

```

-----+-----+-----+-----+-----+-----+-----+-----+
; Data Required Path
-----+-----+-----+-----+-----+-----+-----+-----+
; Total ; Incr ; RF ; Type ; Fanout ; Location ; Element ;
-----+-----+-----+-----+-----+-----+-----+-----+
; 0.000 ; 0.000 ; ; ; ; ; ; latch edge time ;
; 1.639 ; 1.639 ; ; ; ; ; ; clock path ;
; 0.000 ; 0.000 ; ; ; ; ; ; source latency ;
; 0.000 ; 0.000 ; ; ; ; 1 ; PIN_J1 ; clk ;
; 0.000 ; 0.000 ; RR ; IC ; 1 ; IOIBUF_X0_Y36_N8 ; clk~input|i ;
; 0.368 ; 0.368 ; RR ; CELL ; 1 ; IOIBUF_X0_Y36_N8 ; clk~input|o ;
; 0.467 ; 0.099 ; RR ; IC ; 1 ; CLKCTRL_G2 ; clk~inputclkctrl|inclk[0] ;
; 0.467 ; 0.000 ; RR ; CELL ; 2 ; CLKCTRL_G2 ; clk~inputclkctrl|outclk ;
; 1.364 ; 0.897 ; RR ; IC ; 1 ; FF_X11_Y72_N25 ; rego|clk ;
; 1.659 ; 0.295 ; RR ; CELL ; 1 ; FF_X11_Y72_N25 ; rego ;
; 1.639 ; -0.020 ; ; ; ; ; ; clock pessimism removed ;
; 1.639 ; 0.000 ; ; ; ; ; ; clock uncertainty ;
; 1.723 ; 0.084 ; ; ; uTh ; 1 ; FF_X11_Y72_N25 ; rego ;
-----+-----+-----+-----+-----+-----+-----+-----+

```

...

Paths

Command Info	Summary of Paths
Report Path: Found 10 paths. Longest delay is 5.254	
Tcl Command: report_path -panel_name {Report Path} -npaths 0	
Options: -npaths 0 -panel_name "Report Path"	
Delay Model: Slow 1200mV 85C Model	

Command Info	Summary of Paths		
	Delay	From Node	To Node
1	5.254	sin[0]	sout
2	5.156	sin[1]	sout
3	4.607	sin[0]	regi
4	4.582	sin[0]	rego
5	4.425	sin[1]	regi
6	4.422	sin[1]	rego
7	4.098	rego	sout
8	3.143	clk	rego
9	3.143	clk	regi
10	0.909	regi	rego

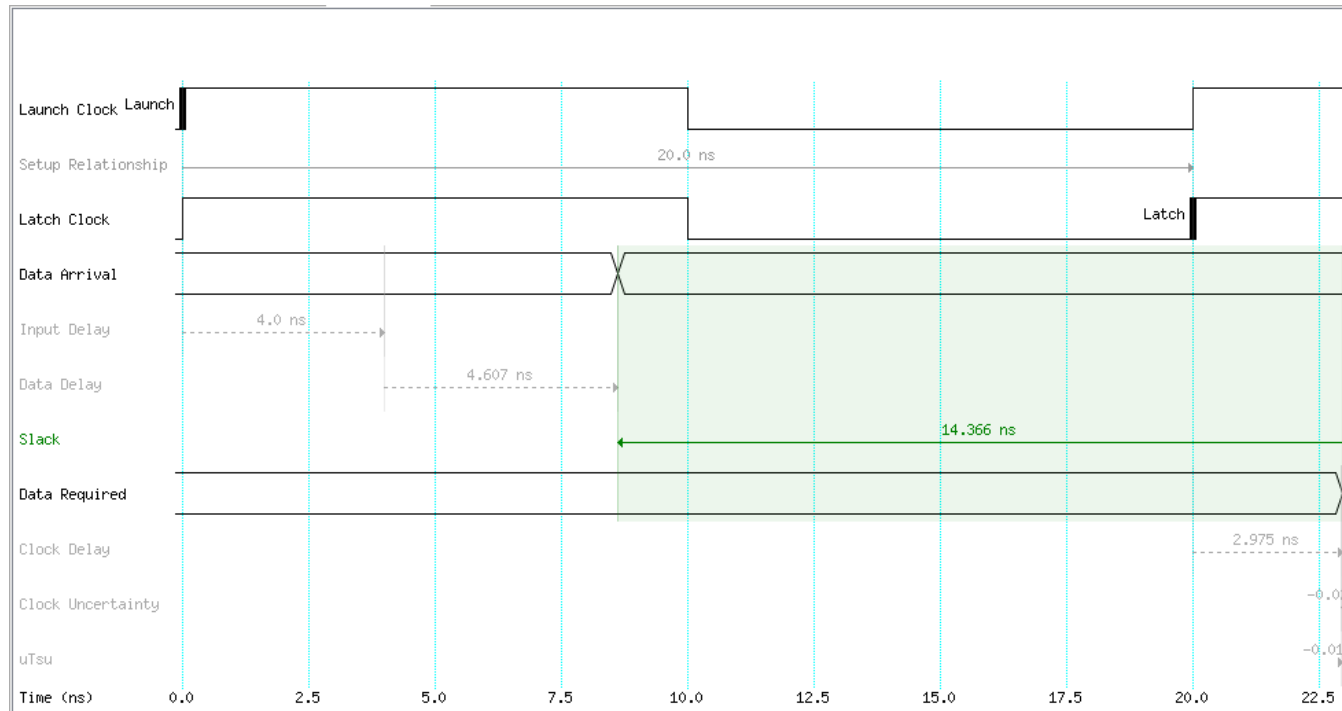
INREG Timing Paths

Command Info	Summary of Paths
Report Timing: Found 4 setup paths (0 violated). Worst case slack is 14.366	
Tcl Command: report_timing -setup -panel_name {Report Timing} -from [get_ports {sin[0] sin[1]}] -to [get_pins {regi d rego d}] -from_clock [get_clocks { clock }] -to_clock [get_clocks { clock }] -npaths 0 -detail full_path	
Options: -from [get_ports {sin[0] sin[1]}] -to [get_pins {regi d rego d}] -from_clock [get_clocks { clock }] -to_clock [get_clocks { clock }] -setup -npaths 0 -detail full_path -panel_name {Report Timing}	
Delay Model: Slow 1200mV 85C Model	

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	14.366	sin[0]	regi	clock	clock	20.000	2.975	4.607
2	14.391	sin[0]	rego	clock	clock	20.000	2.975	4.582
3	14.548	sin[1]	regi	clock	clock	20.000	2.975	4.425
4	14.551	sin[1]	rego	clock	clock	20.000	2.975	4.422

Path #1: Setup slack is 14.366

Path Summary		Statistics	Data Path	Waveform	Extra Fitter Information
	Property	Value			
1	From Node	sin[0]			
2	To Node	regi			
3	Launch Clock	clock			
4	Latch Clock	clock			
5	Data Arrival Time	8.607			
6	Data Required Time	22.973			
7	Slack	14.366			



Path #1: Setup slack is 14.366

Path Summary	Statistics	Data Path	Waveform	Extra Fitter Information
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Data Arrival Path R=rise, F=fall IC=interconnect, IExt = Input External

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	▲ 0.000	0.000					clock path
1	0.000	0.000	R				clock network delay
3	4.000	4.000	F	iExt	1	PIN_E8	sin[0]
4	▲ 8.607	4.607					data path
1	4.000	0.000	FF	IC	1	IOIBUF_X11_Y73_N1	sin[0]~input i
2	4.775	0.775	FF	CELL	3	IOIBUF_X11_Y73_N1	sin[0]~input o
3	8.110	3.335	FF	IC	1	LCCOMB_X11_Y72_N12	regi_d datab
4	8.503	0.393	FF	CELL	1	LCCOMB_X11_Y72_N12	regi_d combout
5	8.503	0.000	FF	IC	1	FF_X11_Y72_N13	regi d
6	8.607	0.104	FF	CELL	1	FF_X11_Y72_N13	regi

Data Required Path uTsu = setup delay

	Total	Incr	RF	Type	Fanout	Location	Element
1	20.000	20.000					latch edge time
2	▲ 22.975	2.975					clock path
1	20.000	0.000					source latency
2	20.000	0.000			1	PIN_J1	clk
3	20.000	0.000	RR	IC	1	IOIBUF_X0_Y36_N8	clk~input i
4	20.730	0.730	RR	CELL	1	IOIBUF_X0_Y36_N8	clk~input o
5	20.910	0.180	RR	IC	1	CLKCTRL_G2	clk~inputclkctrl indk[0]
6	20.910	0.000	RR	CELL	2	CLKCTRL_G2	clk~inputclkctrl outclk
7	22.420	1.510	RR	IC	1	FF_X11_Y72_N13	regi clk
8	22.975	0.555	RR	CELL	1	FF_X11_Y72_N13	regi
3	22.955	-0.020					clock uncertainty
4	22.973	0.018		uTsu	1	FF_X11_Y72_N13	regi

INOUT Timing Paths

Command Info Summary of Paths

Report Timing: Found 2 setup paths (0 violated). Worst case slack is 7.726

Tcl Command:

```
report_timing -setup -panel_name {Report Timing} -from [get_ports {sin[0] sin[1]}] -to [get_ports {sout}] -from_clock [get_clocks { clock }] -to_clock [get_clocks { clock }] -npaths 0 -detail full_path
```

Options:

```
-from [get_ports {sin[0] sin[1]}]
-to [get_ports {sout}]
-from_clock [get_clocks { clock }]
-to_clock [get_clocks { clock }]
-setup
-npaths 0
-detail full_path
-panel_name {Report Timing}
```

Delay Model:

Slow 1200mV 85C Model

Command Info Summary of Paths

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	7.726	sin[0]	sout	clock	clock	20.000	0.000	5.254
2	7.824	sin[1]	sout	clock	clock	20.000	0.000	5.156

Path #1: Setup slack is 7.726

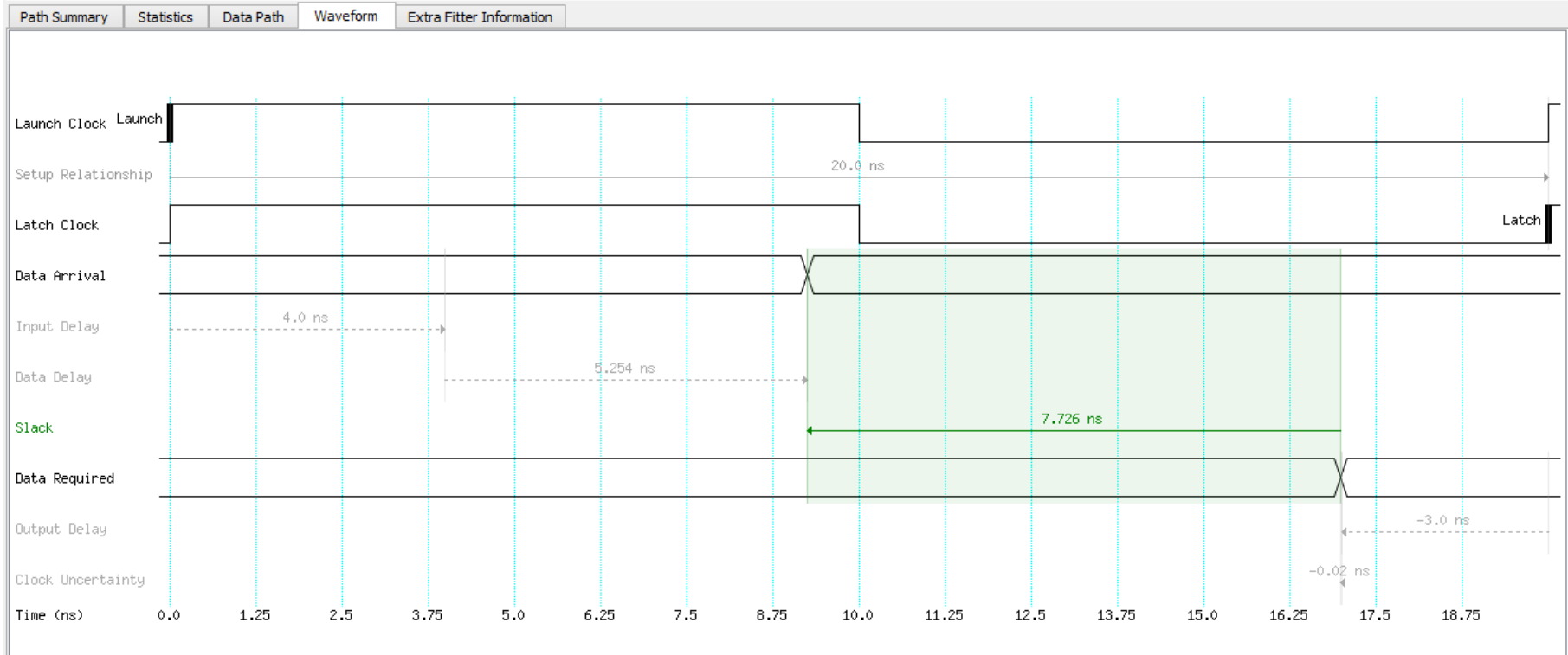
Path Summary Statistics Data Path

	Property	Value
1	From Node	sin[0]
2	To Node	sout
3	Launch Clock	clock
4	Latch Clock	clock
5	Data Arrival Time	9.254
6	Data Required Time	16.980
7	Slack	7.726

Path #1: Setup slack is 7.726

Path Summary		
Statistics		
Data Path		
	Property	Value
1	From Node	sin[0]
2	To Node	sout
3	Launch Clock	clock
4	Latch Clock	clock
5	Data Arrival Time	9.254
6	Data Required Time	16.980
7	Slack	7.726

Path #1: Setup slack is 7.726



Path #1: Setup slack is 7.726

Path Summary Statistics Data Path Waveform Extra Fitter Information

Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	▲ 0.000	0.000					clock path
1	0.000	0.000	R				clock network delay
3	4.000	4.000	F	iExt	1	PIN_E8	sin[0]
4	▲ 9.254	5.254					data path
1	4.000	0.000	FF	IC	1	IOIBUF_X11_Y73_N1	sin[0]~input i
2	4.775	0.775	FF	CELL	3	IOIBUF_X11_Y73_N1	sin[0]~input o
3	5.609	0.834	FF	IC	1	LCCOMB_X11_Y72_N2	sout~0 datac
4	5.869	0.260	FR	CELL	1	LCCOMB_X11_Y72_N2	sout~0 combout
5	6.396	0.527	RR	IC	1	IOOBUF_X11_Y73_N16	sout~output i
6	9.254	2.858	RR	CELL	1	IOOBUF_X11_Y73_N16	sout~output o
7	9.254	0.000	RR	CELL	0	PIN_G8	sout

OExt = Output External delay

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	20.000	20.000					latch edge time
2	▲ 20.000	0.000					clock path
1	20.000	0.000	R				clock network delay
3	19.980	-0.020					clock uncertainty
4	16.980	-3.000	R	oExt	0	PIN_G8	sout

REGOUT Timing Paths

Command Info Summary of Paths

Report Timing: Found 1 setup paths (0 violated). Worst case slack is 9.562

Td Command:

```
report_timing -setup -panel_name {Report Timing} -from [get_cells {reg0}] -to [get_ports {sout}] -from_clock [get_clocks { clock }] -to_clock [get_clocks { clock }] -npaths 0 -detail full_path
```

Options:

```
-from [get_cells {reg0}]
-to [get_ports {sout}]
-from_clock [get_clocks { clock }]
-to_clock [get_clocks { clock }]
-setup
-npaths 0
-detail full_path
-panel_name {Report Timing}
```

Delay Model:

Slow 1200mV 85C Model

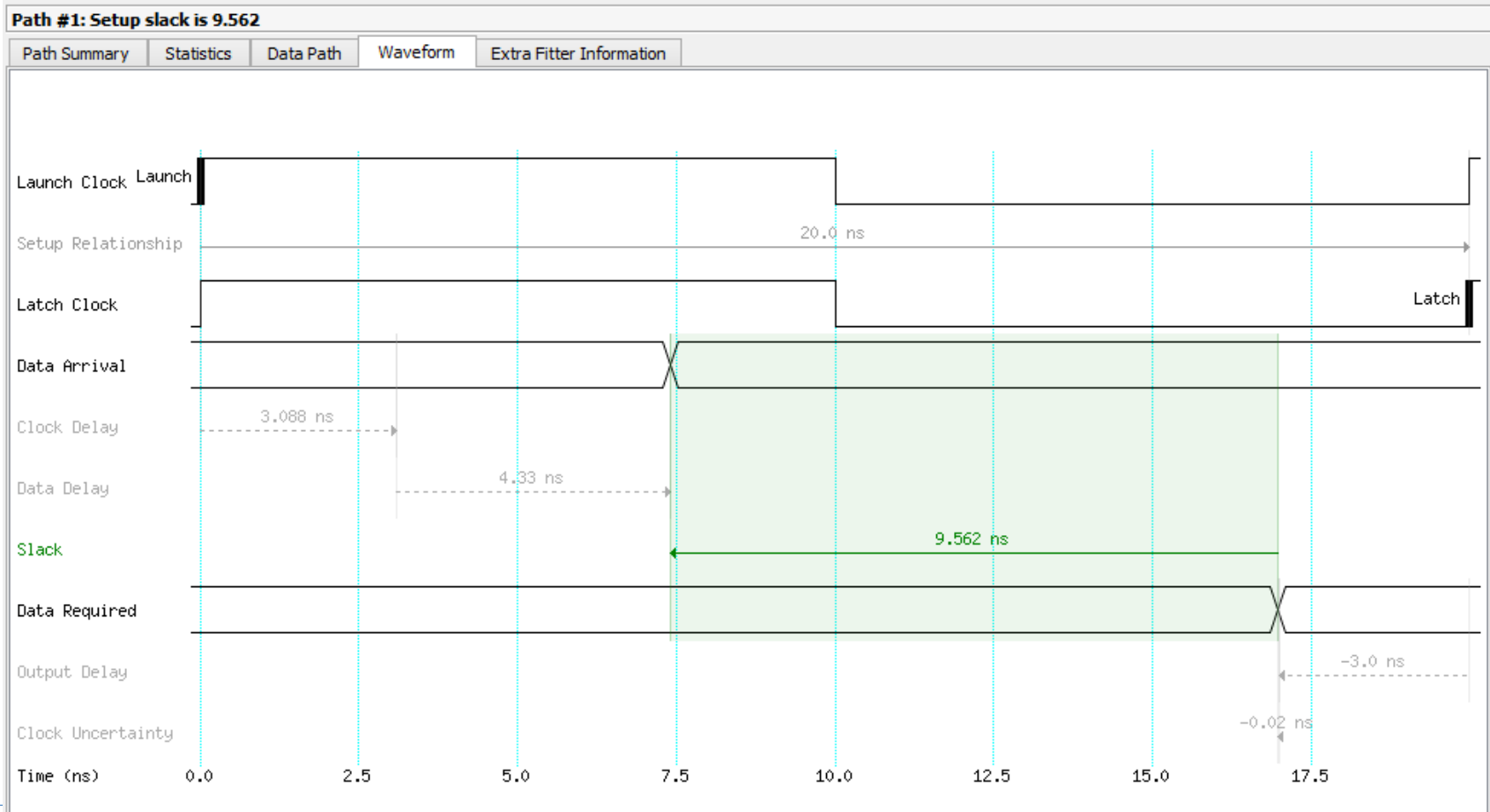
Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1 9.562	reg0	sout	clock	clock	20.000	-3.088	4.330

Path #1: Setup slack is 9.562

Path Summary	Statistics	Data Path	Waveform
	Property	Value	
1	From Node	reg0	
2	To Node	sout	
3	Launch Clock	clock	
4	Latch Clock	clock	
5	Data Arrival Time	7.418	
6	Data Required Time	16.980	
7	Slack	9.562	

Path #1: Setup slack is 9.562

Path Summary		
Property	Value	
1	From Node	rego
2	To Node	sout
3	Launch Clock	clock
4	Latch Clock	clock
5	Data Arrival Time	7.418
6	Data Required Time	16.980
7	Slack	9.562



Path #1: Setup slack is 9.562

Path Summary	Statistics	Data Path	Waveform	Extra Fitter Information
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Data Arrival Path uTco = clock to out delay

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	▲ 3.088	3.088					clock path
1	0.000	0.000					source latency
2	0.000	0.000			1	PIN_J1	clk
3	0.000	0.000	RR	IC	1	IOIBUF_X0_Y36_N8	clk~input i
4	0.730	0.730	RR	CELL	1	IOIBUF_X0_Y36_N8	clk~input o
5	0.917	0.187	RR	IC	1	CLKCTRL_G2	clk~inputclkctrl indk[0]
6	0.917	0.000	RR	CELL	2	CLKCTRL_G2	clk~inputclkctrl outclk
7	2.490	1.573	RR	IC	1	FF_X11_Y72_N25	rego clk
8	3.088	0.598	RR	CELL	1	FF_X11_Y72_N25	rego
3	▲ 7.418	4.330					data path
1	3.320	0.232		uTco	1	FF_X11_Y72_N25	rego
2	3.320	0.000	FF	CELL	1	FF_X11_Y72_N25	rego q
3	3.690	0.370	FF	IC	1	LCCOMB_X11_Y72_N2	sout~0 datab
4	4.115	0.425	FF	CELL	1	LCCOMB_X11_Y72_N2	sout~0 combout
5	4.602	0.487	FF	IC	1	IOOBUF_X11_Y73_N16	sout~output i
6	7.418	2.816	FF	CELL	1	IOOBUF_X11_Y73_N16	sout~output o
7	7.418	0.000	FF	CELL	0	PIN_G8	sout

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	20.000	20.000					latch edge time
2	▲ 20.000	0.000					clock path
1	20.000	0.000	R				clock network delay
3	19.980	-0.020					clock uncertainty
4	16.980	-3.000	F	oExt	0	PIN_G8	sout

CLOCK Timing Paths

Command Info Summary of Paths

Report Timing: Found 1 setup paths (0 violated). Worst case slack is 18.776

Tcl Command:
`report_timing -setup -panel_name {Report Timing} -from [get_registers {regi}] -to [get_registers {rego}] -from_clock [get_clocks { clock }] -to_clock [get_clocks { clock }] -npaths 0 -detail full_path`

Options:
`-from [get_registers {regi}]`
`-to [get_registers {rego}]`
`-from_clock [get_clocks { clock }]`
`-to_clock [get_clocks { clock }]`
`-setup`
`-npaths 0`
`-detail full_path`
`-panel_name {Report Timing}`

Delay Model:
 Slow 1200mV 85C Model

Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1 18.776	regi	rego	clock	clock	20.000	-0.081	1.141

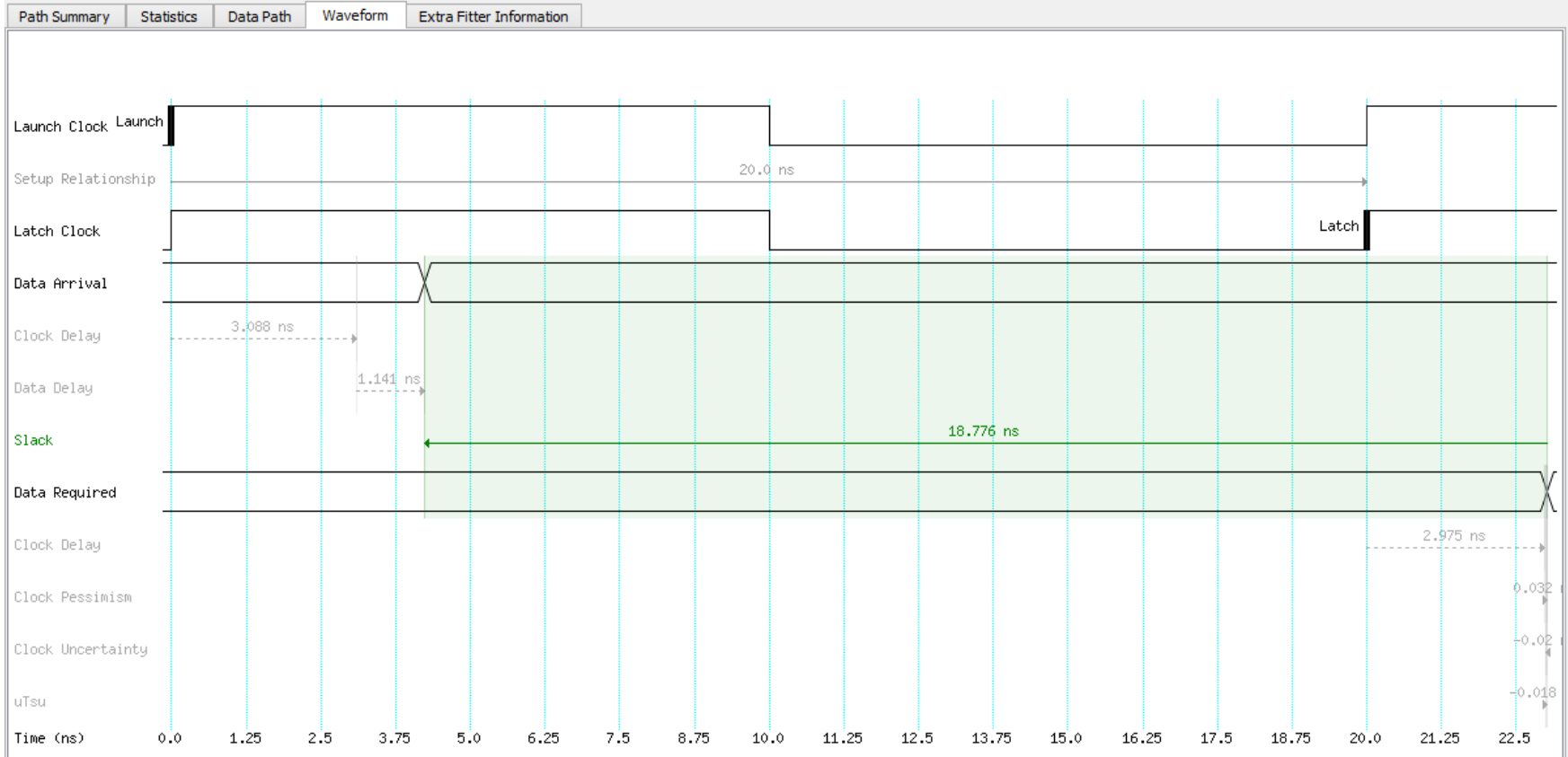
Path #1: Setup slack is 18.776

Path Summary	Statistics	Data Path
	Property	Value
1	From Node	regi
2	To Node	rego
3	Launch Clock	clock
4	Latch Clock	clock
5	Data Arrival Time	4.229
6	Data Required Time	23.005
7	Slack	18.776

Path #1: Setup slack is 18.776

Path Summary		
	Property	Value
1	From Node	regi
2	To Node	rego
3	Launch Clock	clock
4	Latch Clock	clock
5	Data Arrival Time	4.229
6	Data Required Time	23.005
7	Slack	18.776

Path #1: Setup slack is 18.776



Path #1: Setup slack is 18.776

Path Summary	Statistics	Data Path	Waveform	Extra Fitter Information
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Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	▲ 3.088	3.088					clock path
1	0.000	0.000					source latency
2	0.000	0.000			1	PIN_J1	clk
3	0.000	0.000	RR	IC	1	IOIBUF_X0_Y36_N8	clk~input i
4	0.730	0.730	RR	CELL	1	IOIBUF_X0_Y36_N8	clk~input o
5	0.917	0.187	RR	IC	1	CLKCTRL_G2	clk~inputclkctrl inclk[0]
6	0.917	0.000	RR	CELL	2	CLKCTRL_G2	clk~inputclkctrl outclk
7	2.490	1.573	RR	IC	1	FF_X11_Y72_N13	regi clk
8	3.088	0.598	RR	CELL	1	FF_X11_Y72_N13	regi
3	▲ 4.229	1.141					data path
1	3.320	0.232		uTco	1	FF_X11_Y72_N13	regi
2	3.320	0.000	FF	CELL	1	FF_X11_Y72_N13	regi q
3	3.701	0.381	FF	IC	1	LCCOMB_X11_Y72_N24	rego_d dataa
4	4.125	0.424	FF	CELL	1	LCCOMB_X11_Y72_N24	rego_d combout
5	4.125	0.000	FF	IC	1	FF_X11_Y72_N25	rego d
6	4.229	0.104	FF	CELL	1	FF_X11_Y72_N25	rego

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	20.000	20.000					latch edge time
2	▲ 23.007	3.007					clock path
1	20.000	0.000					source latency
2	20.000	0.000			1	PIN_J1	clk
3	20.000	0.000	RR	IC	1	IOIBUF_X0_Y36_N8	clk~input i
4	20.730	0.730	RR	CELL	1	IOIBUF_X0_Y36_N8	clk~input o
5	20.910	0.180	RR	IC	1	CLKCTRL_G2	clk~inputclkctrl inclk[0]
6	20.910	0.000	RR	CELL	2	CLKCTRL_G2	clk~inputclkctrl outclk
7	22.420	1.510	RR	IC	1	FF_X11_Y72_N25	rego clk
8	22.975	0.555	RR	CELL	1	FF_X11_Y72_N25	rego
9	23.007	0.032					clock pessimism removed
3	22.987	-0.020					clock uncertainty
4	23.005	0.018		uTsu	1	FF_X11_Y72_N25	rego