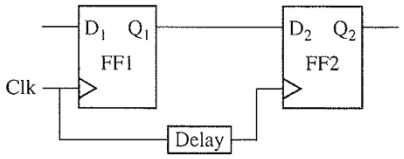
CPEN430 - Problem Set

Problem #1

Two flip-flops are connected as shown below. The delay represents wiring delay between the two clock inputs, which results in clock skew. This can cause possible loss of synchronization. The flip-flop propagation delay from clock to Q is 10 ns $<$ t_p $<$ 15 ns; the setup and hold times are 4 ns and 2 ns, respectively.

(a) What is the maximum value that the delay can have and still achieve proper synchronous operation? Draw a timing diagram to justify your answer.

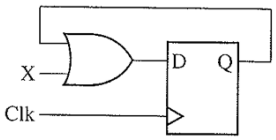


(b) Assuming that the delay is $<$ 3 ns, what is the minimum allowable clock period?

Problem #2

A D flip-flop has a setup time of 5 ns, a hold time of 3 ns, and a propagation delay from the rising edge of the clock to the change in flip-flop output in the range of 6 to 12 ns. An OR gate delay is in the range of 1 to 4 ns.

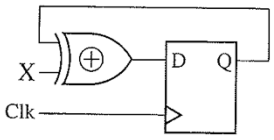
(a) What is the minimum clock period for proper operation of the following circuit?



(b) What is the earliest time after the rising clock edge that X is allowed to change?

Problem #3

In the following circuit, the XOR gate has a delay in the range of 2 to 16 ns. The *D* flip-flop has a propagation delay from clock to *Q* in the range 12 to 24 ns. The setup time is 8 ns, and the hold time is 4 ns.



(a) What is the minimum clock period for proper operation of the circuit?
(b) What are the earliest and latest times after the rising clock edge that *X* is allowed to change and still have proper synchronous operation? (Assume minimum clock period from (a).)

Problem #4

Simulate the mux 2:1 examined in class (files: mux-rtl.vhd and mux-tb.vhd) . Attach a printout of your simulation's waveforms. NOTE: The background must be white !!!