CPEN430 - Problem Set

Problem #1

(a) What do the acronyms VHDL and VHSIC stand for?
(b) How does a hardware description language like VHDL differ from an ordinary programming language?
(c) What are the advantages of using a hardware description language as compared with schematic capture in the design process?

Problem #2

Given the concurrent VHDL statements:

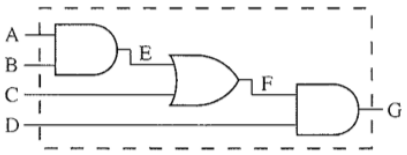
```
B <= A and C after 3ns;
C <= not B after 2ns;
```

(a) Draw the circuit the statements represent.
(b) Draw a timing diagram if initially $A = B =$ '0' and $C =$ '1', and A changes to '1' at time 5 ns.

Problem #3

Write VHDL code for the following circuit. Assume that the gate delays are negligible.

(a) Use concurrent statements.
(b) Use a process with sequential statements.



Problem #4

(a) What device does the following VHDL code represent?

```
process(CLK, Clr, Set)
begin
  if Clr = '1' then Q <= '0';
  elsif Set = '1' then Q <= '1';
  elsif CLK'event and CLK  = '0' then
    Q <= D;
  end if;
end process;
```

(b) What happens if $Clr = Set =$ '1' in the device in part (a)?

(c) Write the complete code and synthesize it with Altera's Quartus. Attach a shapshot of the synthesized code (hint: use RTL view)

(d) Write a testbench for the circuit and simulate it using Modelsim. Attach a shapshot of your simulation's waveforms. NOTE: The background must be white !!!