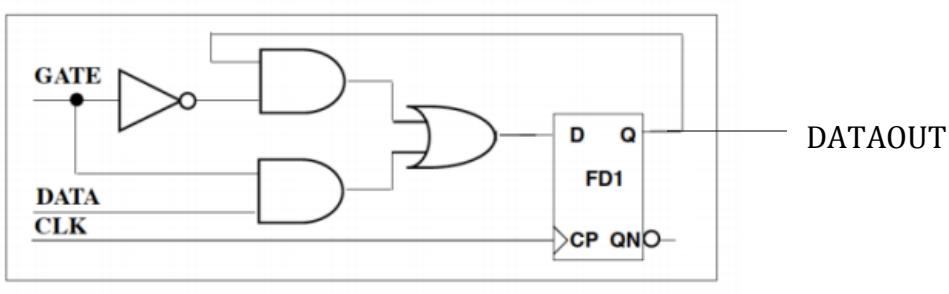
# *CPEN430 - Problem Set*

## *Problem #1*

Given the following circuit code it and simulate it in VHDL.




(a) Synthesize the circuit with Altera's Quartus. Attach your VHDL code and shapshot of the synthesized code (hint: use RTL viewer)
(b) Write a VHDL testbench for the circuit and simulate it using Modelsim. Attach your testbench code and a shapshot of your simulation's waveforms. NOTE: The background must be white !!!