CPEN430 - Problem Set

Problem #1

Write a VHDL description of an S-R Latch using a process.

Problem #2

Consider the following VHDL code:

```
entity Q3 is
  port(A, B, C, F, Clk: in [redacted] std_logic;
       E: out [redacted] std_logic);
end Q3;

architecture Qint of Q3 is
  signal D, G: [redacted] std_logic;
begin
  process(Clk)
  begin
    if Clk'event and Clk = '1' then
      D <= A and B and C;
      G <= not A and not B;
      E <= D or G or F;
    end if;
  end process;
end Qint;
```

(a) Draw a block diagram for the circuit (no gates—at block level only).
(b) Give the circuit generated by the preceding code (at the gate level)

Problem #3

Draw the circuit represented by the following VHDL process.

```
process(clk, clr)
begin
  if clr = '1' then Q <= '0';
  elsif clk'event and clk = '0' and CE = '1' then
    if C = '0' then Q <= A and B;
    else Q <= A or B; end if;
  end if;
end process;
```

Why is *clr* on the sensitivity list but *C* is not?