CPEN430 - Problem Set

Problem #1

Write a VHDL module that describes a 16-bit serial-in, serial-out shift register with inputs *SI* (serial input), *EN* (enable), and *CK* (clock, shifts on rising edge) and a serial output (*SO*).

Problem #2

In the following code, *state* and *nextstate* are integers with a range of 0 to 2.

```
process(state, X)
begin
  case state is
    when 0 => if X = '1' then nextstate <= 1;
    when 1 => if X = '0' then nextstate <= 2;

     when 2 => if X = '1' then nextstate <= 0;
  end case;
end process;
```

(a) Explain why a latch would be created when the code is synthesized.
(b) What signal would appear at the latch output?
(c) Make changes in the code which would eliminate the latch.

Problem #3

What is wrong with the following model of a 4-to-1 MUX? (It is not a syntax error.)

```
architecture mux_rtl of 4to1mux is
signal sel: integer range 0 to 3;
begin
  process(A, B, I0, I1, I2, I3)
  begin
    sel <= 0;
    if A = '1' then sel <= sel + 1; end if;
    if B = '1' then sel <= sel + 2; end if;
    case sel is
      when 0 => F <= I0;
      when 1 => F <= I1;
      when 2 => F <= I2;
      when 3 => F <= I3;
    end case;
  end process;
end mux_rtl;
```