CPEN430 - Problem Set

Problem #1

Examine the following VHDL code and complete the following exercises:

```
entity Problem
  port(X, CLK: in std_logic;
       Z1, Z2: out std_logic);
end Problem;

architecture Table of Problem is
  signal State, Nextstate: integer range 0 to 3 := 0;
begin
  process(State, X)       --Combinational Circuit
  begin
    case State is
      when 0 =>
        if X = '0' then Z1 < = '1'; Z2 <= '0'; Nextstate < = 0;
        else Z1 < = '0'; Z2 < = '0'; Nextstate < = 1; end if;
      when 1 =>
        if X = '0' then Z1 < = '0'; Z2 <= '1'; Nextstate < = 1;
        else Z1 < = '0'; Z2 < = '1'; Nextstate < = 2; end if;
      when 2 =>
        if X = '0' then Z1 < = '0'; Z2 <= '1'; Nextstate < = 2;
        else Z1 < = '0'; Z2 < = '1'; Nextstate < = 3; end if;
      when 3 =>
        if X = '0' then Z1 < = '0'; Z2 <= '0'; Nextstate < = 0;
        else Z1 < = '1'; Z2 < = '0'; Nextstate < = 1; end if;
    end case;
  end process;
  process(CLK)            --State Register
  begin
    if CLK'event and CLK = '1' then     --rising edge of clock
      State <= Nextstate;
    end if;
  end process;
end Table;
```

(a) Draw a block diagram of the circuit implemented by this code.

(b) Write the state table that is implemented by this code.

Please answer part (b) by filling the following template:

State	Next State		X=0		X=1	
	X=0	X=1	Z1	Z2	Z1	Z2
S0						
S1						
S2						
S3						

Problem #2

(a) Construct an SM chart equivalent to the following state table. Test only one variable in each decision box. Try to minimize the number of decision boxes.

(b) Write a VHDL description of the state machine based on the SM chart.

Present State	Next State X_1X_2 = 00	01	10	11	Output (Z_1Z_2) X_1X_2 = 00	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01