High Speed Op-Amp Design: Compensation and Topologies for Two and Three Stage Designs

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Abstract:

As CMOS technology continues to evolve, the supply voltages are decreasing while at the same time the transistor threshold voltages are remaining relatively constant. Making matters worse, the inherent gain available from the nano-CMOS transistors is dropping. Traditional techniques for achieving high gain by vertically stacking (i.e. cascoding) transistors becomes less useful in sub-100nm processes. Horizontal cascading (multi-stage) must be used in order to realize op-amps in low supply voltage processes. This seminar discusses new design techniques for the realization of multi-stage op-amps. Both single- and fully-differential op-amps are presented where low power, small VDD, and high speed are important. The proposed, and experimentally verified, op-amps exhibit significant improvements in speed over the traditional op-amp designs while at the same time having smaller layout area.
Outline

- Introduction
- Two-stage Op-Amp Compensation
- Multi-stage Op-Amp Design
- Multi-stage Fully-Differential Op-Amps
- Conclusion
Op-Amps and CMOS Scaling

- The Operational Amplifier (op-amp) is a fundamental building block in Mixed Signal design.
  - Employed profusely in data converters, filters, sensors, drivers etc.
- Continued scaling in CMOS technology has been challenging the established paradigms for op-amp design.
- With downscaling in channel length (L)
  - Transition frequency increases (more speed).
  - Open-loop gain reduces (lower gains).
  - Supply voltage is scaled down (lower headroom) [1].

\[ f_T \propto \frac{V_{ov}}{L} \]
\[ g_m r_o \propto \frac{L}{V_{ov}} \]
CMOS Scaling Trends

- VDD is scaling down but $V_{THN}$ is almost constant.
  - Design headroom is shrinking faster.
- Transistor open-loop gain is dropping (~10’s in nano-CMOS)
  - Results in lower op-amp open-loop gain. But we need gain!
- Random offsets due to device mismatches. $\sigma_{\Delta VTH} \propto \frac{1}{L \cdot W}$

[3], [4].
Integration of Analog into Nano-CMOS?

- Design low-VDD op-amps.
  - Replace vertical stacking (cascoding) by horizontal cascading of gain stages (see the next slide).
- Explore more effective op-amp compensation techniques.
- Offset tolerant designs.
- Also minimize power and layout area to keep up with the digital trend.
- Better power supply noise rejection (PSRR).

Cascoding vs Cascading in Op-Amps

A Telescopic Two-stage Op-Amp

A Cascade of low-VDD Amplifier Blocks.
(Compensation not shown here)

V\text{DD}_\text{min} > 4V_{\text{ovn}} + V_{\text{ovp}} + V_{\text{THP}} \text{ with wide-swing biasing.} [1]

V\text{DD}_\text{min} = 2V_{\text{ovn}} + V_{\text{ovp}} + V_{\text{THP}}.

❑ Even if we employ wide-swing biasing for low-voltage designs, three- or higher stage op-amps will be indispensable in realizing large open-loop DC gain.

TWO-STAGE OP-AMP COMPENSATION
Direct (or Miller) Compensation

- Compensation capacitor \((C_c)\) between the output of the gain stages causes pole-splitting and achieves dominant pole compensation.
- An RHP zero exists at \(z_1 = \frac{g_{m2}}{C_c}\)
  - Due to feed-forward component of the compensation current \((i_C)\).
- The second pole is located at \(-\frac{g_{m2}}{C_1 + C_2}\)
- The unity-gain frequency is \(f_{un} = \frac{g_{m1}}{2\pi C_c}\)

![Diagram](image1.png)

- All the op-amps presented have been designed in AMI C5N 0.5\(\mu\)m CMOS process with scale=0.3 \(\mu\)m and \(L_{min}=2\).
  - The op-amps drive a 30pF off-chip load offered by the test-setup.
Drawbacks of Direct (Miller) Compensation

- The RHP zero decreases phase margin
  - Requires large $C_C$ for compensation (10pF here for a 30pF load!).
- Slow-speed for a given load, $C_L$.
- Poor PSRR
  - Supply noise feeds to the output through $C_C$.
- Large layout size.

Unlabeled NMOS are 10/2. Unlabeled PMOS are 22/2.
Indirect Compensation

- The RHP zero can be eliminated by blocking the feed-forward compensation current component by using
  - A common gate stage,
  - A voltage buffer,
  - Common gate “embedded” in the cascode diff-amp, or
  - A current mirror buffer.

- Now, the compensation current is fed-back from the output to node-1 indirectly through a low-Z node-A.

- Since node-1 is not loaded by $C_C$, this results in higher unity-gain frequency ($f_{un}$).
Indirect Compensation in a Cascoded Op-Amp

Indirect-compensation using cascoded current mirror load.

Employing the common gate device “embedded” in the cascode structure for indirect compensation avoids a separate buffer stage.

- Lower power consumption.
- Also voltage buffer reduces the swing which is avoided here.
Analytical Modeling of Indirect Compensation

The compensation current ($i_C$) is indirectly fed-back to node-1.

R_C is the resistance attached to node-A.

Small signal analytical model
Derivation of the Small-Signal Model

Resistance $r_{oc}$ is assumed to be large.

The small-signal model for a common gate indirect compensated op-amp topology is approximated to the simplified model seen in the last slide.

$g_{mc} >> r_{oc}^{-1}, R_A^{-1}$, $C_C >> C_A$
Analytical Results for Indirect Compensation

- Pole $p_2$ is much farther away from $f_{un}$.
  - Can use smaller $g_{m2}$ => less power!
- LHP zero improves phase margin.
- Much faster op-amp with lower power and smaller $C_C$.
- Better slew rate as $C_C$ is smaller.

\[
\frac{v_{out}}{v_s} = -A_v \left( \frac{1 + b_1 s}{1 + a_1 s + a_2 s^2 + a_3 s^3} \right)
\]

\[
z_1 \approx -\frac{1}{R_c C_c} \quad \text{LHP zero}
\]

\[
p_1 \approx -\frac{1}{a_1} = -\frac{1}{g_{m2} R_2 R_1 C_c}
\]

\[
p_2 \approx -\frac{a_1}{a_2} = -\frac{g_{m2} R_1 C_c}{C_2 (R_c C_c + R_1 C_1)} \approx -\frac{g_{m2} C_c}{C_L C_1}
\]

\[
p_3 \approx -\frac{a_2}{a_3} = -\left[ \frac{1}{R_c C_c} + \frac{1}{R_1 C_1} \right]
\]

\[
f_{un} = \left| \frac{p_1 A_v}{2\pi} \right| \approx \frac{g_{m1}}{2\pi C_c}
\]
Indirect Compensation Using Split-Length Devices

- As VDD scales down, cascoding is becoming tough. Then how to realize indirect compensation as we have no low-Z node available?
- Solution: Employ split-length devices to create a low-Z node.
  - Creates a pseudo-cascode stack but its really a single device.
- In the NMOS case, the lower device is always in triode hence node-A is a low-Z node. Similarly for the PMOS, node-A is low-Z.

 ![NMOS Diagram](image1)
![PMOS Diagram](image2)

Split-length 44/4 (=22/2) PMOS layout
Split-Length Current Mirror Load (SLCL) Op-Amp

- The current mirror load devices are split-length to create low-Z node-A.
- Here, \( f_{un} = 20 \text{MHz} \), \( \text{PM} = 75^\circ \) and \( t_s = 60 \text{ns} \).
SLCL Op-Amp Analysis

\[ v_{out} = A_{1} g_{mp} i_{d1} + v_{s2} C_L \]

\[ v_{out} = A_{1} g_{mp} i_{d2} - v_{s1} C_L \]

Here \( f_{z1} = 3.77 f_{un} \)

\( LHP \) zero appears at a higher frequency than \( f_{un} \).
The diff-pair devices are split-length to create low-Z node-A.

Here, $f_{un} = 35\text{MHz}$, $PM = 62^\circ$, $t_s = 75\text{ns}$.

Better PSRR due to isolation of node-A from the supply rails.
SLDP Op-Amp Analysis

\[ v_{out} = \frac{A}{i_d} v_s - v_{s2} \]

\[ C_L \]

\[ C_c \]

\[ g_{mn} \]

\[ f_{un} = \frac{2g_{m1}}{2\pi C_c} \]

\[ p_1 \approx -\frac{2}{g_{m2} R_2 R_1 C_c} \]

\[ |Re(p_2, 3)| = \frac{g_{m2}}{C_L} \sqrt{\frac{g_{mp} C_L}{C_m C_1}} \]

\[ z_1 \approx -\frac{4g_{mn}}{3(C_c + C_A)} = -\frac{2}{3(1 + \frac{1}{C_c + C_A})} \approx \frac{2\sqrt{2}}{3} \omega_{un} \]

- Here \( f_{z1} = 0.94 f_{un} \),
  - LHP zero appears slightly before \( f_{un} \) and flattens the magnitude response.
  - This may degrade the phase margin.

- Not as good as SLCL, but is of great utility in multi-stage op-amp design due to higher PSRR.
Test Chip 1: Two-stage Op-Amps

- AMI C5N 0.5µm CMOS, 1.5mmX1.5mm die size.
Test Results and Performance Comparison

Performance comparison of the op-amps for $C_L=30\text{pF}$.

<table>
<thead>
<tr>
<th>Op-amp Topology</th>
<th>$A_{DC}$ (dB)</th>
<th>$f_{un}$ (MHz)</th>
<th>$C_C$ (pF)</th>
<th>PM</th>
<th>$t_s$ (ns)</th>
<th>Power (mW)</th>
<th>Layout area (mm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Miller</td>
<td>57</td>
<td>2.5</td>
<td>10</td>
<td>74°</td>
<td>270</td>
<td>1.2</td>
<td>0.031</td>
</tr>
<tr>
<td>Miller with $R_Z$</td>
<td>57</td>
<td>2.7</td>
<td>10</td>
<td>85°</td>
<td>250</td>
<td>1.2</td>
<td>0.034</td>
</tr>
<tr>
<td>SLCL (this work)</td>
<td>66</td>
<td>20</td>
<td>2</td>
<td>75°</td>
<td>60</td>
<td>0.7</td>
<td>0.015</td>
</tr>
<tr>
<td>SLDP (this work)</td>
<td>60</td>
<td>35</td>
<td>2</td>
<td>62°</td>
<td>75</td>
<td>0.7</td>
<td>0.015</td>
</tr>
</tbody>
</table>

- 10X gain bandwidth ($f_{un}$).
- 4X faster settling time.
- 55% smaller layout area.
- 40% less power consumption.
MULTI-STAGE OP-AMP DESIGN
Three-Stage Op-Amps

- Higher gain can be achieved by cascading three gain stages.
  - $\sim 100$dB in 0.5$\mu$m CMOS
- Results in at least a third order system
  - 3 poles and two zeros.
  - RHP zero(s) degrade the phase margin.
- Hard to compensate and stabilize.
- Large power consumption compared to the two-stage op-amps.
Biasing of Multi-Stage Op-Amps

Diff-amps should be employed in inner gain stages to properly bias second and third gain stages:
- Current in third stage is precisely set.
- Robust against large offsets.
- Boosts the CMRR of the op-amp (needed).

Common source second stage should be avoided.
- Will work in feedback configuration but will have offsets in nano-CMOS processes.
Conventional Three-Stage Topologies

Nested Miller Compensation (NMC) [6]

- Requires $p_3=2p_2=4\omega_{un}$ for stability (Butterworth response)
  - Huge power consumption
- RHP zero appears before the LHP zero and degrades the phase margin.
- Second stage is non-inverting
  - Implemented using a current mirror.
  - Excess forward path delay (not modeled or discussed in the literature).
Conventional Three-Stage Topologies contd.

Nested Gm-C Compensation (NGCC) [7]

- Employs feed-forward $g_m$’s to eliminate zeros.
  - $g_{mf1} = g_{m1}$ and $g_{mf2} = g_{m2}$
- Class AB output stage.
- Hard to implement $g_{mf1}$ which tracks $g_{m1}$ for large signal swings.
  - Also wasteful of power.
- $g_{mf2}$ is a power device and will not always be equal to $g_{m2}$.
  - Compensation breaks down.
- Still consumes large power.
Conventional Three-Stage Topologies contd.

Transconductance with Capacitive Feedback Compensation (TCFC) [14]

- Four poles and double LHP zeros
  - One LHP zero $z_1$ cancels the pole $p_3$.
  - Other LHP zero $z_2$ enhances phase margin.
- Set $p_2=2\omega_{un}$ for $PM=60^\circ$.
- Relatively low power.
- Still design criterions are complex.
- Complicated bias circuit.
  - More power.
- Excess forward path delay.

\[ \begin{align*}
  V_{B1} & \quad V_{DD} \\
  & \downarrow \quad 1 \\
  & \downarrow \quad 2 \\
  g_{m1} & \quad \text{g}_{\mu/2} \\
  V_{B2} & \quad V_{DD} \\
  & \downarrow \quad 3 \\
  & \downarrow \quad 4 \\
  & \downarrow \quad 5 \\
  g_{m2} & \quad \text{g}_{\mu/2} \\
  V_{B3} & \quad V_{DD} \\
  & \downarrow \quad 6 \\
  & \downarrow \quad 7 \\
  & \downarrow \quad 8 \\
  g_{m3} & \quad \text{g}_{\mu/2} \\
  V_{B4} & \quad V_{DD} \\
  & \downarrow \quad 9 \\
  & \downarrow \quad 10 \\
  & \downarrow \quad 11 \\
  & \downarrow \quad 12 \\
  g_{m4} & \quad \text{g}_{\mu/2} \\
  \end{align*} \]
Three-Stage Topologies: Latest in the literature

Reverse Nested Miller with Voltage Buffer and Resistance (RNMC-VBR) [8]

- Employs reverse nesting of compensation capacitors
  - Since output is only loaded by only $C_{C2}$, results in potentially higher $f_{un}$. 
  - Third stage is always non-inverting.

- Uses pole-zero cancellation to realize higher phase margins.

- Excess forward path delay.

- Biasing not robust against process variations. How do you control the current in the output buffer?
Three-Stage Topologies: Latest in the literature contd.

Active Feedback Frequency Compensation (AFFC) [9]

- Reversed nested with elimination of RHP zero.
  - High gain block (HGB) realizes gain by cascading stages.
  - High speed block (HSB) implements compensation at high frequencies.
- Complex design criterions.
- Excess forward path delay. Again, uses a non-inverting gain stage.
- Employs a complicated bias circuit.
  - More power consumption.
Three-Stage Topologies: Latest in the literature contd.

- Various topologies have been recently reported by combining the earlier techniques.
  - RNMC feed-forward with nulling resistor (RNMCFNR) [17].
  - Reverse active feedback frequency compensation (RAFFC) [17].
- Further improvements are required in
  - Eliminating excess forward path delay arising due to the compulsory non-inverting stages.
  - Robust biasing against random offsets in nano-CMOS.
  - Further reduction in power and circuit complexity.
  - Better PSRR.
Indirect Compensation in Three-Stage Op-Amps

- Indirectly feedback the compensation currents $i_{c1}$ and $i_{c2}$.
  - Reversed Nested
    - Thus named RNIC.

- Employ diff-amp stages for robust biasing and higher CMRR.

- Use SLDP for higher PSRR.

- Minimum forward path delay.

- No compulsion on the polarity of gain stages.
  - Can realize any permutation of stage polarities by just changing the sign of the fed-back compensation current using ‘fbr’ and ‘fbl’ nodes.

- Low-voltage design.

- Note Class A (we’ll modify after theory is discussed).
Indirect Compensation in Three-Stage Op-Amps contd.

- Note the red arrows showing the node movements and the signs of the compensation currents.
  - $f_{br}$ and $f_{bl}$ are the low-Z nodes used for indirect compensation (have resistances $R_{c1}$ and $R_{c2}$ attached to them).
- The $C_C$’s are connected across two-nodes which move in opposite direction for overall negative feedback the compensation loops.
- Note feedback and forward delays!
Analysis of the Indirect Compensated 3-Stage Op-Amp

Plug in the indirect compensation model developed for the two-stage op-amps.

\[ v_{out} = A_v \left( \frac{b_0 + b_1 s + b_2 s^2}{a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4 + a_5 s^5} \right) \]

\[ z_1 = -\frac{1}{R_{c1}C_{c1}} \]

\[ z_2 = -\frac{1}{R_{c2}C_{c2}} \]

Two LHP zeros

\[ p_1 \approx -\frac{a_0}{a_1} = -\frac{1}{g_{m3}R_3g_{m2}R_2R_1C_{c2}} \]

\[ f_{un} = \frac{|p_1|A_v}{2\pi} \approx \frac{g_{m1}}{2\pi C_{c2}} \]

Four non-dominant poles.
Pole-zero Cancellation

- Poles $p_{4,5}$ are parasitic conjugated poles located far away in frequency.
  - Appear due to the loading of the nodes fbr and fbl.

- The small signal transfer function can be written as

$$A(s) = \frac{(b_0 + b_1 s + b_2 s^2)}{(1 + s/p_1) \left( 1 + \frac{a_2}{a_1} s + \frac{a_3}{a_1} s^2 \right) \left( 1 + \frac{a_4}{a_3} s + \frac{a_5}{a_3} s^2 \right)}$$

- The quadratic expression in the denominator describing the poles $p_2$ and $p_3$ can be canceled by the numerator which describes the LHP zeros.
  - Results in LHP zeros $z_1$ and $z_2$ canceling the poles $p_2$ and $p_3$ resp.

- The resulting expression looks like a single pole system for low frequencies. → Phase margin close to 90°.

$$\frac{v_{out}}{v_s} \approx -\frac{-A_v}{\left( 1 - \frac{s}{p_1} \right) \left( 1 + \frac{a_4}{a_3} s + \frac{a_5}{a_3} s^2 \right) \left( 1 - \frac{s}{p_1} \right)} \approx -\frac{-A_v}{\left( 1 - \frac{s}{p_1} \right)} \text{ for } f \ll f_T$$
Pole-zero Cancellation contd.

- Place pole-zero doublets \((p_2-z_1\) and \(p_3-z_2\)) out of \(f_{un}\) for clean transients.
  - i.e. \(f_{p2}, f_{p3} > f_{un}\).

- Best possible pole-zero arrangement for low power design.

- Results into design equations independent of parasitics \((C_3 \approx C_L\) here).

- \(R_{c1}\) and \(R_{c2}\) are realized by adding poly \(R\)’s in series with \(C_{C1}\) and \(C_{C2}\).
  - Also \(R_{c1}, R_{c2} \geq R_{c0}\), the impedance attached to the low-Z nodes fbr/fbl.

- Robust against even 50% process variations in \(R\)’s and \(C\)’s as long as the pole-zero doublets stay out of \(f_{un}\).

**Design Equations**

\[
R_{c1} \approx \frac{C_3}{g_{m3} C_{c2}}
\]

\[
R_{c2} \approx \frac{C_{c1}}{C_{c2}^2 g_{m3}} (C_3 + C_{c2})
\]
Pole-zero cancelled Class-A Op-Amp

- A Here, the poly resistors are estimated as $R_{kc} = R_{ck} - \frac{1}{\sqrt{2}g_{m1}}$, $k=1,2$

- Low power, simple, robust and manufacturable topology*.

- The presented three-stage op-amps have been designed with transient and SR performances to be comparable to their two-stage counterparts.
Pole-zero cancelled Class-AB Op-Amp 1

- A dual-gain path, low-power Class-AB op-amp topology (RNIC-1).
- The design equation for $R_{c1}$ is modified as $R_{c1} \approx \frac{C_3}{g_m C_2} - \frac{1}{g_m}$.
Pole-zero cancelled Class-AB Op-Amp 2

A single-gain path, Class-AB op-amp topology for good THD performance.

- Floating current source for biasing the output buffer.
- Here, $V_{\text{ncas}} = 2V_{\text{GS}}$ and $V_{\text{pcas}} = VDD - 2V_{\text{SG}}$.
- Note the lack of gratuitous forward delay.

Unlabeled NMOS are 10/2.
Unlabeled PMOS are 22/2.
Analytical model of the Class-AB (RNIC-1) topology is simulated in MATLAB.

The pole-zero plot illustrates the double pole-zero cancelation (collocation).

- p₄ and p₅ are parasitic poles located at frequencies close to that of the fₜ limited (or mirror) poles.

Here, fun≈30MHz and PM=90° for C_L=30pF.
Simulation of Three-stage Op-Amps contd.

- SPICE simulation of the same Class AB op-amp.
- $C_L=30\text{pF}$: $f_{\text{un}}=30\text{MHz}$, $PM\approx88^\circ$, $t_s=70\text{ns}$, $0.84\text{mW}$, $SR=20\text{V/}\mu\text{s}$.
- As fast as a two-stage op-amp with only 20% more power, at 50% VDD and with the same layout area (simpler bias circuit).
- Operates at VDD as low as 1.25V in a 5V process (25% of $V_{\text{DD}}$).
- SPICE simulation match with the MATLAB simulation
  - Our theory for three-stage indirect compensation is validated.
Chip 2: Low-VDD 3-Stage Op-Amps

- AMI C5N 0.5μm CMOS, 1.5mmX1.5mm die size.
Performance Comparison

<table>
<thead>
<tr>
<th>Topology</th>
<th>$C_L$ (pF)</th>
<th>$V_{DD}$ (V)</th>
<th>$I_{DP}$ (mA)</th>
<th>Power (mW)</th>
<th>$f_{max}$ (MHz)</th>
<th>Avg. SR (V/1ns)</th>
<th>$C_{st}$, $C_{sc}$ (pF)</th>
<th>FoM$_S$ (GHz/μW)</th>
<th>FoM$_L$ (GHz/μV)</th>
<th>IFoM$_S$ (GHz/μA/V)</th>
<th>IFoM$_L$ (GHz/μA/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MNM [10]</td>
<td>100</td>
<td>8</td>
<td>9.5</td>
<td>76</td>
<td>100</td>
<td>35</td>
<td>--</td>
<td>122</td>
<td>46</td>
<td>1053</td>
<td>368</td>
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<tr>
<td>NGCC [10]</td>
<td>20</td>
<td>2</td>
<td>0.34</td>
<td>0.68</td>
<td>0.61</td>
<td>2.5</td>
<td>--</td>
<td>18</td>
<td>74</td>
<td>36</td>
<td>147</td>
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<tr>
<td>NMCNFRK [11]</td>
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<td>2</td>
<td>0.2</td>
<td>0.4</td>
<td>1.8</td>
<td>0.79</td>
<td>30, 5.3</td>
<td>450</td>
<td>198</td>
<td>900</td>
<td>395</td>
</tr>
<tr>
<td>DFCFC [12]</td>
<td>1600</td>
<td>2</td>
<td>0.2</td>
<td>0.4</td>
<td>1</td>
<td>0.36</td>
<td>55.3</td>
<td>2500</td>
<td>900</td>
<td>5000</td>
<td>1800</td>
</tr>
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<td>AFFC [9]</td>
<td>100</td>
<td>1.5</td>
<td>0.17</td>
<td>0.255</td>
<td>5.5</td>
<td>0.36</td>
<td>5.4, 4</td>
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<td>ACBFC [13]</td>
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<td>1.9</td>
<td>1</td>
<td>10.3</td>
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<td>TCFC [14]</td>
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<td>3450</td>
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<td>30, 20</td>
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<td>RNMCVBR [16]</td>
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<td>1.44</td>
<td>19.46</td>
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<td>3, 0.7</td>
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<td>0.21</td>
<td>0.42</td>
<td>9</td>
<td>3.4</td>
<td>4</td>
<td>2571</td>
<td>971</td>
<td>5143</td>
<td>1943</td>
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<tr>
<td>RNNMFB [18]</td>
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<td>3</td>
<td>0.085</td>
<td>0.255</td>
<td>2.4</td>
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<td>500</td>
<td>3</td>
<td>0.105</td>
<td>0.315</td>
<td>2.4</td>
<td>1.95</td>
<td>11.5, 0.35</td>
<td>3810</td>
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<tr>
<td>RAFFC Low-Power [18]</td>
<td>500</td>
<td>3</td>
<td>0.035</td>
<td>0.105</td>
<td>1.1</td>
<td>1.29</td>
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<td>&lt;5238</td>
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<td>RNIC-1 (This work)</td>
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<td>3</td>
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<td>3</td>
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<td>11111</td>
<td>7407</td>
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<td>22222</td>
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<td>1.5</td>
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<td>6667</td>
<td>35000</td>
<td>20000</td>
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<tr>
<td>RNIC-1A (This work)</td>
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<td>2</td>
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<td>0.56</td>
<td>15</td>
<td>20</td>
<td>1, 2</td>
<td>864</td>
<td>1071</td>
<td>1607</td>
<td>2143</td>
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<tr>
<td>RNIC-2A (This work)</td>
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<td>0.18</td>
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<td>20</td>
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<td>RNIC-3A (This work)</td>
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<td>2</td>
<td>0.5</td>
<td>1</td>
<td>17</td>
<td>20</td>
<td>10, 0.2</td>
<td>&lt;8500</td>
<td>16000</td>
<td>17000</td>
<td>20000</td>
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</table>

- Figures of Merit
  - FoM$_S$ = $f_{max}$ $C_L$/Power
  - FoM$_L$ = SR $C_L$/Power
  - IFoM$_S$ = $f_{max}$ $C_L$/I$_{DD}$
  - IFoM$_L$ = SR $C_L$/I$_{DD}$

- RNIC op-amp designed for 500pF load for a fair comparison.
- FoMs>2X than state-of-the-art at $V_{DD}$=3V.
- Comparable performance even at lower $V_{DD}$=2V.
- Practical, stable and production worthy.
Performance Comparison contd.

- Higher performance figures than state-of-the-art.
- 10X faster settling.
- Better phase margins.
- Layout area same or smaller.

### Table: Op-amp Topology Comparison

<table>
<thead>
<tr>
<th>Op-amp Topology</th>
<th>VDD (V)</th>
<th>$C_L$ (pF)</th>
<th>Power (mW)</th>
<th>$f_{\text{un}}$ (MHz)</th>
<th>Avg. SR (V/µs)</th>
<th>PM ($°$)</th>
<th>$t_s$ (ns)</th>
<th>Area (mm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RNMCFBNR [18]</td>
<td>3</td>
<td>500</td>
<td>0.255</td>
<td>2.4</td>
<td>1.8</td>
<td>58</td>
<td>810</td>
<td>0.025</td>
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<tr>
<td>RAFFC [18]</td>
<td>3</td>
<td>500</td>
<td>0.315</td>
<td>2.4</td>
<td>1.95</td>
<td>58</td>
<td>560</td>
<td>0.025</td>
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<td>3</td>
<td>500</td>
<td>0.105</td>
<td>1.1</td>
<td>1.29</td>
<td>56</td>
<td>1000</td>
<td>0.024</td>
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<tr>
<td>RNIC-1 (This work)</td>
<td>3</td>
<td>30</td>
<td>0.84</td>
<td>30</td>
<td>20</td>
<td>89</td>
<td>70</td>
<td>0.018</td>
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<tr>
<td>RNIC-2 (This work)</td>
<td>3</td>
<td>500</td>
<td>0.54</td>
<td>12</td>
<td>8</td>
<td>88</td>
<td>250</td>
<td>0.022</td>
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<tr>
<td>RNIC-3 (This work)</td>
<td>3</td>
<td>500</td>
<td>1.5</td>
<td>35</td>
<td>20</td>
<td>72</td>
<td>100</td>
<td>0.031</td>
</tr>
<tr>
<td>RNIC-1A (This work)</td>
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<td>30</td>
<td>0.56</td>
<td>15</td>
<td>20</td>
<td>89</td>
<td>90</td>
<td>0.018</td>
</tr>
<tr>
<td>RNIC-2A (This work)</td>
<td>2</td>
<td>500</td>
<td>0.36</td>
<td>6</td>
<td>20</td>
<td>88</td>
<td>350</td>
<td>0.022</td>
</tr>
<tr>
<td>RNIC-3A (This work)</td>
<td>2</td>
<td>500</td>
<td>1</td>
<td>17</td>
<td>20</td>
<td>72</td>
<td>150</td>
<td>0.031</td>
</tr>
</tbody>
</table>
Flowchart for RNIC Op-Amp Design

1. Start with the initial specifications on \( I_{o}, C_{s}, A_{s}, \) and SR.
2. Split DC gain \( A_{o,DC} \) across \( A_{s} \) and \( A_{h} \).
3. Select the overdrive (% of VDC) which will set \( V_{DD}, I_{DD} \), and transistor gain \( g_{m}/r_{o} \).
4. Identify \( g_{m} \). Can initially set \( g_{m} \) equal to \( g_{m} \) or a to lower value.
5. Select \( C_{m} = g_{m}/r_{o} \).
6. Select \( C_{s} \) and \( g_{m} \) such that the \( p_{p,2} \) and \( p_{p,4} \) double locations are outside \( f_{R} \).
7. Calculate \( R_{L} \) and \( R_{o} \).
8. Is either of \( R_{L} \) or \( R_{o} \) negative?
   - Yes: Move the corresponding \( p_{n} \) double to a lower frequency by changing \( C_{m} \) and \( R_{o} \). May have to sacrifice \( f_{o} \).
   - No: Simulate the design for frequency response and transient settling.
9. Does the design meet the specifications?
   - Yes: End.
   - No: Nothing works! Revise biasing.
10. Are the parasitic poles \( (p_{p,4}) \) degrading PM by closing on \( f_{o} \)?
    - Yes: Increase \( p_{o} \).
    - No: Increase \( g_{m} \) or decrease \( C_{m} \).
11. More Speed?
    - Yes: Increase \( g_{m} \) or decrease \( C_{m} \).
    - No: Lower power?
      - Yes: In the worst case scenario decrease \( g_{m} \).
      - No: Smaller layout area?
        - Yes: Reduce \( C_{m} \), \( C_{o} \), or \( g_{m} \).
        - No: Increase bias current in the first stage (\( I_{B,1} \)) or use smaller Ci’s.
12. Better SR?
    - Yes: Increase \( p_{o} \).
    - No: Nothing works! Revise biasing.
N-Stage Indirect Compensation Theory

The three-stage indirect compensation theory has been extended to N-stages and the closed form small signal transfer function is obtained.

\[
\frac{v_{\text{out}}}{v_s} = \frac{1}{\sum_{k=1}^{n-1} \frac{1}{z_k}} \prod_{j=1}^{n-1} \frac{1 + s\tau_{j-1}}{1 + s\tau_j} + \prod_{j=1}^{n-1} R_k \sum_{r=1}^{n-1} \prod_{p=1}^{r} \frac{sC_{r-1}}{\sum_{q=r}^{n} \prod_{j=1}^{q} \frac{1 + s\tau_q}{1 + s\tau_{j-1}}} \prod_{j=r+1}^{n-1} \frac{1 + s\tau_{j-1}}{1 + s\tau_j}
\]

\[
z_k = \frac{1}{\tau_{c_k}} = \frac{1}{R_{c_k} C_{c_k}}, \quad k=1,\ldots,n-1
\]

\[
p_1 = \frac{1}{\prod_{k=2}^{n} g_{mk} R_k} \frac{1}{2\pi C_{c_{n-1}}}, \quad f_{\text{un}} \approx \frac{|A_c p_1|}{2\pi}, \quad A_c p_1 = \frac{g_{m1}}{2\pi C_{c_{n-1}}}
\]
MULTI-STAGE FULLY-DIFFERENTIAL OP-AMPS
Fully Differential Op-Amps

- Analog signal processing uses ‘only’ fully differential (FD) circuits.
  - Cancels switch non-linearities and even order harmonics.
  - Double the dynamic range.
- Needs additional circuitry to maintain the output common-mode level.
  - Common-mode feedback circuit (CMFB) is employed.

\[
V_{\text{op}} - V_{\text{om}} = -A(v_{\text{inp}} - v_{\text{inm}})
\]
The CMFB loop disturbs the DC biasing of the intermediate gain stages.

- Degrades the gain, performance and may cause instability.
Three-Stage FD Op-Amp Design: Solutions

Employ CMFB

1. Individually across all the stages.
2. Only across the last two stages as the biasing of the output buffer need not be precise.
3. Only in the third stage (output buffer).
Three-Stage FD Op-Amp Design

- Use CMFB only in the output (third) stage. → Manufacturable design.
  - Leaves the biasing of second and third stage alone without disturbing them.
- Employ diff-amp pairs in the second stage for robust biasing.
Three-Stage FD Op-Amp: Enlarged

First Gain Stage

Second Gain Stage

Output Buffer (Third Stage)

Unlabeled NMOS are 10/2.
Unlabeled PMOS are 22/2.
Chip 3: Low-VDD FD Op-Amps

- AMI C5N 0.5µm CMOS, 1.5mm×1.5mm die size.
Simulation and Performance Comparison

DC behavior

82dB gain

Transient response

\(ts = 275\,\text{ns}\)

<table>
<thead>
<tr>
<th>Topology</th>
<th>(C_L) (pF)</th>
<th>(V_{DD}) (V)</th>
<th>(I_{DD}) (mA)</th>
<th>Power (mW)</th>
<th>(f_{un}) (MHz)</th>
<th>Avg. SR (V/(\mu)s)</th>
<th>(C_{c1, c2}) (pF)</th>
<th>(t_s) (ns)</th>
<th>(\text{FoM}_S) (MHz,pF/mW)</th>
<th>(\text{FoM}_L) (V/(\mu)s,pF/mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buffered RNMC [19]</td>
<td>100</td>
<td>1.2</td>
<td>0.285</td>
<td>0.342</td>
<td>8.9</td>
<td>5.5</td>
<td>2, 0.65</td>
<td>2400</td>
<td>2602</td>
<td>1608</td>
</tr>
<tr>
<td>RNIC-1-FD (This work)</td>
<td>30</td>
<td>3</td>
<td>0.4</td>
<td>1.2</td>
<td>12</td>
<td>10</td>
<td>4, 4</td>
<td>275</td>
<td>300</td>
<td>250</td>
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<tr>
<td>RNIC-2-FD (This work)</td>
<td>500</td>
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<td>8</td>
<td>5, 0.2</td>
<td>370</td>
<td>8333</td>
<td>3333</td>
</tr>
</tbody>
</table>

>2.5X figure of merit (FoM).
Flowchart for Three-Stage FD Op-Amp Design

1. Start with the initial specifications on $f_{m}$, $C$, $A_{v}$, and SR.
2. Design a singly-ended pole-zero cancelled three-stage op-amp for the given specifications.
3. Convert the singly-ended op-amp into a fully differential one by mirroring it. Use a pair of diff-pairs for the second stage for robust biasing.
4. Add a CMFB circuit in the output buffer.
5. Update the value of $\beta$ corresponding to the output buffer and recalculate $R_{IC}$ and $R_{OC}$.
6. Simulate the design.
7. Does the design meet specifications?
   - Yes: End
   - No: Go back to Step 2.
Conclusions

- Indirect compensation leads to significantly faster, lower power op-amps with smaller layout area.
- Indirect compensation using split-length devices facilitates low-VDD op-amp design.
- Novel pole-zero canceled three-stage RNIC op-amps exhibit substantial improvement over the state-of-the-art.
- A theory for multi-stage op-amps is presented.
- New methodologies for designing multi-stage FD op-amps proposed which improve the state-of-the-art.
- All proposed op-amps are low voltage
  - Open new avenues for low-VDD mixed signal system design.
Future Scope

- Mathematical optimization of PZC op-amps.
- Design of low-VDD systems in nano-CMOS process
  - Pipelined and Delta-Sigma data converters,
  - Analog filters,
  - Audio drivers, etc.
- Further investigation into indirect-compensated op-amps for $n \geq 4$ stages.
References

[5] Slide courtesy: bwrc.eecs.berkeley.edu/People/Faculty/jan/presentations/ASPDACJanuary05.pdf
References contd.


Questions?