Voltage Biasing Considerations (From the CS atom toward the differential pair atom)

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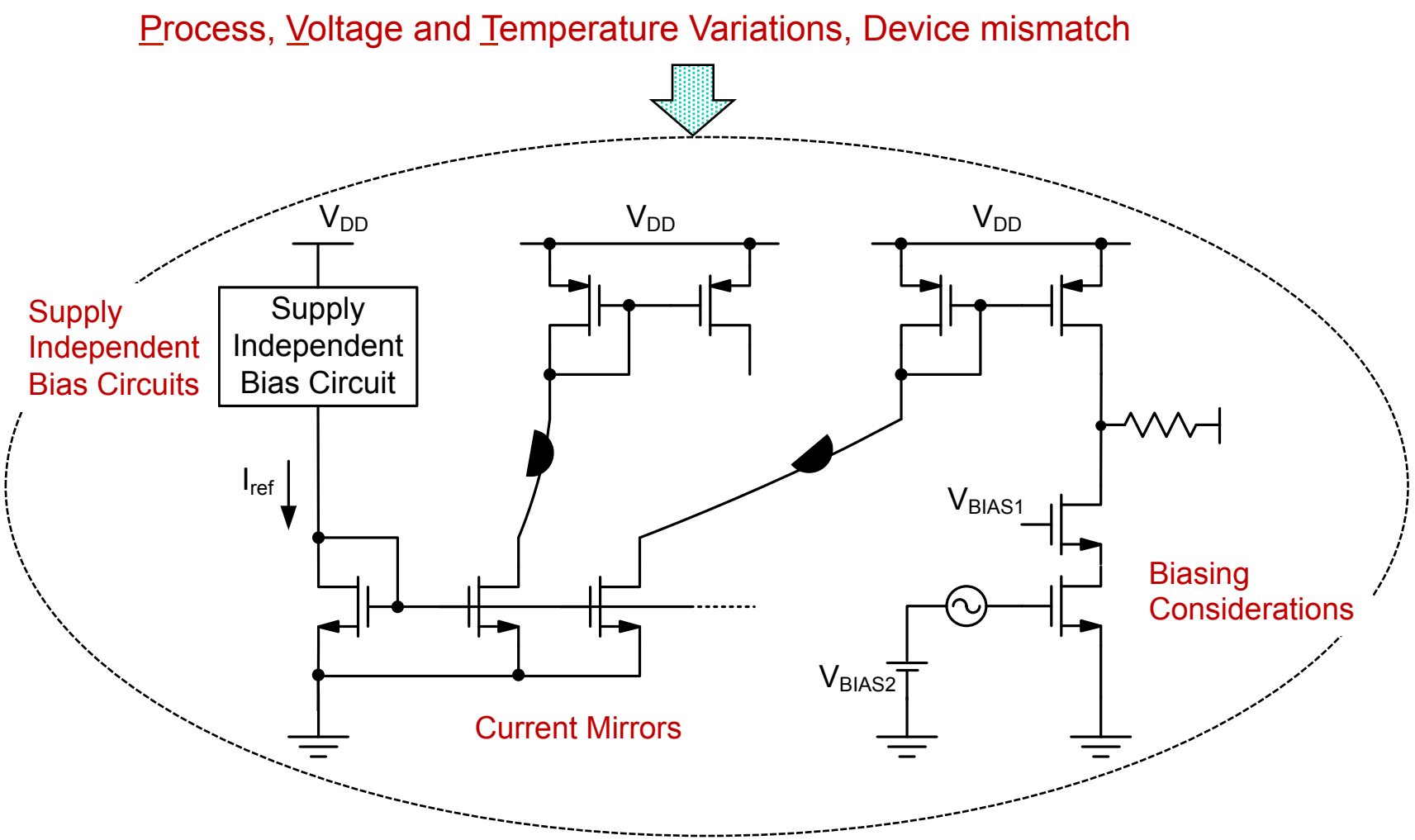
Voltage Biasing Considerations

- In addition to bias currents, building a complete analog circuit requires the generation of various bias voltages
- The CS stage is very sensitive to variations in its input bias voltage
  - In the majority of practical cases CS circuits are embedded in feedback networks that regulate the input bias voltage to the proper value, therefore absorbing process variations and mismatch effects (CMFB)
  - This complication typically does not exist for CG stages and CD stages

Assumptions so far …

- So far we have implicitly assumed
  - We have nearly ideal current and voltage sources available to set up the transistors' bias points
  - Transistor parameters and supply voltage do not vary
- As we move toward the practical implementation of transistor stages we we must
  - Focus on biasing schemes that are insensitive to variations commonly seen in IC technology

Overview


Process, Voltage and Temperature Variations, Device mismatch
Supply Independent Bias Circuits
Supply Independent Bias Circuit
VDD
VDD
VDD
Iref
VBIAS1
VBIAS2
Current Mirrors
Biasing Considerations

Variations

- Process-Voltage-Temperature (PVT) variations
  - global variations → they affect the devices on a chip uniformly
- Device mismatches
  - Local variations → Typically follows Gaussian distribution

- Process Corners: slow, nominal fast

- PVT corners
  - slow-slow
  - nom-nom
  - fast-fast

NMOS PMOS

$$\text{nominal} = P, V, T$$
$$\text{slow} = P_{slow}, V \downarrow, T \uparrow$$
$$\text{fast} = P_{fast}, V \uparrow, T \downarrow$$

$$\mu \propto T^{-3/2} \Leftrightarrow T \uparrow \rightarrow \mu \downarrow$$

[more temperature = more collisions = less mobility]

$$I \propto V^2 \Leftrightarrow V \uparrow \rightarrow I \uparrow$$

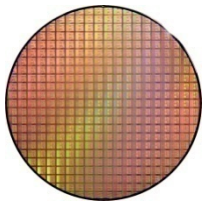
[more voltage = more current = less time to charge/discharge caps.]

PVT Variations

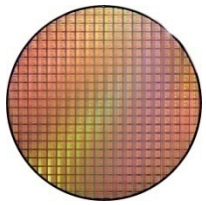
- PROCESS
  - Variations between production lots
  - "Slow, Nominal and Fast" corners
- VOLTAGE
  - V_{DD} is usually specified only within ±10%
  - E.g. V_{DD}= 4.5…5.5 V
- TEMPERATURE
  - Ambient temperature variations
  - 0…70°C (or −40…+125 °C)

source: R. Dutton, B. Murmann

Process Variations



Wafer made yesterday
All NMOS are “slow”
All PMOS are “nominal”
All R are nominal
All C are “fast”



Wafer made today
All NMOS are “fast”
All PMOS are “fast”
All R are nominal
All C are “slow”

Parameter	“Slow”	“Nominal”	“Fast”
V_T	0.65V	0.5V	0.35V
μC_{ox} (NMOS)	40 $\mu A/V^2$	50 $\mu A/V^2$	60 $\mu A/V^2$
μC_{ox} (PMOS)	20 $\mu A/V^2$	25 $\mu A/V^2$	30 $\mu A/V^2$
R_{poly2}	60Ω/□	50Ω/□	40Ω/□
R_{nwell}	1.4 kΩ/□	1 kΩ/□	0.6 kΩ/□
$C_{poly\text{-}poly2}$	1.15 fF/μm^2	1 fF/μm^2	0.85 fF/μm^2

source: R. Dutton, B. Murmann

Temperature Coefficients

Mostly due to the dependence on T of the surface potential Φ_S

Mostly due to the dependence on T of mobility

Parameter	Approximate TC
V_T	-1.2 mV/°C
μC_{ox} (NMOS)	-0.33 %/°C
μC_{ox} (PMOS)	-0.33 %/°C
R_{poly2}	+0.2 %/°C
R_{nwell}	+1 %/°C
$C_{poly\text{-}poly2}$	-30 ppm/°C

Temperature expands and contracts dielectric thickness

$$T \downarrow \Leftrightarrow t \downarrow \Leftrightarrow C \uparrow$$

```
* The default temperature in Spice is 25 degrees Celsius
* The following command sets the temperature to 100 degrees Celsius
.temp 100
```

Aside: V_T dependence on temperature

$$V_T = V_{T0} + \Delta V_T = V_{T0} + \gamma\left(\sqrt{\Phi_s - V_{BS}} - \sqrt{\Phi_s}\right)$$

- Both V_{T0} and ΔV_T depends on Φ_S

$$V_{T0} \propto \Phi_S$$

$$\Phi_S = \frac{2KT}{q}\ln\frac{N_{bulk}}{n_i} = Surface\ \ Potential \equiv PHI$$

$$\gamma = \frac{\sqrt{2q\varepsilon_S N_{bulk}}}{\varepsilon_{ox}/t_{ox}} = Body\ \ Effect\ \ Coefficient \equiv GAMMA$$

The higher the doping N_{bulk} the more voltage is required to produce an inversion layer: N_{bulk} goes up → V_T goes up
If $C_{ox} = \varepsilon_{ox}/t_{ox}$ is higher (= t_{ox} thinner) the less voltage is required to produce an inversion layer (Q=CV): C_{ox} goes up → V_T goes down

- The dependence on temperature of n_i is stronger than the linear dependence in the thermal voltage term (KT/q)
  - As a result: $for\ T \uparrow \Leftrightarrow V_T \downarrow$

Source: Muller and Kamins

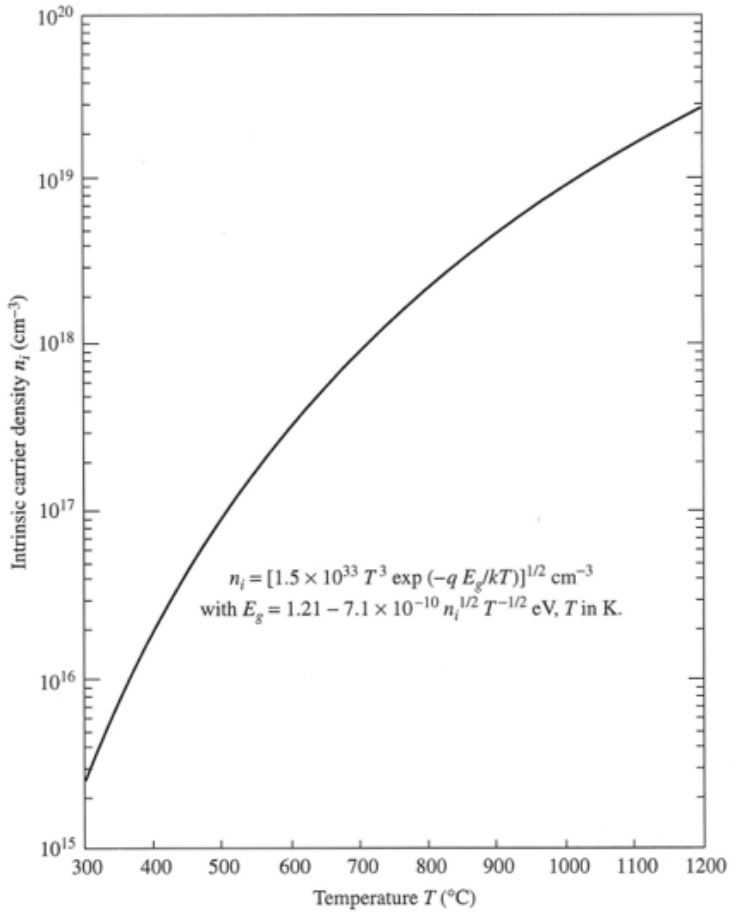
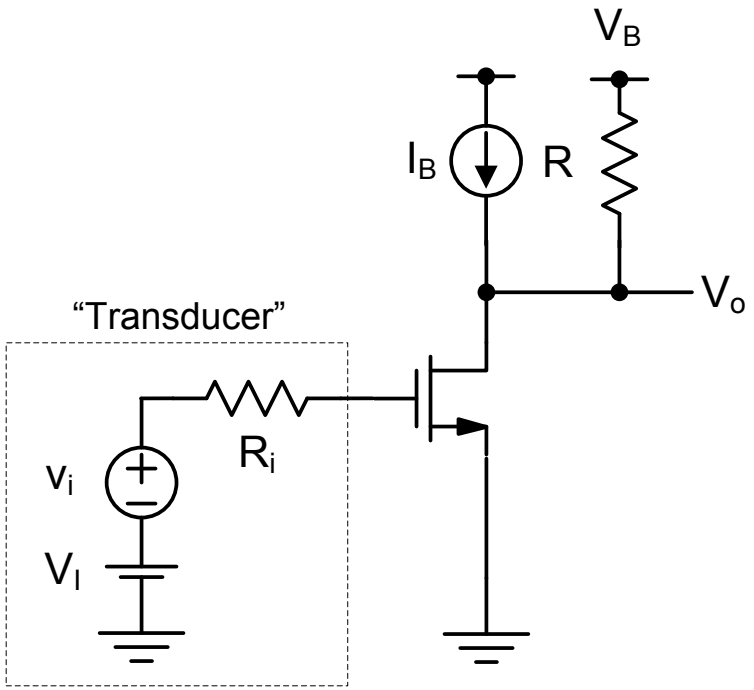


FIGURE 2.10 The intrinsic carrier density n_i in silicon between 300 and 1200°C [10].

Voltage Biasing for a CS stage

- CS stage revisited



Example:

$V_B = 2.5V$
$V_I = 1.394V$
$I_B = 500\mu A$
$W/L = 20\mu m/1\mu m$
$R = 5k\Omega$
$R_i = 50k\Omega$

- Nominal conditions: KP=50μA/V², VT0= 0.5V, TEMP=25°C
- Fast conditions: KP=60μA/V², VT0= 0.35V, TEMP=−20°C

HSPICE .OP output

```
*** .op output (nominal)
element  0:mn1
region      Saturati
  id         499.6020u
  vgs          1.3940
  vds          2.5020
  vth        500.0000m
  vod        894.0000m
  beta         1.2502m
  gm           1.1177m
  gds         39.9618u
...
```

```
*** .op output (fast, -20degC)
element  0:mn1
region       Linear
  id         817.8268u
  vgs          1.3940
  vds        910.8661m
  vth        402.0530m
  vod        991.9470m
  beta         1.6735m
  gm           1.5243m
  gds        210.6442u
...
```

Ouch !!

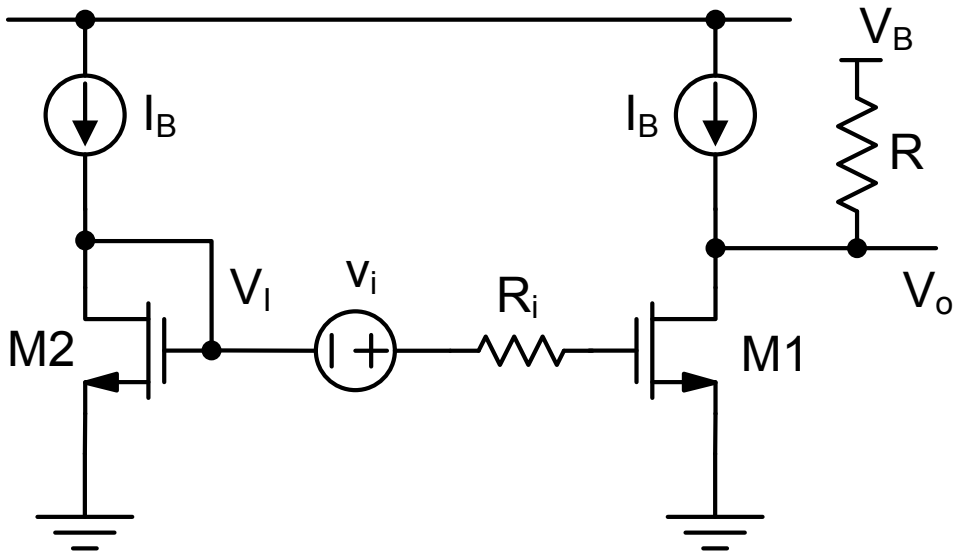
source: R. Dutton, B. Murmann

The Problem with This Circuit

- Process and temperature variations cause large changes in V_T and mobility (μ)
  - But V_I is kept constant, causing large changes in I_D, forcing the device into the triode region
- First cut idea
  - Use another MOSFET to "compute" V_I such that I_D stays roughly constant and tracks process and temperature
  - Note that the same "trick" is used in a current mirror

source: R. Dutton, B. Murmann

First Cut Solution



- What we expect to see in simulation
  - V_I ($=V_{GS1}=V_{GS2}$) changes with process and temperature
  - But I_{D1} and V_O stay roughly constant

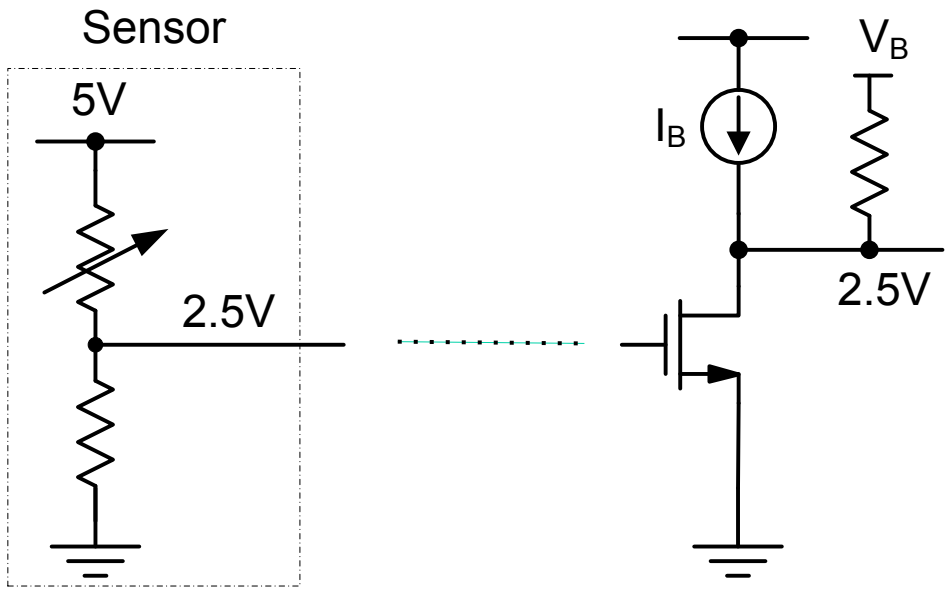
HSPICE .OP Output

```
*** .op output (nominal)
 element    0:m1         0:m2
 region      Saturati     Saturati
  id        538.2075u    500.0000u
  vgs         1.4351       1.4351
  vds         2.3090       1.4351
  vth       500.0000m    500.0000m
  beta        1.2309m      1.1435m
  gm          1.1511m      1.0694m
  gds        43.7248u     43.7248u
...
```

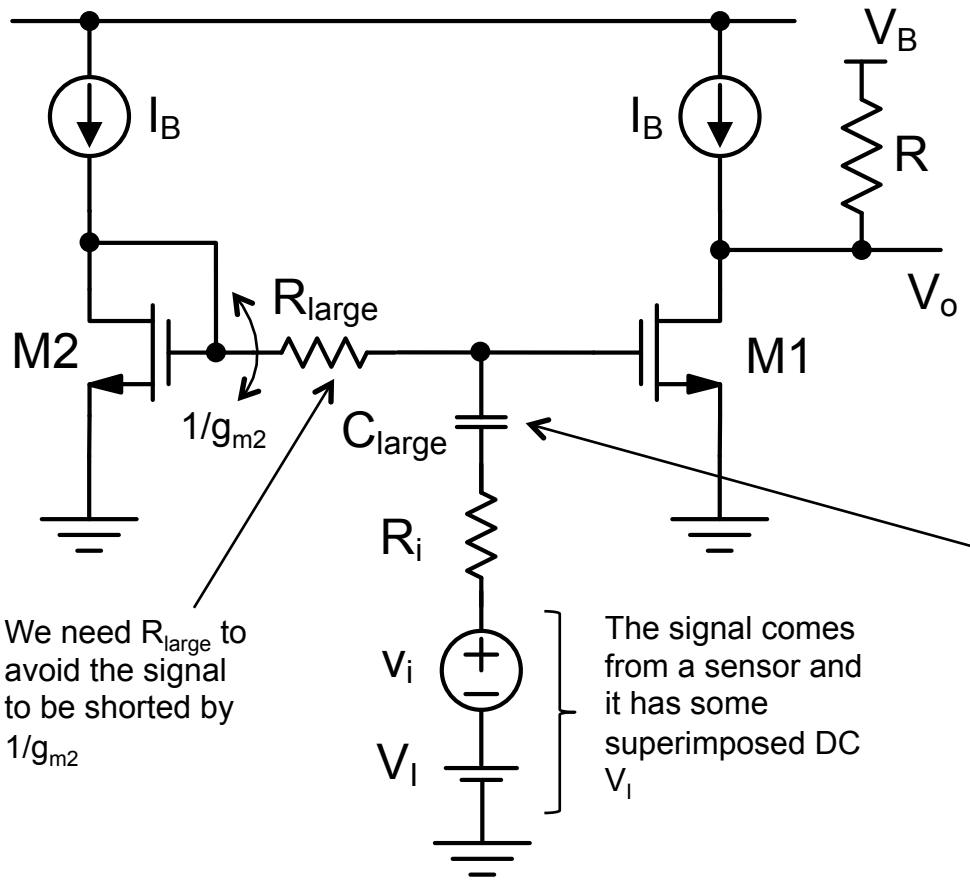
```
*** .op output (fast, -20degC)
 element     0:m1         0:m2
 region      Saturati     Saturati
  id        548.8001u    500.0000u
  vgs         1.1662       1.1662
  vds         2.2560       1.1662
  vth       402.0530m    402.0530m
  beta        1.8798m      1.7127m
  gm          1.4364m      1.3087m
  gds        44.7781u     44.7781u
...
```

Remaining Issue with first cut solution

- What if we do not have access to the "−" node of the input transducer?
  - Consider e.g. a sensor or another amplifier that produces a ground referenced signal with "arbitrary" quiescent voltage



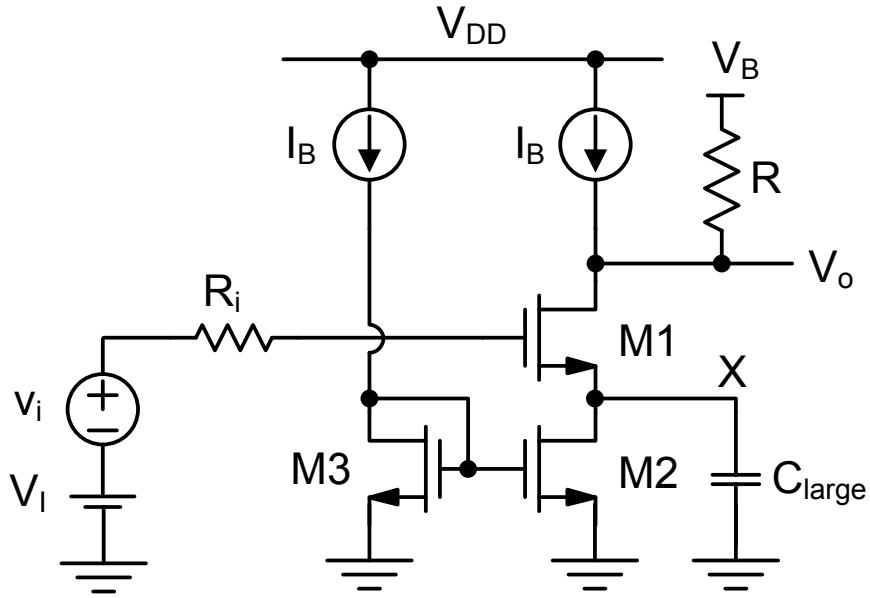
Second Attempt: Replica Biasing with AC Coupling



- Issues
  - Don't like R_{large}, C_{large} in integrated circuits
  - R_i and R_{large}(+1/gm2) form a resistive divider
    - Problematic if R_i is large

Another Idea: Third Attempt

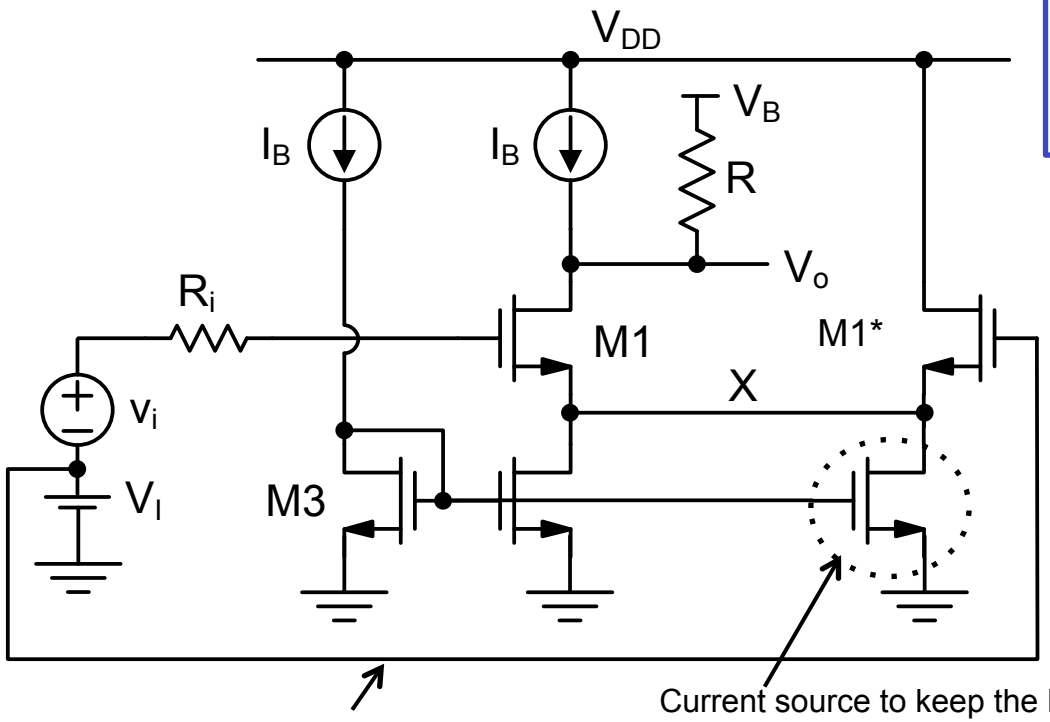
- Draw I_B out of M_1 source
  - Quiescent point voltage at node X changes over process, temperature, but M_1 current stays roughly constant (thanks to the M_3-M_2 mirror)
    - The DC voltage at the node G1 can move around without causing an issue as long as the moving around of V_{G1} is absorbed by V_X (=V_{DS2})
  - Make C_{large} large enough to essentially provide a "short" to ground at minimum desired input frequency



- Issue: Don't like C_{large} … (but without we would kill the gain:
  $|A_V| \sim g_{m1}R/(1+g'_{m1}r_{o2})$

Yet Another Idea (A really good one): Forth Attempt

- Instead of AC shorting node X with a cap. why not use another MOSFET (M1*) to provide low impedance at node X.
- As before, circuit is insensitive to changes in V_I and transistor V_T
  - No large caps or resistors needed to accomplish this!



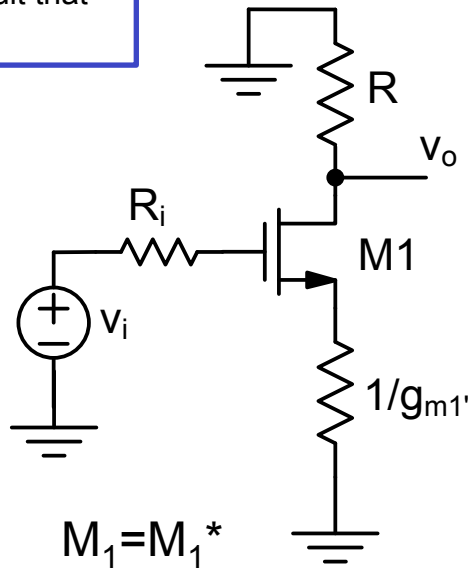
"recycle" V_I to bias the gate of M1*

Current source to keep the DC current through M1* roughly constant

The price is we lost $0.5g_m$ (Not too bad given the alternative: a circuit that doesn't work !)

$$A_V \cong -\frac{g_{m1}}{2}R$$

ac equivalent



$M_1=M_1^*$

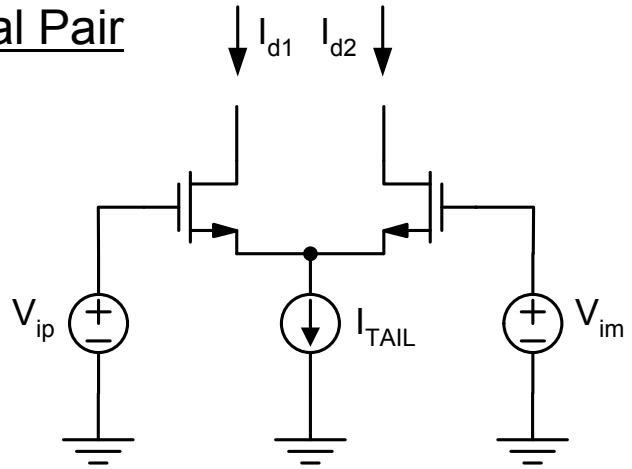
$g_{m1'}=g_{m1}+g_{mb1}$

Comments on the “Improved CS” Solution

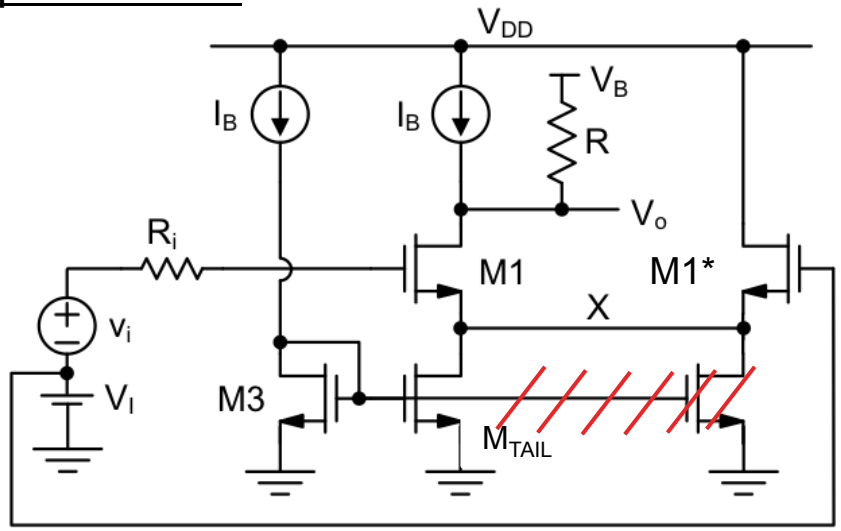
- The structure we arrived to “improve” the CS is so good that it has its own name***: Differential Pair***
- The Differential Pair main feature is to evaluate the difference between two voltages
  - In our “improved CS” the two voltages are V_I and V_I+v_i
  - To first order changes in V_I and process and temperature do not affect the output voltage

Differential Pair vs. "Improved CS" stage

Differential Pair



"Improved CS"



- Differences:
  - We do not necessarily need the second bottom transistor

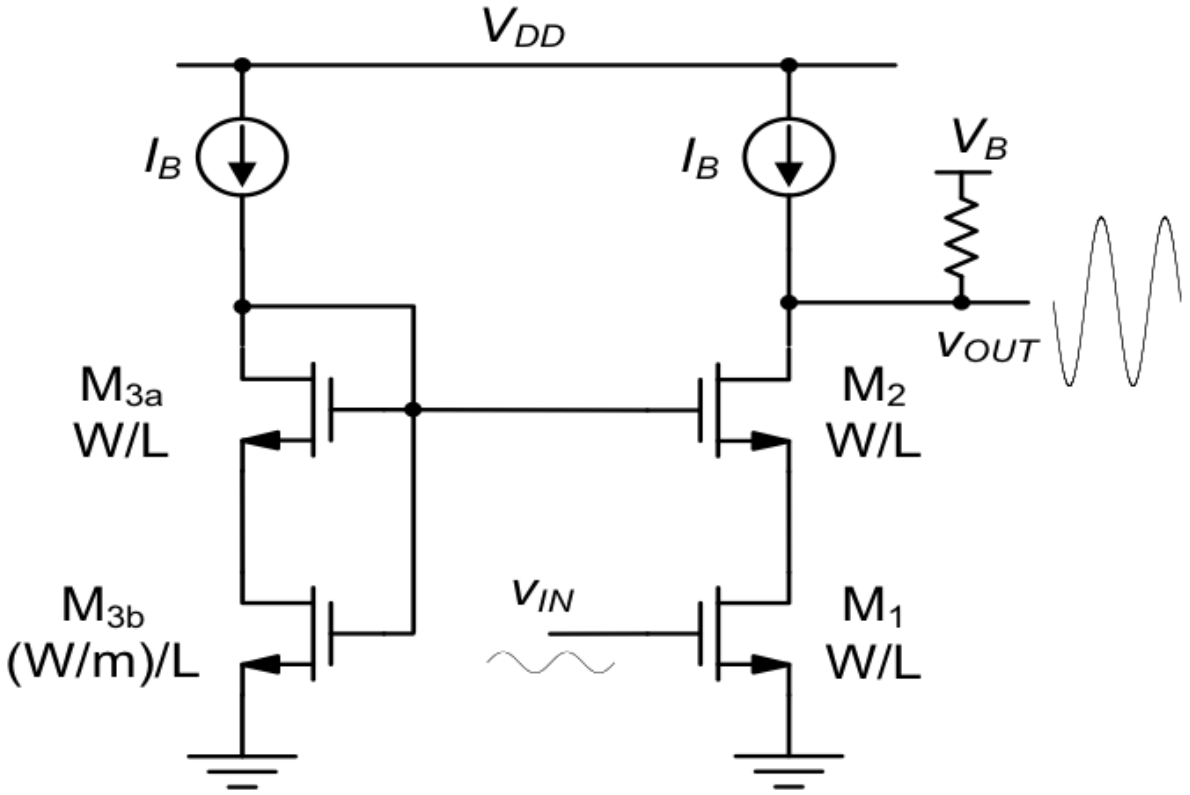
    $$I_{M1}=I_{M1*}=I_{TAIL}/2$$
  - We usually put signal both at the gate of M1 and at the gate of M1*

Voltage Biasing for a CG stage (1)

- Compared to a CS stage, setting up the bias voltage for the gate of a CG stage is usually less intricate

Example 1 – Cascode Stage

Source: B. Murmann Textbook p. 137

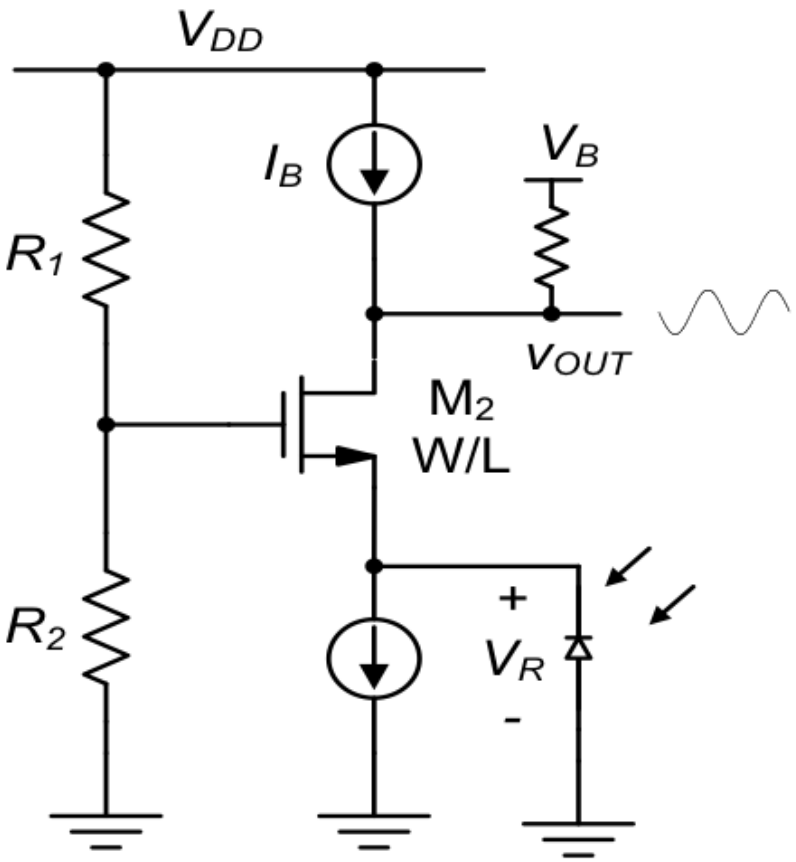


m = 5 → V_{DS1} = 1.45 V_{OV}

Voltage Biasing for a CG stage (2)

Example 2 – CG stage interfacing a Photodiode

Source: B. Murmann Textbook p. 137

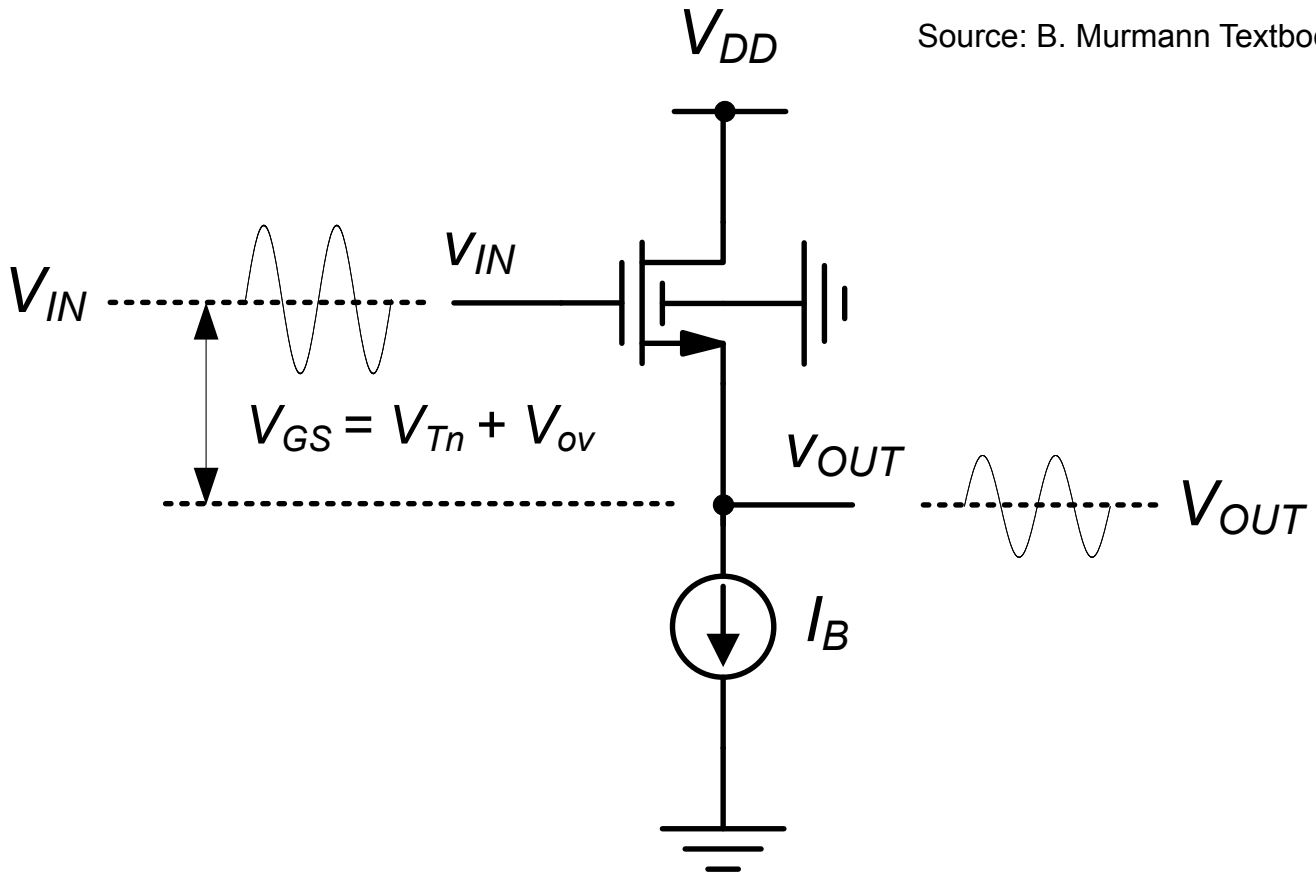


- In this circuit the output swing is usually not very large, and thus the bias voltage V_{G2} is not tightly constrained by voltage swing requirements.
- Typically, V_{G2} is set such that the photodiode is biased at a suitable reverse bias. This is accomplished by sizing R_1 and R_2 properly.

R_1 and R_2 are AC shorted (G_2 is at AC ground)

Voltage Biasing for a CD stage (1)

- In a CD stage the input and output voltage bias are directly coupled
- Proper voltage biasing in a CD stage boils down to making sure that the input and output bias voltages are compatible with the circuits that are connecting to.

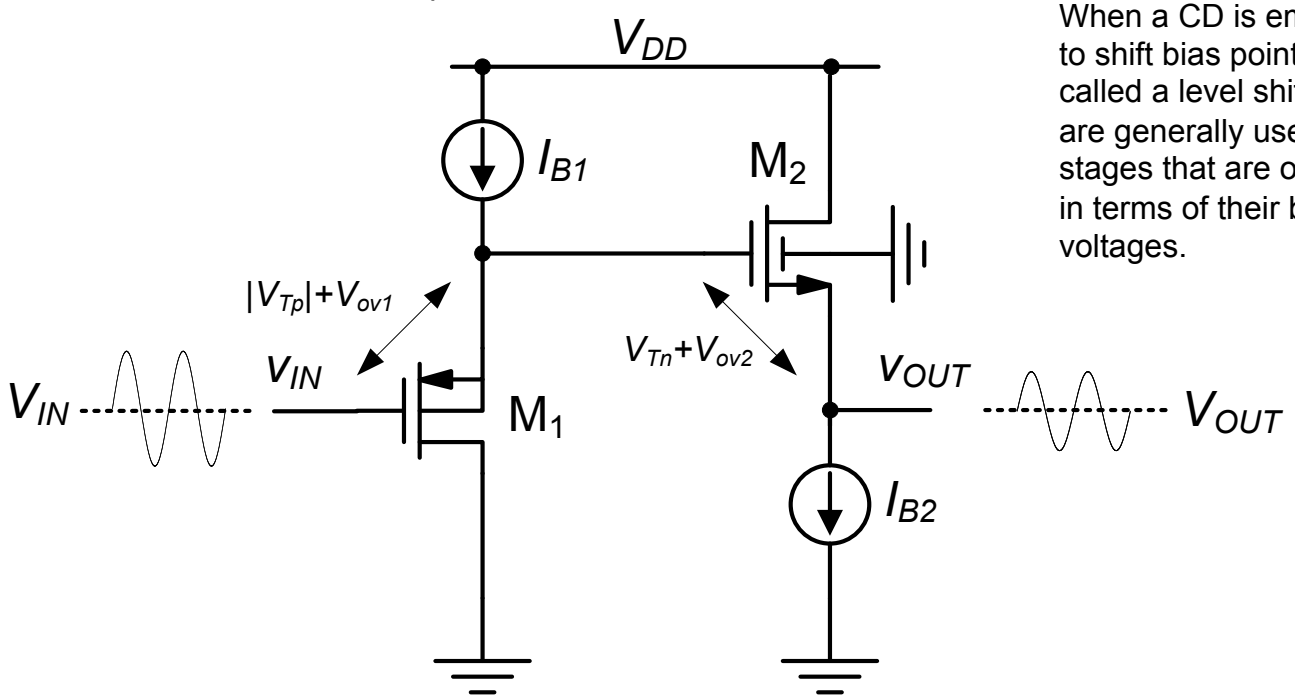


Source: B. Murmann Textbook p. 138

Voltage Biasing for a CD stage (2)

- In some application, the shift between the input and output bias is undesired. In this case a p-MOS CD stage can be used to provide a shift in the opposite direction
- M_1 can be sized such that the bias voltages V_{IN} and V_{OUT} are approximately the same

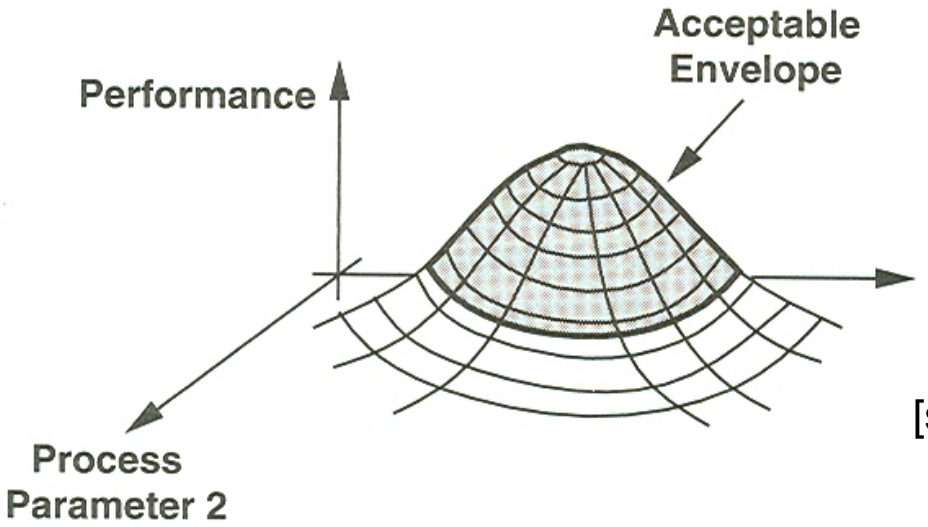
Source: B. Murmann Textbook p. 139



When a CD is employed primarily to shift bias points the circuit is called a level shifter. Level shifters are generally useful to interface two stages that are otherwise incompatible in terms of their bias input/output voltages.

The Challenge for Circuit Designers

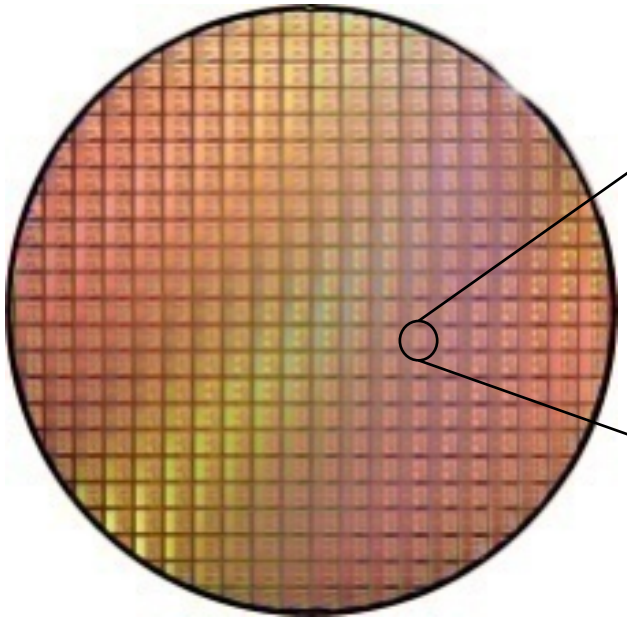
- Making sure that the circuit is biased properly across all possible conditions
  - And also maintain a set of performance specs (gain, bandwidth, power dissipation, …) in presence of parameter variations

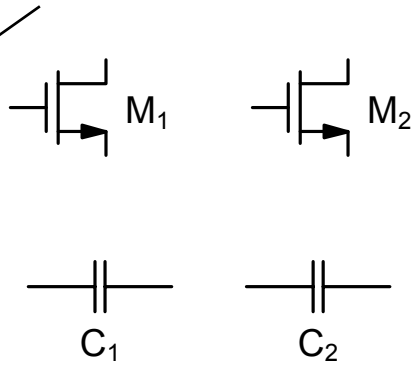


[source Razavi, p. 599]

Mismatch

- Upon closer inspection, device parameters not only vary from lot-to-lot or wafer-to-wafer, but there are also differences between closely spaced, nominally identical devices on the same chip (local variations)
  - These differences are called mismatch





$$V_{T1} - V_{T2} = \Delta V_T$$

$$\left(\mu C_{ox}\frac{W}{L}\right)_1 - \left(\mu C_{ox}\frac{W}{L}\right)_2 = \Delta\beta$$

$$C_1 - C_2 = \Delta C$$

source: R. Dutton, B. Murmann

Statistical Model

- Experiments over the past decades have shown that mismatches in device parameters (ΔV_T, ΔC, …) are typically "random" and well-described by a Gaussian distribution
  - With zero mean and a standard deviation that depends on the process and the size of the device
- Empirically, the standard deviation of the mismatch between two closely spaced devices can be modeled using the following expression

$$\sigma_{\Delta X} = \frac{A_X}{\sqrt{WL}}$$

where WL represents the area of the device, and X is the device parameter under consideration

Example of Coefficients for 1 µm Technology

Parameter	Value
A_{Vt}	20 mV-µm
$A_{\Delta\beta/\beta}$	2 %-µm
$A_{\Delta C/C}$ (Poly-Poly2 capacitor)	2.5 %-µm
$A_{\Delta R/R}$ (Poly2 resistor)	10 %-µm

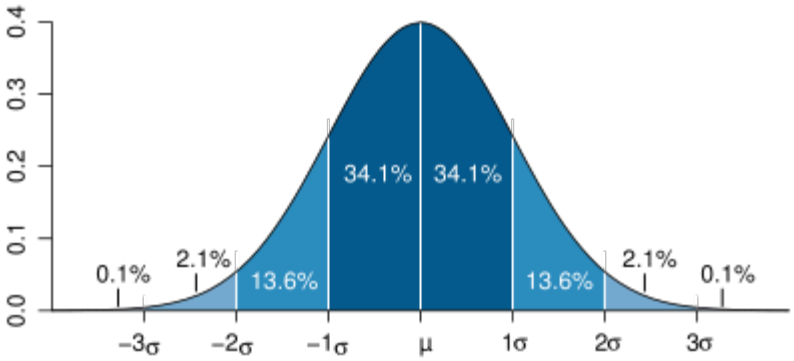
source: R. Dutton, B. Murmann

Example

- Example: MOSFET with W= 20μm, L=1μm

$$\sigma_{\Delta V_t} = \frac{20mV}{\sqrt{20}} = 4.5mV \qquad \sigma_{\frac{\Delta\beta}{\beta}} = \frac{2\%}{\sqrt{20}} = 0.45\%$$

http://en.wikipedia.org/wiki/Image:Standard_deviation_diagram.svg



$$3\sigma_{\Delta V_t} = 13.5mV$$

$$3\sigma_{\frac{\Delta\beta}{\beta}} = 1.35\%$$