Common Drain Stage
(Source Follower)

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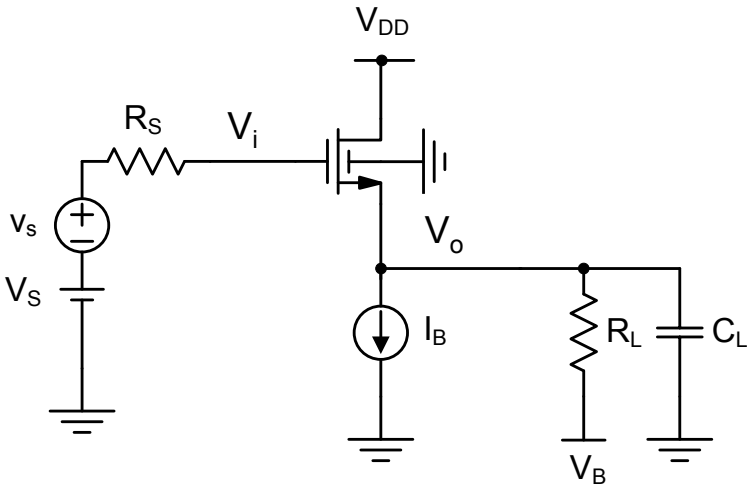
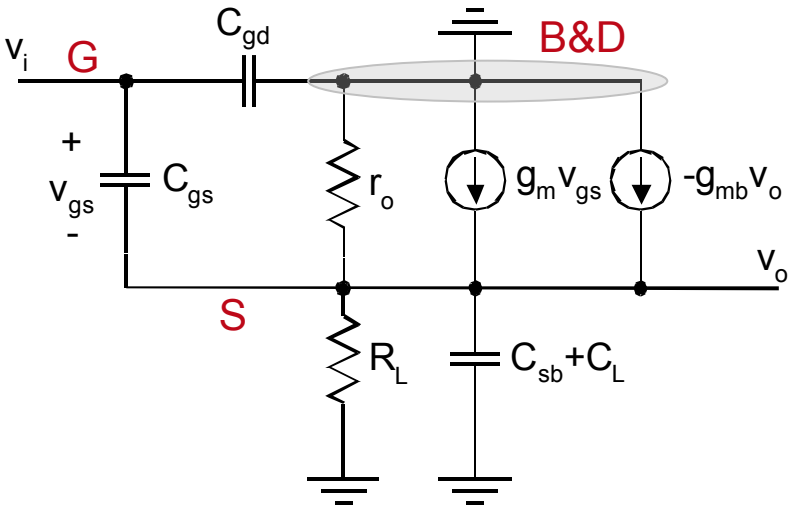
Common Drain Stage

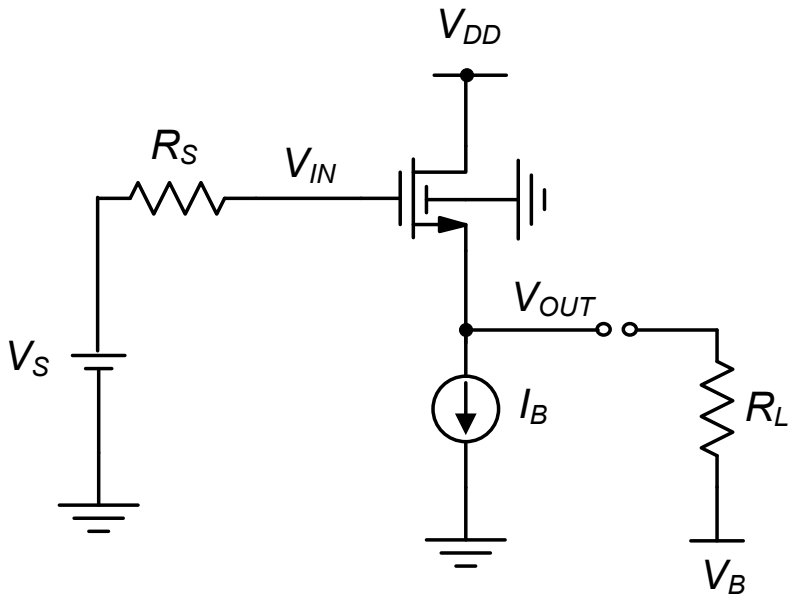


$$v_{gs} = v_i - v_o$$

$$v_{bs} = -v_o$$



CD Bias Point



- Assume $V_B=V_{OUT}$, so $I_D=I_B$

$$V_{OUT} = V_{IN} - V_{GS}$$

$$V_{GS} = V_T + \sqrt{\frac{I_D}{0.5C_{OX}W/L}}$$

$$V_T = V_{T0} + \gamma\left(\sqrt{PHI + V_{OUT}} - \sqrt{PHI}\right)$$

$$V_{DS} = V_{DD} - V_{OUT} = V_{DD} - V_{IN} + V_{GS}$$

- For M_1 to be in saturation

$$V_{DS} > V_{OV} = V_{GS} + V_T$$

$$\Updownarrow$$

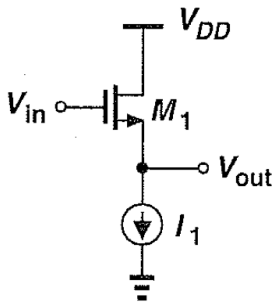
$$V_{DD} - V_{IN} + V_{GS} > V_{GS} + V_T$$

$$\Updownarrow$$

$$V_{IN} < V_{DD} + V_T$$

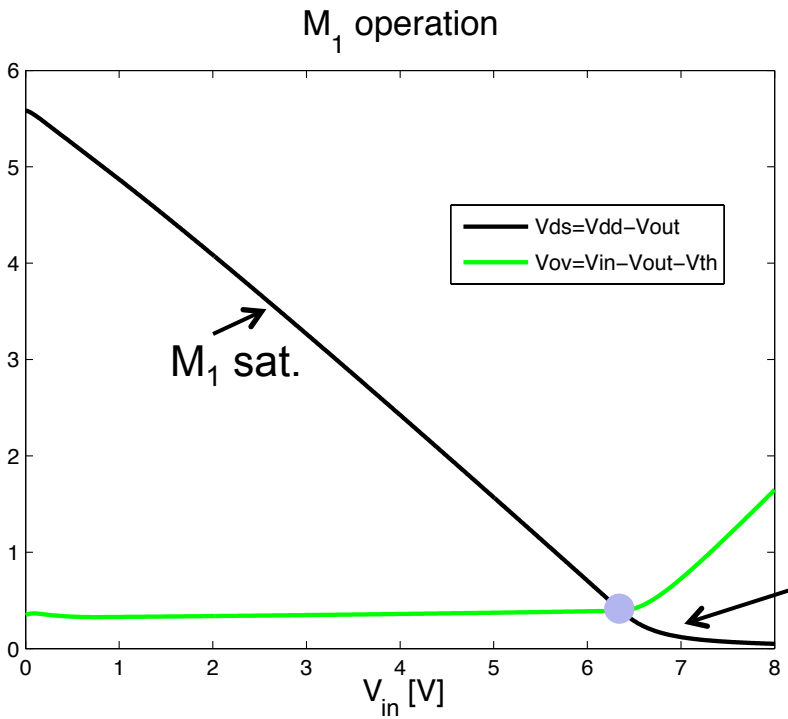
This is almost always the case in practical realizations

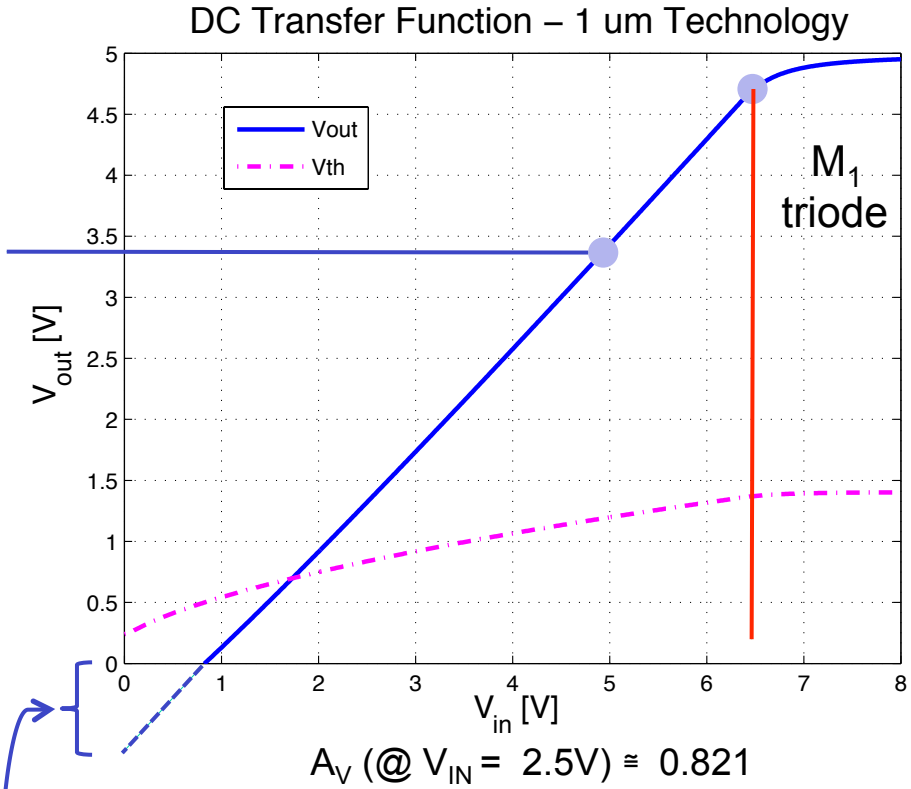
I/O DC characteristic (1)



Source: Razavi

Example:
V_{IN} = 2.5V; I_1=400μA;
V_{DD}=5V; W/L=100μm/1μm



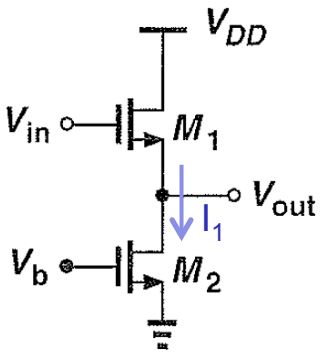


A_V (@ V_{IN} = 2.5V) ≅ 0.821

Math "artifact" due to ideal current source (a current source can take any voltage value across it !!)

- $V_{out}(min) \approx 0$
- $V_{out}(max) \approx V_{DD}-V_{th}$

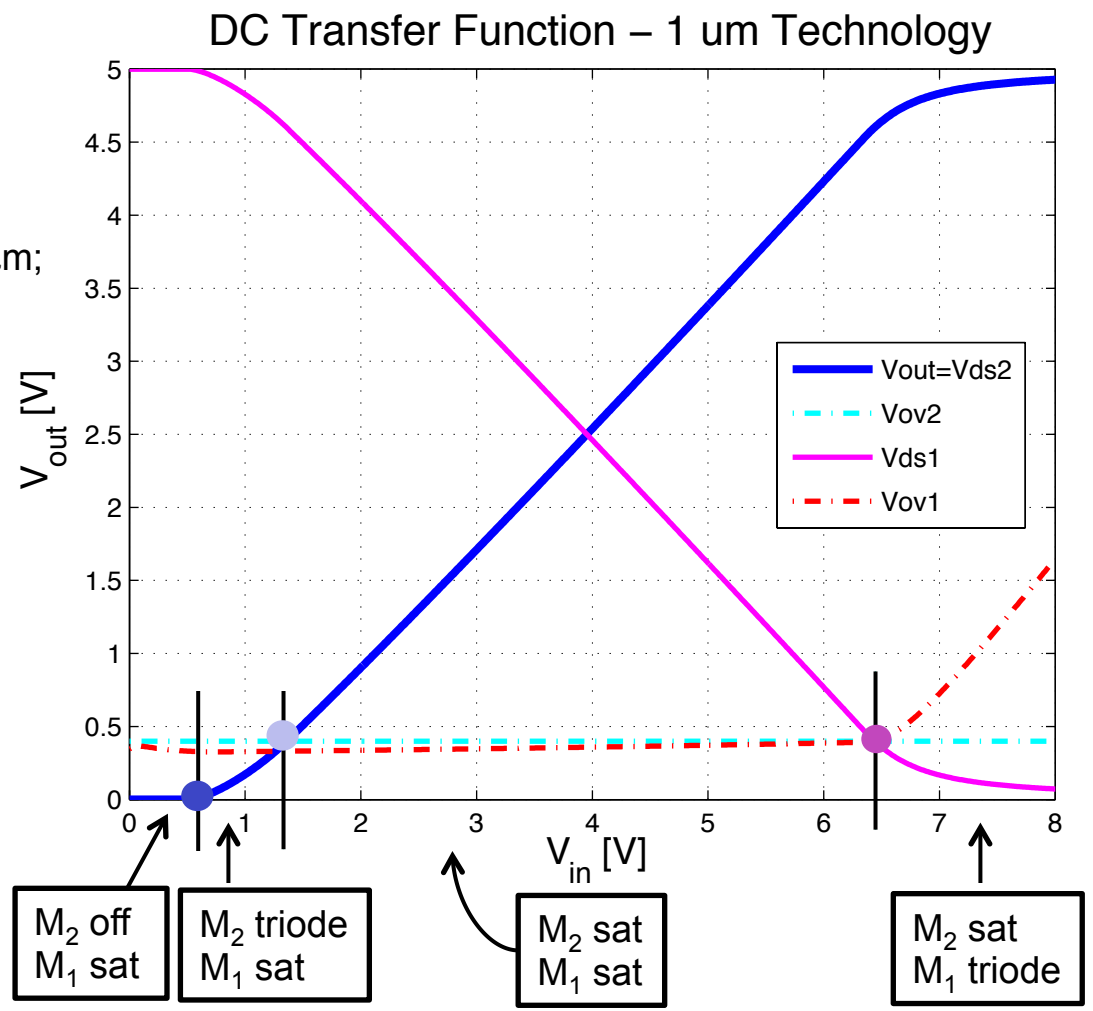
I/O DC characteristic (2)



Example:
V_{IN} = 2.5V;
I_1=400μA;
V_{DD}= 5V;
V_B = 0.9V;
W/L=100μm/1μm;

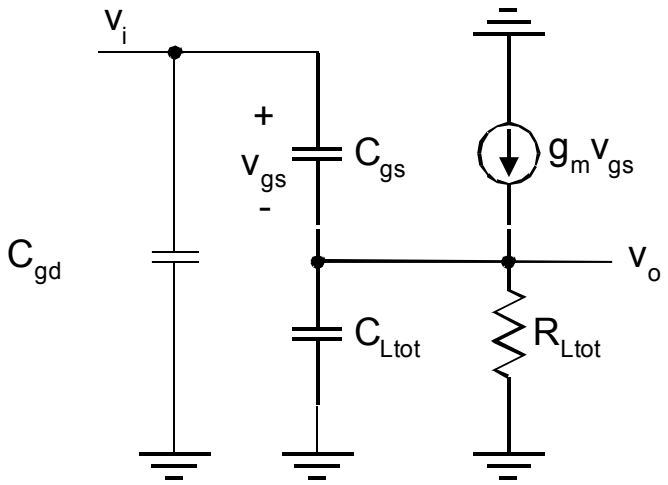
element	0:m1	0:m2
model	0:simple_n	0:simple_n
region	Saturati	Saturati
id	452.1261u	452.1261u
ibs	-13.0315f	0.
ibd	-50.0000f	-13.0315f
vgs	1.1968	900.0000m
vds	3.6968	1.3032
vbs	-1.3032	0.
vth	833.4784m	500.0000m
vdsat	363.3703m	400.0000m
vod	363.3703m	400.0000m
beta	6.8484m	5.6516m
gam eff	600.0000m	600.0000m
gm	2.4885m	2.2606m
gds	33.0095u	40.0000u
gmb	514.7852u	758.2384u
cdtot	72.3963f	93.2122f
cgtot	256.5245f	256.4846f
cstot	246.1466f	286.3341f
cbtot	66.1318f	128.5634f
cgs	203.3341f	203.3341f
cgd	51.1337f	50.3996f

```
* measurement
av0= 808.9285m
```



- Reduced output (and input) swing
  - $V_{out}(max) = V_{DD} - V_{OV1}$
  - $V_{out}(min) = V_{OV2}$

CD Voltage Transfer



$$v_o\left(sC_{Ltot}+sC_{gs}+\frac{1}{R_{Ltot}}\right)-v_i sC_{gs}-g_m\left(v_i-v_o\right)=0$$

$$\frac{v_o}{v_i}=\frac{g_m+sC_{gs}}{g_m+sC_{gs}+sC_{Ltot}+\frac{1}{R_{Ltot}}}$$

LHP zero

$$\frac{v_o}{v_i}=\frac{g_m}{g_m+\frac{1}{R_{Ltot}}}\cdot\frac{1+\frac{sC_{gs}}{g_m}}{1+\frac{s\left(C_{gs}+C_{Ltot}\right)}{g_m+\frac{1}{R_{Ltot}}}}=$$

$$=a_{v0}\cdot\frac{1-\frac{s}{z}}{1-\frac{s}{p}}$$

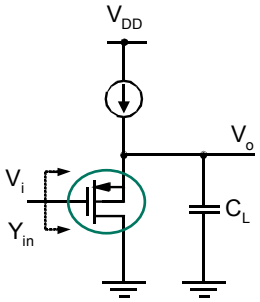
$$C_{Ltot}=C_L+C_{sb}\qquad R_{Ltot}=R_L\,||\,\frac{1}{g_{mb}}\,||\,r_o$$

often $R_{Ltot}\cong 1/g_{mb}$

Low Frequency Gain

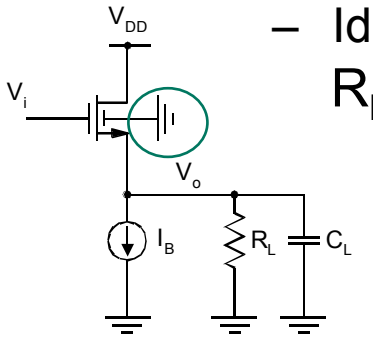
$$a_{v0} = \frac{g_m}{g_m + \frac{1}{R_{Ltot}}} \qquad R_{Ltot} = R_L \,||\, \frac{1}{g_{mb}} \,||\, r_o$$

- Interesting cases
  - Ideal current source; PMOS with source tied to body; no load resistor; $R_L=\infty$, $r_o=\infty$, $g_{mb}= 0$



$$\boxed{a_{v0} = 1}$$

  - Ideal current source; NMOS; no load resistor; $R_L=\infty$, $r_o=\infty$, $g_{mb}\neq 0$

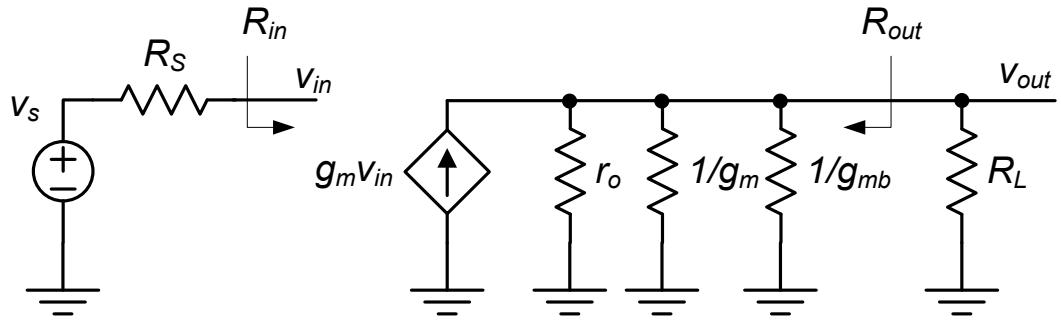


$$\boxed{a_{v0} = \frac{g_m}{g_m + g_{mb}}}$$ (typically ≅ 0.8)

  - Ideal current source, PMOS with source tied to body; load resistor $r_o=\infty$, $g_{mb}=0$, R_L finite

$$\boxed{a_{v0} = \frac{g_m}{g_m + \frac{1}{R_L}}}$$

Low frequency input and output resistances



$$a_{v0} = g_m / (g'_m + 1/r_o + 1/R_L)$$

- $R_{in} = \infty$
- $R_{out} = r_o \,||\, (1/g'_m)$

High Frequency Gain

$$a_{v0} = \frac{g_m}{g'_m + 1/r_o + 1/R_L}$$

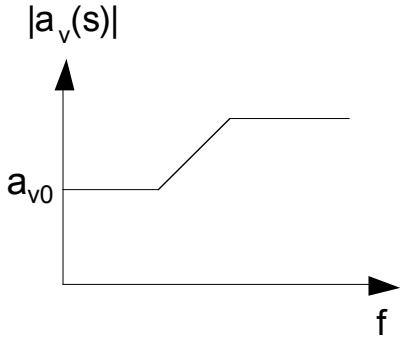
$$a_v(s) = \frac{v_o}{v_i} = a_{v0} \cdot \frac{1 - \frac{s}{z}}{1 - \frac{s}{p}}$$

$$z = -\frac{g_m}{C_{gs}}$$

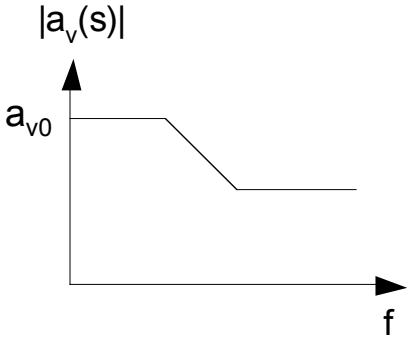
$$p = -\frac{g_m + \frac{1}{R_{Ltot}}}{C_{gs} + C_{Ltot}}$$

- Three scenarios:

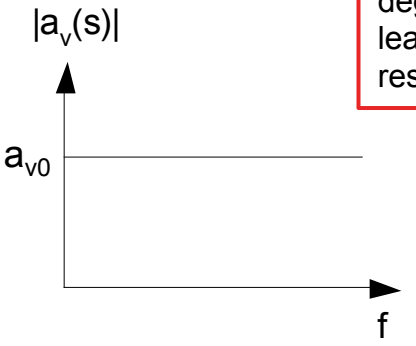
|z|<|p|



|z|>|p|



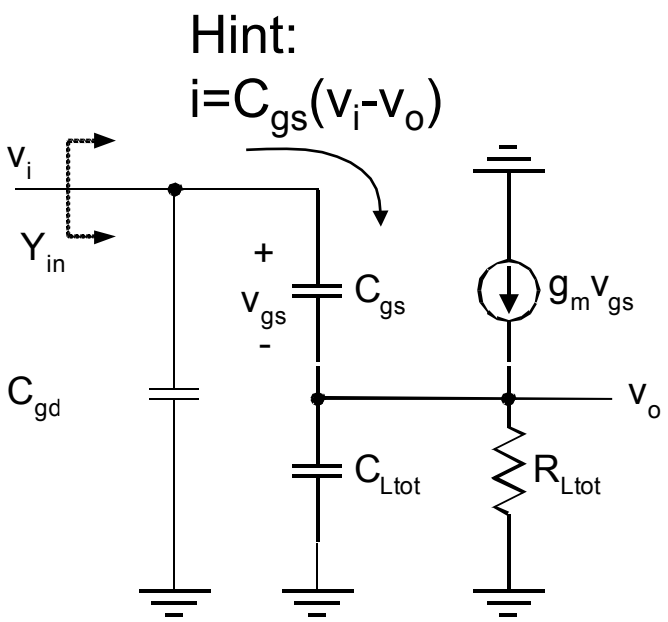
|z|=|p|



The presence of a LHP zero leads to the possibility that the pole and zero will provide some degree of cancellation, leading to a broadband response

(infinite bandwidth ?!?)

CD Input Impedance



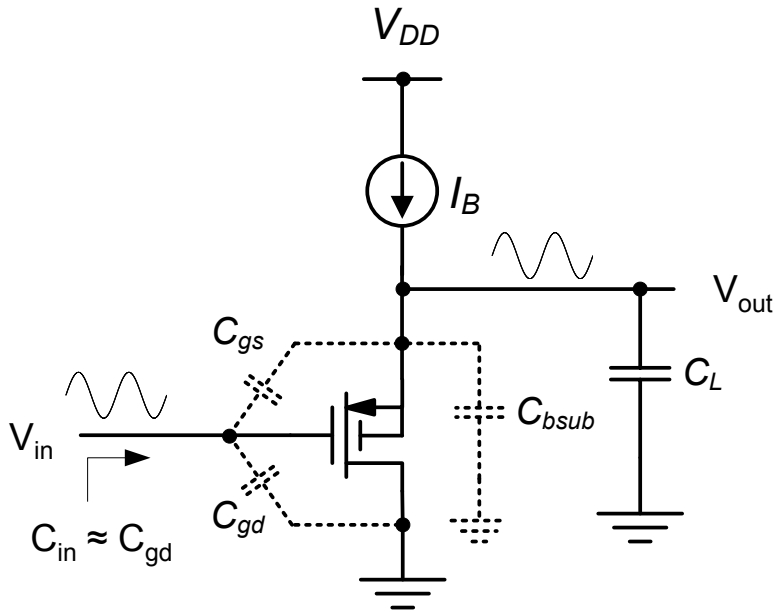
- By inspection:

Consistent with insight from Miller Theorem

$$Y_{in} = sC_{gd} + sC_{gs}\left(1 - a_v(s)\right)$$

- Gain term $a_v(s)$ is real and close to unity up to fairly high frequencies
- Hence, up to moderate frequencies, we see a capacitor looking into the input
  - A fairly small one, C_{gd}, plus a fraction of C_{gs}

CD input impedance for PMOS stage (with Body-source tie)



- g_{mb} generator inactive
  - Low frequency gain very close to unity

$g_m r_o >> 1$

$$a_{v0} = \frac{g_m}{g_m + \frac{1}{r_o}} \cong 1$$

- Very small input capacitance

$$Y_{in} = sC_{gd} + sC_{gs}\left(1 - a_v(s)\right)$$

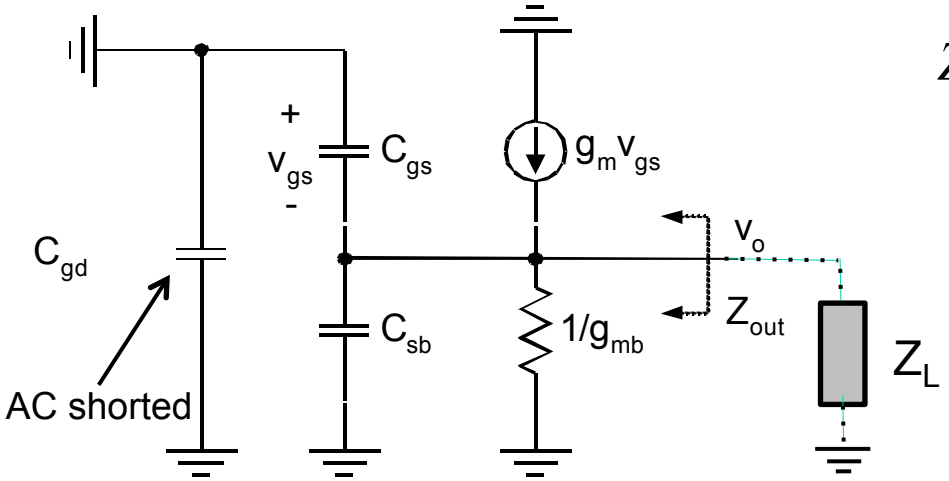
$$Y_{in} \cong sC_{gd}$$

for a_v=1 (V_{out}=V_{in}) no current flows through C_{gs}(perfect bootstrap)

- The well-body capacitance C_{bsub} can be large and may significantly affect the 3-db bandwidth

CD Output Impedance (1)

- Let's first look at an analytically simple case
  - Input driven by ideal voltage source



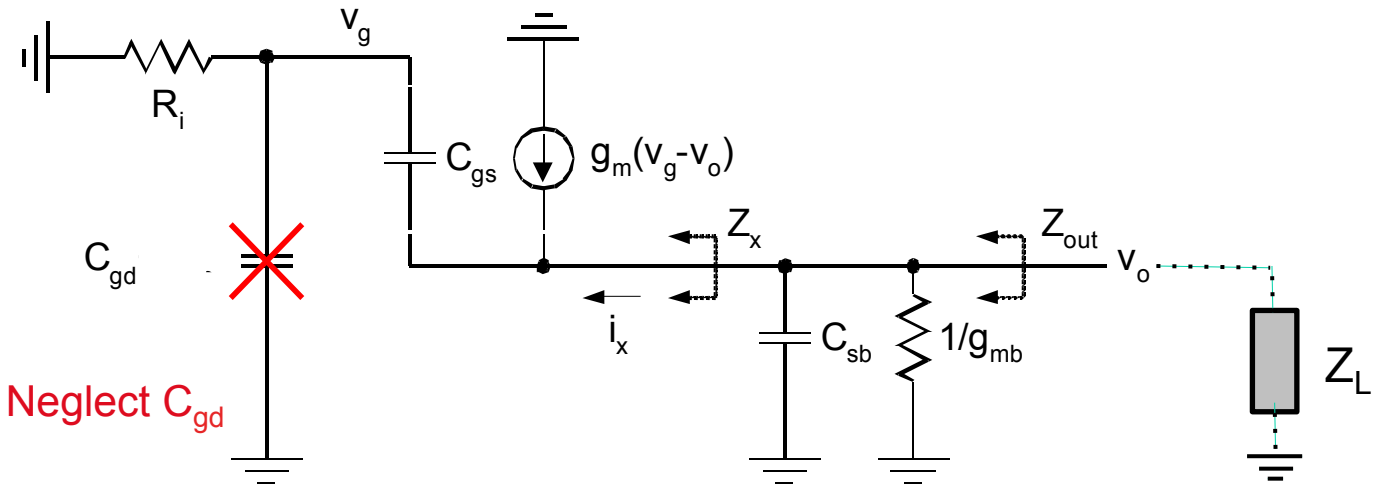
$$Z_{out} = \frac{1}{g_m + g_{mb}} \left\| \frac{1}{s\left(C_{gs} + C_{sb}\right)} \right.$$

$Y_L = sC_L + 1/R_L$

Low output impedance
- Resistive up to very high frequencies

CD Output Impedance (2)

- Now include finite source resistance



Neglecting C_{gd}

$$i_x = \left(v_o - v_g\right)\left(g_m + sC_{gs}\right) = v_o\left(1 - \frac{v_g}{v_o}\right)\left(g_m + sC_{gs}\right)$$

$$\frac{v_g}{v_o} \cong \frac{R_i}{\frac{1}{sC_{gs}} + R_i}$$

$$Z_x = \frac{v_o}{i_x} \cong \frac{1 + sR_iC_{gs}}{g_m + sC_{gs}} = \frac{1}{g_m}\left(\frac{1 + sR_iC_{gs}}{1 + \frac{sC_{gs}}{g_m}}\right)$$

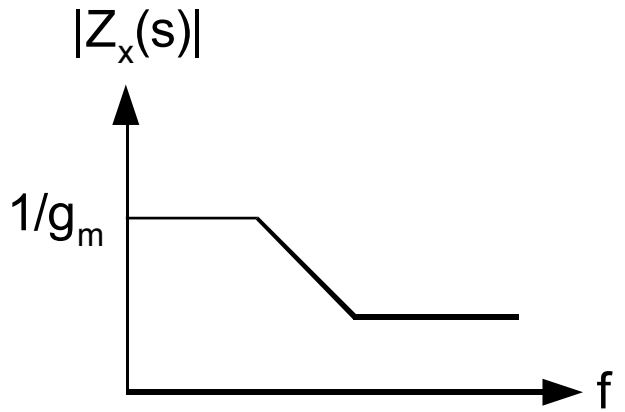
CD Output Impedance (3)

$$Z_x \cong \frac{1}{g_m}\frac{\left(1+sR_iC_{gs}\right)}{\left(1+\frac{sC_{gs}}{g_m}\right)}$$

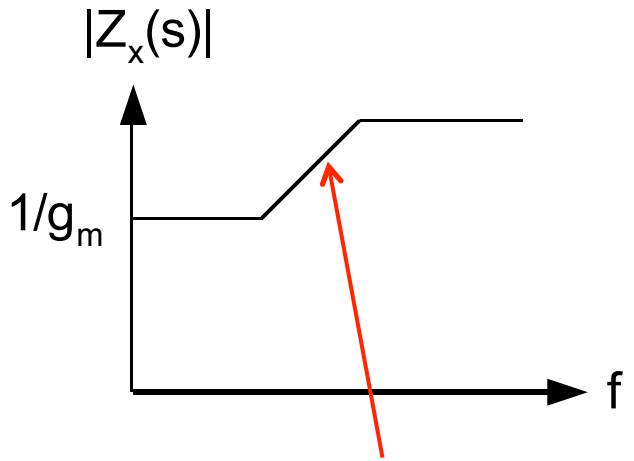
- Two interesting cases

NOTE:
Typically 1/gm is small,
so this can happen !!

$R_i < 1/g_m$



$R_i > 1/g_m$

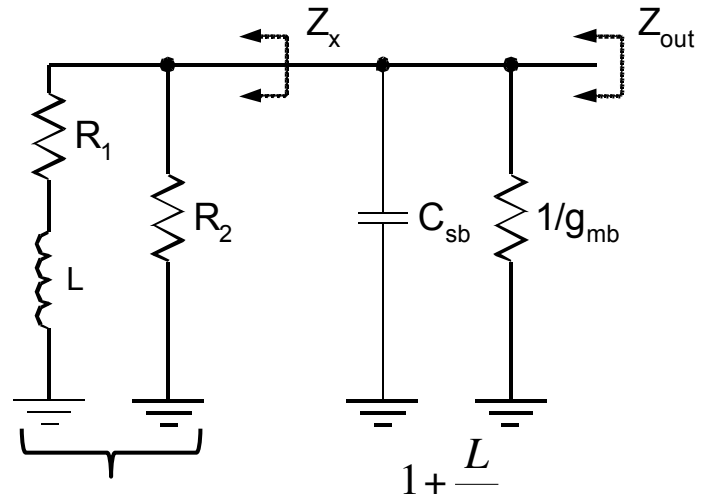


Inductive behavior!

Equivalent Circuit for $R_i > 1/g_m$

$$Z_x \cong \frac{1}{g_m}\frac{\left(1+sR_iC_{gs}\right)}{\left(1+\frac{sC_{gs}}{g_m}\right)}$$

$$for\ s=0 \Rightarrow Z_x = 1/g_m$$
$$for\ s\to\infty \Rightarrow Z_x = R_i$$



$$for\ s=0 \Rightarrow Z_x = R_1 \,||\, R_2$$
$$for\ s\to\infty \Rightarrow Z_x = R_2$$

$$R_1 \,||\, R_2 = \frac{1}{g_m}$$

$$R_2 = R_i$$

$$L = \frac{R_i^2 C_{gs}}{g_m R_i - 1}$$

$$Z_x = \frac{(R_1+sL)R_2}{R_1+R_2+sL} = \frac{R_1R_2}{R_1+R_2}\frac{1+\frac{L}{R_1}}{1+\frac{L}{R_1+R_2}}$$

- This circuit is prone to ringing!
  - L forms an LC tank with any capacitance at the output
  - If the circuit drives a large capacitance the response to step-like signals will result in ringing

Inclusion of Parasitic Input Capacitance*

What happens to the output impedance if we don't neglect $C_i=C_{gd}$?

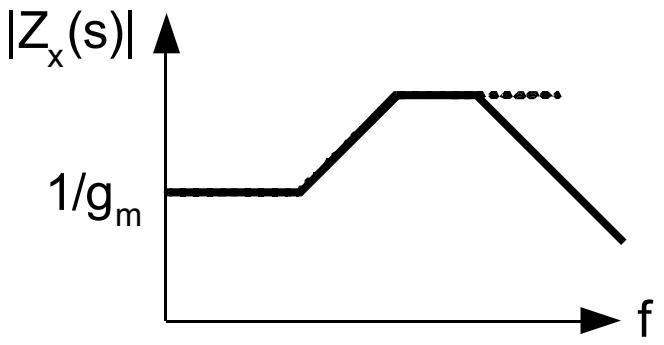
* Hint:
replace R_i with

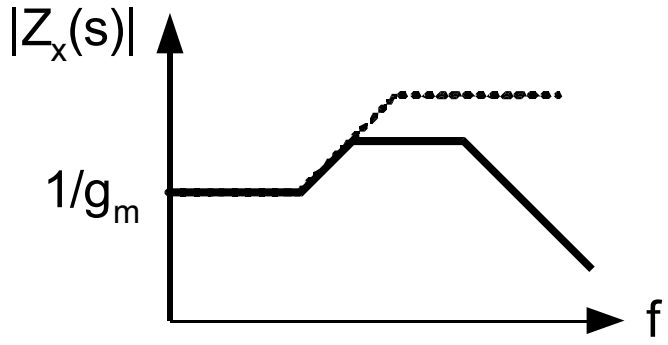
$$Z_i = \frac{R_i}{R_i + sC_iR_i}$$

$$Z_x = \frac{1}{g_m}\frac{\left(1+sR_i\left(C_{gs}+C_i\right)\right)}{\left(1+\frac{sC_{gs}}{g_m}\right)\left(1+sR_iC_i\right)}$$

$$\frac{1}{R_i\left(C_{gs}+C_i\right)} < \frac{g_m}{C_{gs}} < \frac{1}{R_iC_i}$$

$$\frac{1}{R_i\left(C_{gs}+C_i\right)} < \frac{1}{R_iC_i} < \frac{g_m}{C_{gs}}$$





Applications of the Common Drain Stage

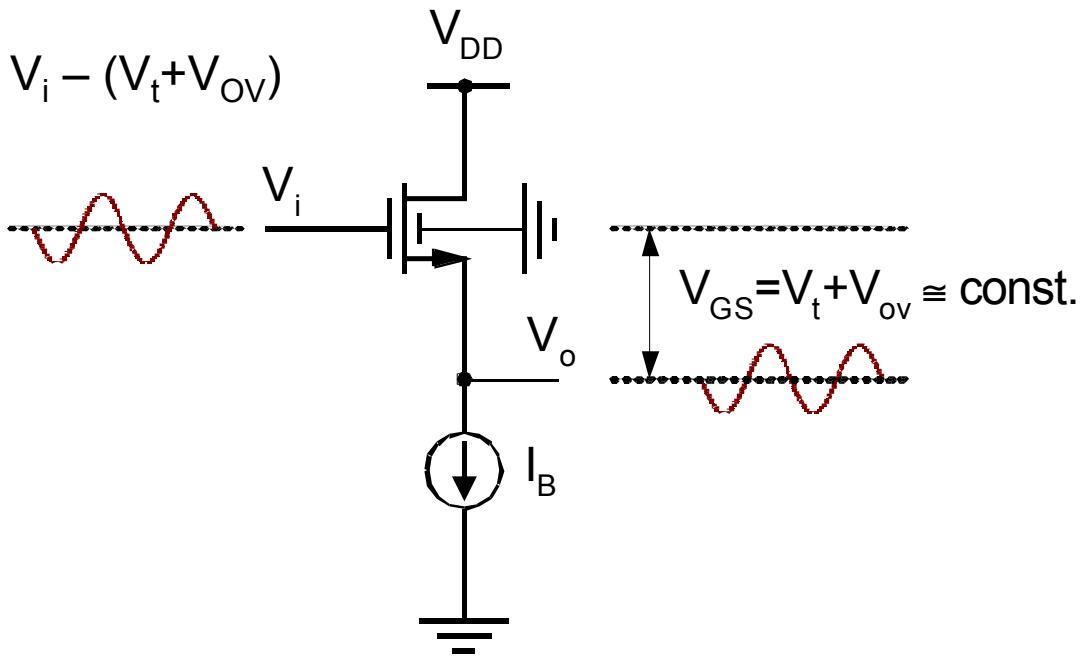
- Level Shifter
- Voltage Buffer
- Load Device

Application 1: Level Shifter

$V_i = V_{GS} + V_o$

$\updownarrow$

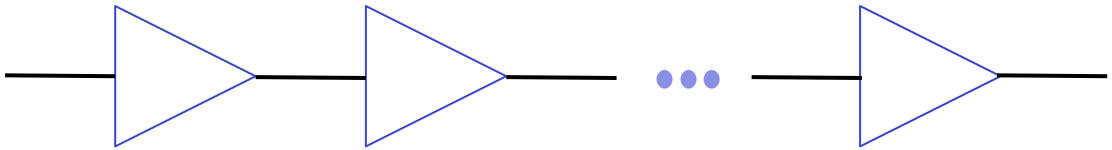
$V_o = V_i - V_{GS} = V_i - (V_t + V_{OV})$



- Output quiescent point is roughly V_t+V_{ov} lower than input quiescent point
- Adjusting the W/L ratio allows to “tune” Vov (= the desired shifting level)

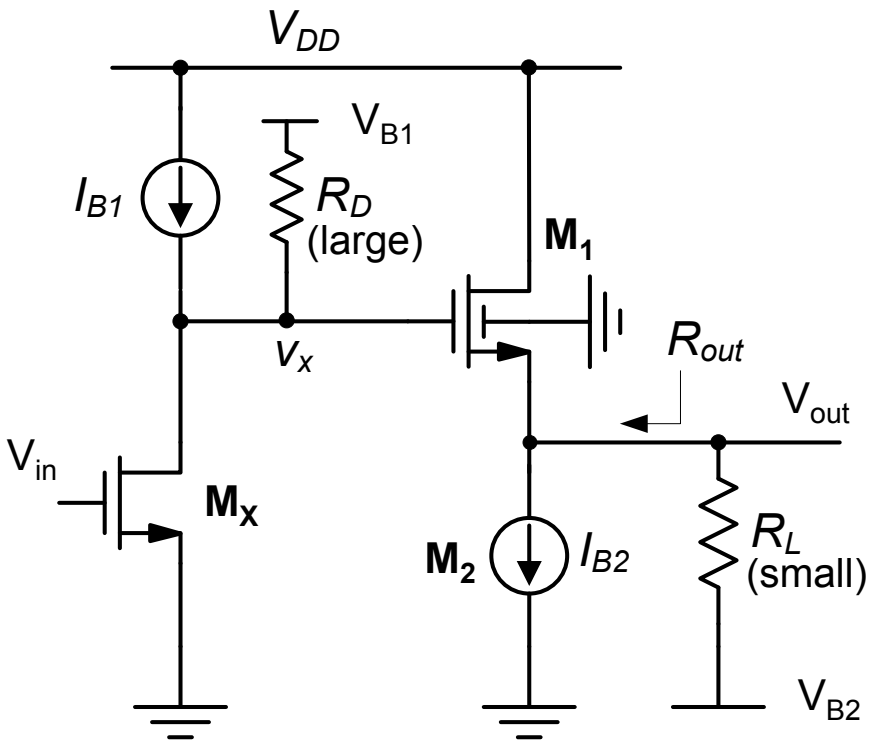
Why is lowering the DC level useful ?

- When building cascades of CS and CG amplifiers, as we move along the DC level moves up



- A CD stage is a way to buffer the signal, and moving down the DC level

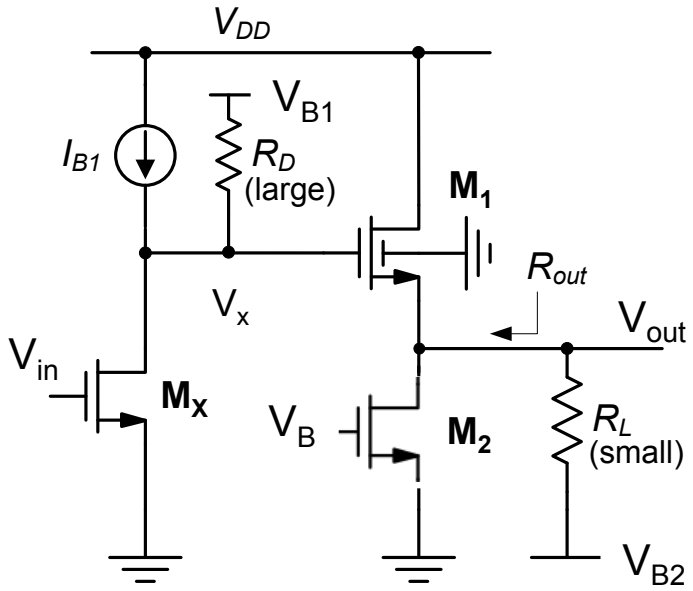
Application 2: Buffer



- Low frequency voltage gain of the above circuit is ~$g_m R_{big}$
  - Would be ~$g_m(R_{small}||R_{big})$ ~ $g_m R_{small}$ without CD buffer stage
- Disadvantage
  - Reduced swing

$$\begin{cases} V_{out}(\max) = V_{DD} - V_{OV1} \\ V_{out}(\min) = V_{OV2} \end{cases}$$

Buffer Design Considerations

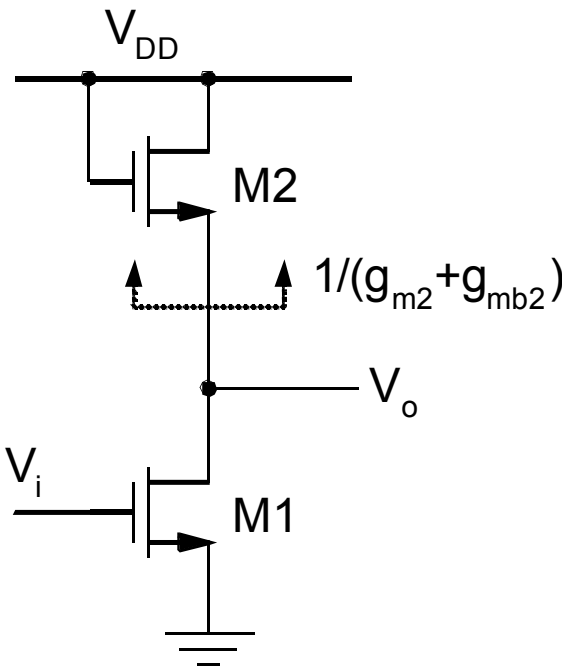


- Without the buffer the minimum allowable value of V_x for M_x to remain in saturation is:
  $V_X > V_{GSX} - V_{thx}$
- With the buffer for M_2 to remain in sat. it must be:
  $V_X > V_{GS1}+V_{GS2}-V_{th2}$

- Assuming the overdrive of M_x and M_2 are comparable this means that the allowable swing at X is reduced by V_{GS1} which is a significant amount ($V_{GS1}=V_{OV1}+V_{th1}$)

Application 3: Load Device

Looks familiar ? ➡ "CS stage with diode connected load"



$$a_{v0} = \frac{g_{m1}}{g_{m2} + g_{mb2}}$$

- Advantages compared to resistor load
  - "Ratiometric"
    - Gain depends on ratio of similar parameters
    - Reduced process and temperature variations
  - First order cancellation of nonlinearities
- Disadvantage
  - Reduced swing

$$V_{out}(\max) = V_{DD} - V_{th2}$$

$$V_{out}(\min) = V_{IN} - V_{th1} = V_{OV1}$$

CD stage Issues

- Several sources of nonlinearity
  - V_t is a function of V_o (NMOS, without S to B connection)

$$V_t = V_{t0} + \gamma\left(\sqrt{PHI + V_o} - \sqrt{PHI}\right)$$

  - I_D and thus V_{ov} changes with V_o
    - Gets worse with small R_L

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}\left(V_{GS} - V_t\right)^2$$

If we worry about distortion we need to keep $\Delta V_{in}/2V_{OV}$ small (→ we need large V_{OV}, and this affect adversely signal swing). If R_L is small, things are even worse because to obtain the desired ΔV_{out} we need more ΔV_{in} (and so even more V_{OV})

$$\frac{\Delta V_{out}}{\Delta V_{in}} \approx \frac{g_m}{g'_m + 1/R_L}$$ ← Small R_L means less gain

- Reduced input and output voltage swing
  - Consider e.g. V_{DD}=1V, V_t=0.3V, V_{OV}=0.2V ($V_{GS}=V_t+V_{ov}$=0.5V)
    - CD buffer stage consumes 50% of supply headroom!
  - In low V_{DD} applications that require large output swing, using a CD buffer is often not possible
  - CD buffers are more frequently used when the required swing is small
    - E.g. pre-amplifiers or LNAs that turn μV into mV at the output

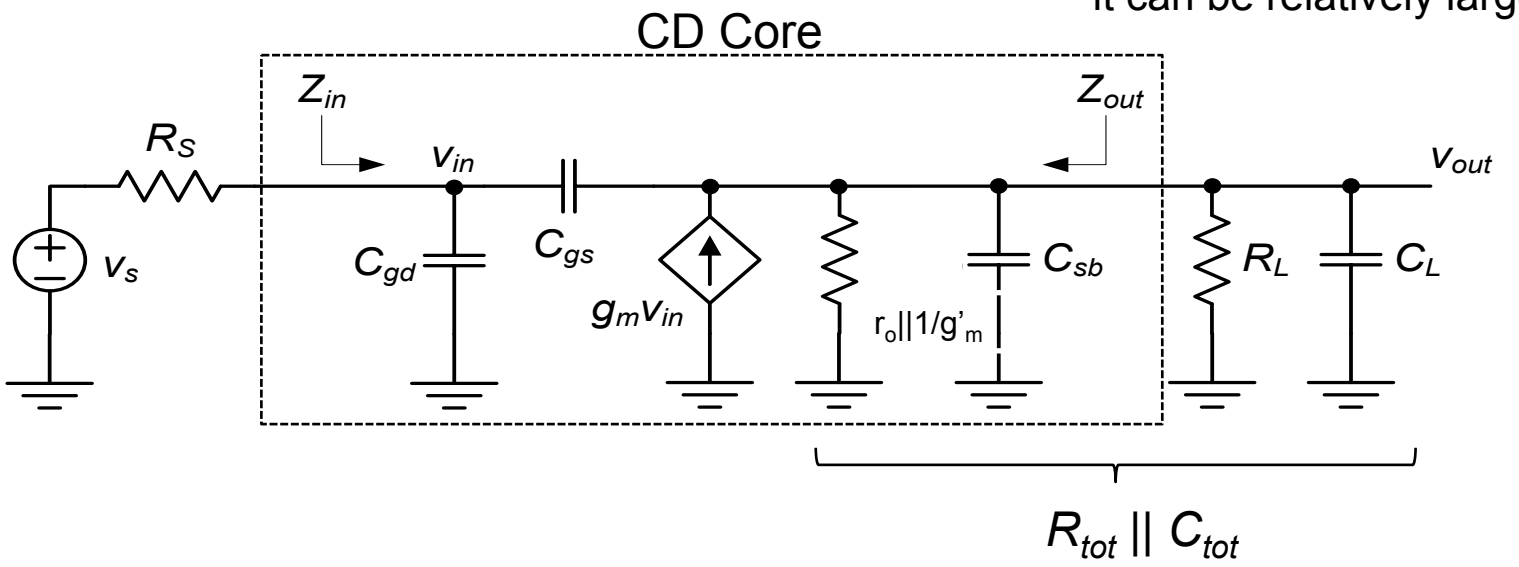
Summary – Elementary Transistor Stages

- Common source
  - VCCS, makes a good voltage amplifier when terminated with a high impedance
- Common gate
  - Typically low input impedance, high output impedance
  - Can be used to improve the intrinsic voltage gain of a common source stage
    - "Cascode" stage
- Common drain
  - Typically high input impedance, low output impedance
  - Great for shifting the DC operating point of signals
  - Useful as a voltage buffer when swing and nonlinearity are not an issue

CD Voltage Transfer Revisited (1)

- The driving circuit has a finite resistance R_s

example: if R_S is the output resistance of a CS stage it can be relatively large



- This model resembles the model of the CS stage
  - The main difference is in the polarity of the controlled source
  - This difference has profound impact on the Miller amplification of the capacitance coupling input and output

CD Voltage Transfer Revisited (2)

$$\frac{v_{out}}{v_s} = a_{v0} \cdot \frac{1 + s\dfrac{C_{gs}}{g_m}}{1 + b_1 s + b_2 s^2}$$

$$a_{v0} = g_m R_{tot}$$

$$b_1 = R_s C_{gs}(1 - a_{v0}) + R_S C_{gd} + R_{tot} C_{gs} + R_{tot} C_{tot}$$

$$b_2 = R_S R_{tot}(C_{gs} C_{gd} + C_{gs} C_{tot} + C_{gd} C_{tot})$$

- The zero in the transfer function is on the LHP and it occurs at approximately ω_T
- Unfortunately the high frequency analysis can become quite involved. A dominant real pole does not always exist, in fact poles can be complex. In the case the poles are complex a designer should be careful that the circuit does not exhibit too much overshoot and ringing.

CD Voltage Transfer Revisited (3)

$$\frac{v_{out}}{v_s} = a_{v0} \cdot \frac{1 + s\dfrac{C_{gs}}{g_m}}{1 + b_1 s + b_2 s^2} = a_{v0} \cdot \frac{1 + s\dfrac{C_{gs}}{g_m}}{1 + \dfrac{s}{\omega_0 Q} + \dfrac{s^2}{\omega_0^2}}$$

- Interesting cases:
  - A dominant pole condition exist $\longrightarrow$ $\omega_{3dB} \cong \dfrac{1}{b_1} \quad \left(b_1 = \sum \tau_j\right)$
  - Poles are complex

A dominant pole condition exist for: $Q^2 << 1/4$

$\Updownarrow$

$\dfrac{b_2}{b_1^2} << 1/4$

Poles Location

- Roots of the denominator of the transfer function: $1+\frac{s}{\omega_0 Q}+\frac{s^2}{\omega_0^2}=0$

- Complex Conjugate poles (overshooting in step response)

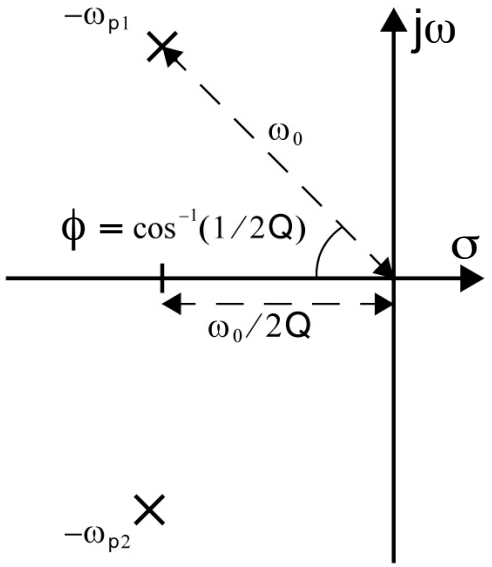
$$for \quad Q>0.5 \Rightarrow s_{1,2}=-\frac{\omega_0}{2Q}\left(1\pm j\sqrt{4Q^2-1}\right)$$

  - For Q = 0.707 (ϕ=45°), the −3dB frequency is ω_0 (Maximally Flat Magnitude or Butterworth Response)
  - For Q > 0.707 the frequency response has peaking

- Real poles (no overshoot in the step response)

$$for \quad Q\le 0.5 \Rightarrow s_{1,2}=-\frac{\omega_0}{2Q}\left(1\pm\sqrt{1-4Q^2}\right)$$

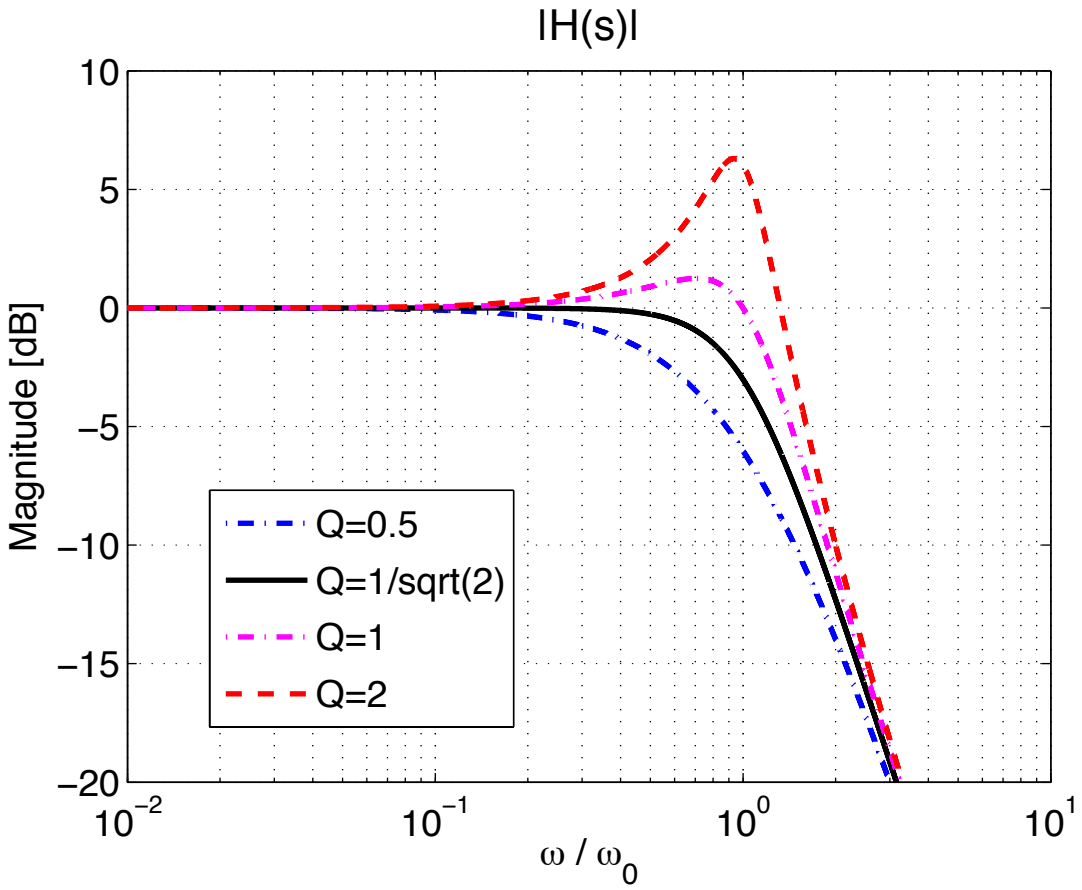
Poles location with Q> 0.5



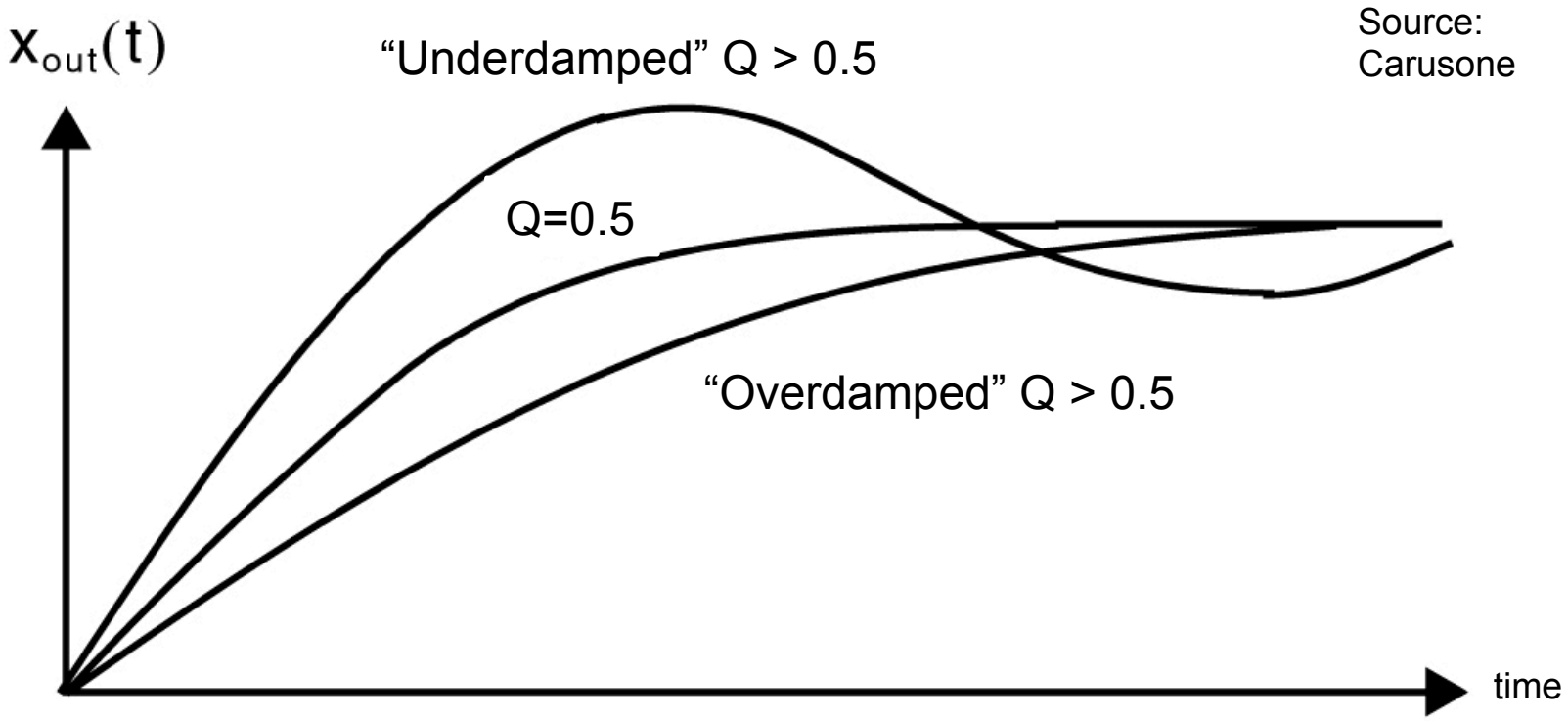
Source: Carusone

Frequency Response

$$H(s) = \frac{1}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}}$$



Step Response



- Ringing for Q > 0.5
- The case Q=0.5 is called maximally damped response (fastest settling without any overshoot)