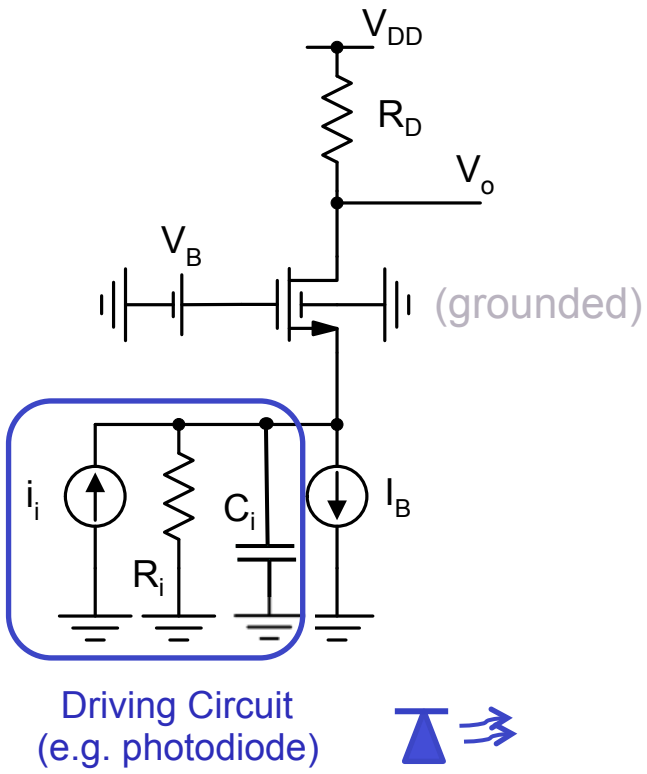
Common Gate Stage
Cascode Stage

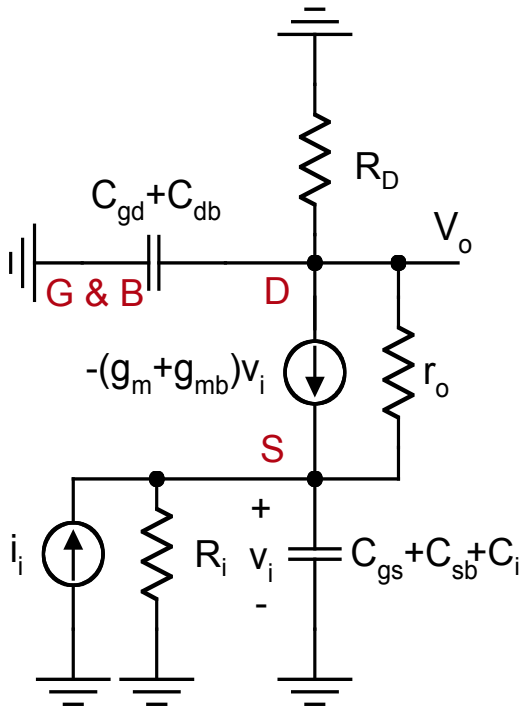
Claudio Talarico, Gonzaga University

Common Gate Stage

The overdrive due to V_B must be "consistent" with the current pulled by the DC source I_B



careful with signs:
$v_{gs} = v_{bs} = -v_i$



Define: $C_S = C_{gs} + C_{sb} + C_i$

$C_D = C_{gd} + C_{db}$

$g'_m = g_m + g_{mb}$

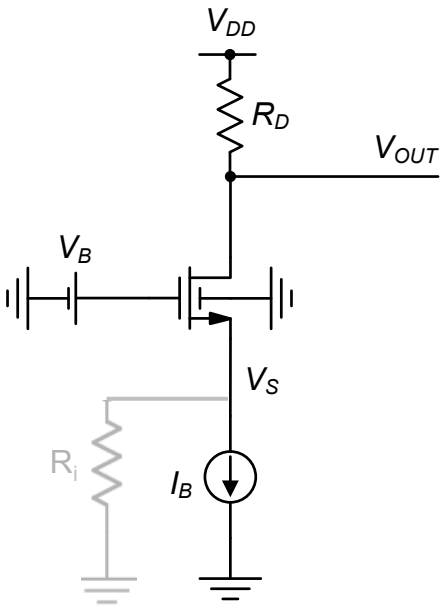
"enhanced" g_m' due to both "gates"

R_i models finite resistance in the driving circuit
C_i models parasitic capacitance in the driving circuit

Common Stage Bias Point Analysis

- Assume R_i is large: (very reasonable for a reverse biased photodiode)

$I_D \cong I_B$



$$I_B \cong I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS}-V_t)^2 \qquad V_t = V_{t0} + \gamma\left(\sqrt{PHI + V_{SB}} - \sqrt{PHI}\right)$$

$$V_{SB} = V_S$$

$$V_{OUT} = V_{DD} - R_D I_B$$

$$V_{GS} = V_t + \sqrt{\frac{I_B}{0.5\mu C_{OX} W/L}}$$

$$V_S = V_B - V_{GS} = V_B - V_t - \sqrt{\frac{I_B}{0.5\mu C_{OX} W/L}}$$

A precise solution requires numerical iterations. Since the dependency of V_t on V_S is weak a few iterations are satisfactory for hand calculation

Once V_S is computed we can check that M1 operates in saturation:

$$V_{DS} = V_{OUT} - V_S > V_{Dsat} = V_{GS} - V_t$$

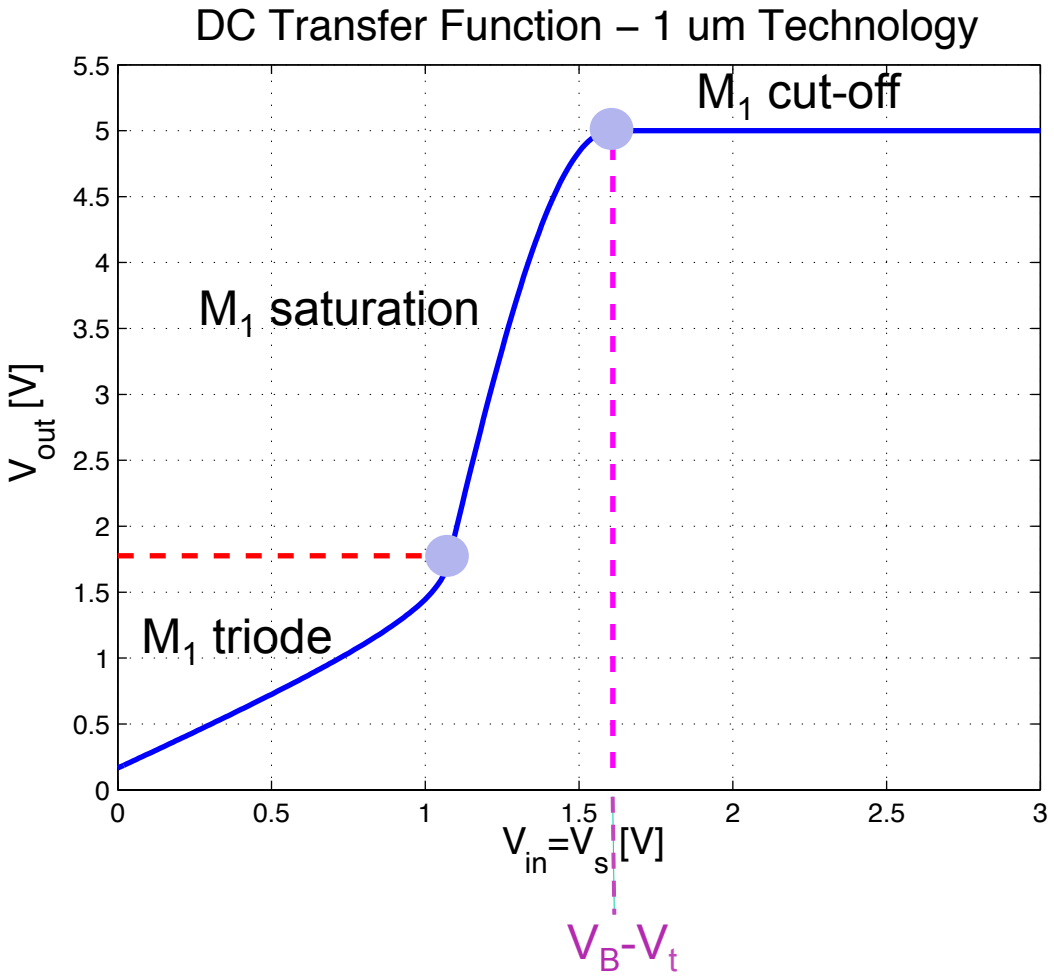
CG biasing (1)

- Example:
  V_{DD} = 5V; V_B = 2.5V; I_B = 400μA; R_D=3KΩ; W=100μm; L=1μm; V_{t0} = 0.5V

```
* CG stage
* filename: cgbias.sp
* C. Talarico, Fall 2014

*** device model
.model simple_nmos nmos kp=50u vto=0.5 lambda=0.1 cox=2.3e-3 capop=2
+ cgdo=0.5n cgso=0.5n cj=0.1m cjsw=0.5n pb=0.95 mj=0.5 mjsw=0.95
+ acm=3 cjgate=0 hdif=1.5u gamma=0.6 PHI=0.8

*** useful options
.option post brief nomod accurate

*** circuit
VDD vdd 0  5
* IB  vi 0 dc 400u
VS  vi  0  dc  1.3077   *** value for .op analysis
VB  vb  0  dc  2.5
*** d   g   s   b
mn1 vo  vb  vi   0   simple_nmos w=100u  l=1u
Rd  vdd vo  3k
*** calculate operating point
.op
*** large signal analysis (sweep Vi)
.dc VS 0 5 0.01

.end
```

```
element  0:mn1
 model    0:simple_n
 region     Saturati
  id        400.0000u
  ibs       -13.0770f
  ibd       -38.0000f
  vgs         1.1923
  vds         2.4923
  vbs        -1.3077
  vth       834.4189m
  vdsat     357.8811m
  vod       357.8811m
  beta        6.2462m
  gam eff   600.0000m
  gm          2.2354m
  gds        32.0197u
  gmb       461.9214u
  cdtot      75.6690f
  cgtot     256.1831f
  cstot     246.0823f
  cbtot      69.7376f
  cgs       203.3341f
  cgd        50.7643f
```

CG biasing (2)



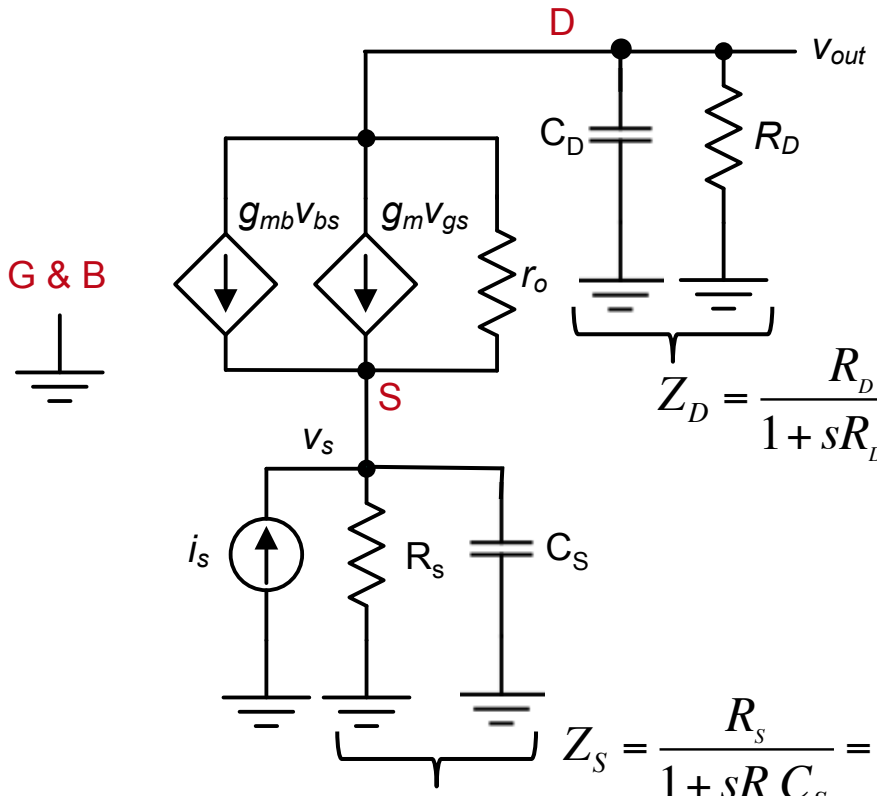
- The I/O characteristic is flipped w.r.t. the CS stage (small signal voltage gain $A_V = dV_{out}/dV_{in}$ is positive !)

CG small signal model

- Depending on how the CG is used the output variable of interest may be:
  - The current that flows into the output (Current Buffer)
  - The voltage at the output (Transresistance Amplifier)

careful with signs:

$v_{bs}=v_{gs} = -v_s$



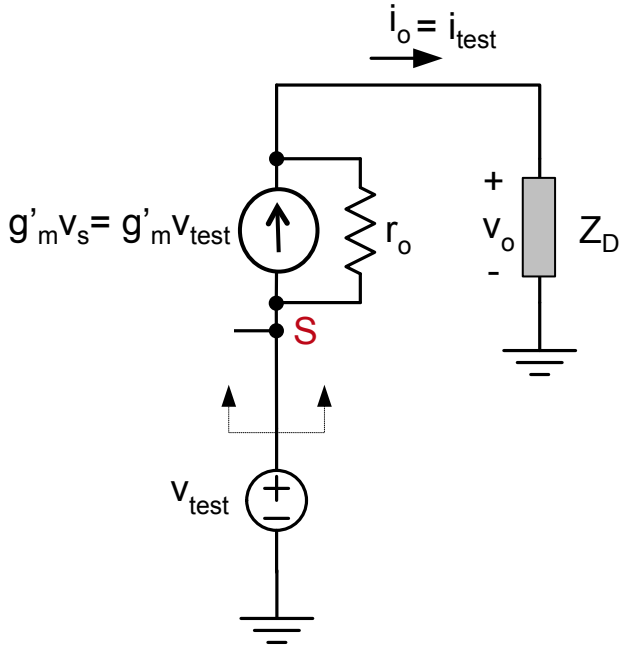
$$Z_D = \frac{R_D}{1+sR_DC_D} = \frac{1}{sC_D + \frac{1}{R_D}}$$

$$Z_S = \frac{R_S}{1+sR_SC_S} = \frac{1}{sC_S + \frac{1}{R_S}}$$

CG input impedance (1)

First pass:

Z_S in || to v_{test} so let's temporarily "remove" it



$KCL@v_o$: w.r.t. ($g'_m r_o >> 1$)

$$0 = \frac{v_o}{Z_D} + \frac{v_o}{r_o} - \frac{v_{test}}{r_o} - g'_m v_{test} \Rightarrow v_o \cong g'_m \left(Z_D \| r_o\right) v_{test}$$

$KCL@v_{test}$: w.r.t. ($g'_m r_o >> 1$)

$$i_{test} = g'_m v_{test} + \frac{v_{test}}{r_o} - \frac{v_o}{r_o}$$

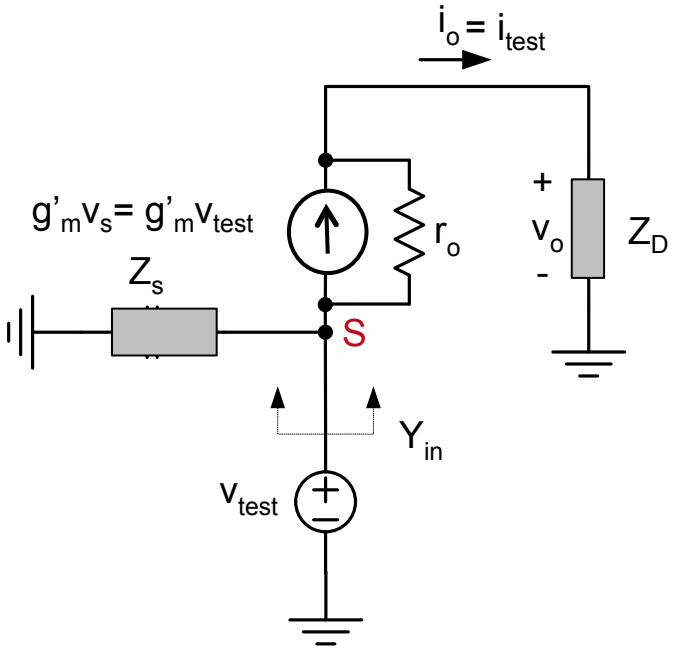
$$\frac{i_{test}}{v_{test}} \cong g'_m - g'_m \frac{Z_D r_o}{r_o(Z_D + r_o)} = \frac{g'_m r_o}{Z_D + r_o}$$

Aside: if $g'_m r_o$ is not >> 1

$$\frac{v_{test}}{i_{test}} = \frac{1 + \frac{Z_D}{r_o}}{g'_m + \frac{1}{r_o}}$$

CG input impedance (2)

Final Pass: Let's bring back Z_S:



$$Y_{in} \cong \frac{g'_m r_o}{Z_D + r_o} + sC_S + \frac{1}{R_S} = \frac{g'_m r_o}{\left(R_D \parallel \frac{1}{sC_D}\right) + r_o} + sC_S + \frac{1}{R_S}$$

$$Z_{in} \cong \frac{r_o + \left(R_D \parallel \frac{1}{sC_D}\right)}{g'_m r_o} \parallel \frac{1}{sC_S} \parallel R_S$$

$g'_m r_o >> 1$
(always true with our technology !!)

CG input impedance: Summary (1)

$$Z_{in} \cong \frac{r_o + \left(R_D \,||\, \frac{1}{sC_D} \right)}{g'_m r_o} \,||\, \frac{1}{sC_S} \,||\, R_S$$

- At low frequency: $\boxed{R_{in} \cong \frac{r_o + R_D}{g'_m r_o} \,||\, R_S}$

- Two interesting cases:
  - $R_D << r_o$

$$R_{in} \cong \frac{1}{g'_m} \,||\, R_S$$

Typically $R_S >> 1/g'_m$

If not most of the driving current instead of going to the MOS is lost !!

Well known result !

  - R_D is not << r_o

This happen quite often !!
(example: R_D is a current source load)

Not so Well known …

CG input impedance: Summary (2)

$$Z_{in} \cong \frac{r_o + \left(R_D \parallel \frac{1}{sC_D}\right)}{g'_m r_o} \parallel \frac{1}{sC_S} \parallel R_S$$

- At high frequency
  - As long as $R_D << r_o$ (regardless of the term C_D)

Typically $R_S >> 1/g'_m$

$$Z_{in} \cong \frac{1}{g'_m} \parallel \frac{1}{sC_S} \parallel R_S \cong \frac{1}{g'_m} \parallel \frac{1}{sC_S}$$

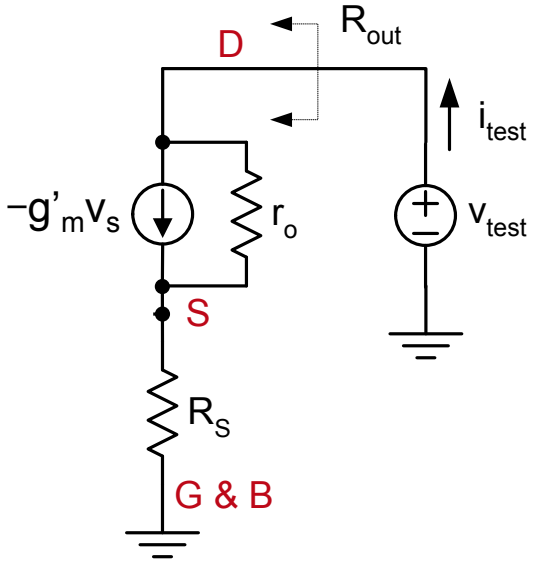
NOTE:

$R_D \parallel \frac{1}{sC_D}$ is always < than R_D.

If $R_D << r_o$ so is $R_D \parallel \frac{1}{sC_D}$

CG output impedance (1)

- At low frequency



w.r.t. ($g'_m r_o >> 1$)

$$i_{test} = \frac{v_{test}}{r_o} - \frac{v_s}{r_o} - g'_m v_s$$

$$v_s = R_S \cdot i_{test}$$

$$R_{out} = \frac{v_{test}}{i_{test}} \cong r_o(1 + g'_m R_S)$$

(Very high if $g'_m R_S >> 1$)

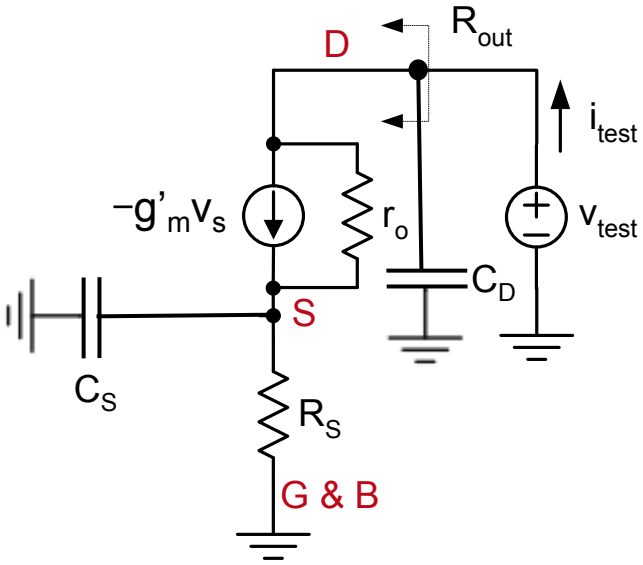
$$R_{out} = \frac{v_{test}}{i_{test}} \cong r_o g'_m R_S$$

Aside: if $g'_m r_o$ is not >> 1

$$R_{out} = \frac{v_{test}}{i_{test}} = R_s + r_o(1 + g'_m R_s)$$

CG output impedance (2)

- At high frequency

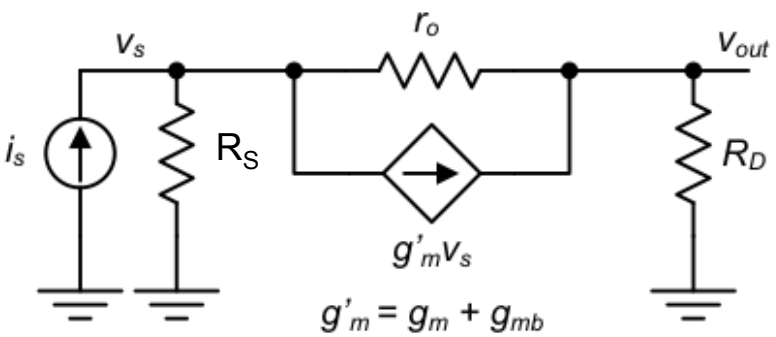


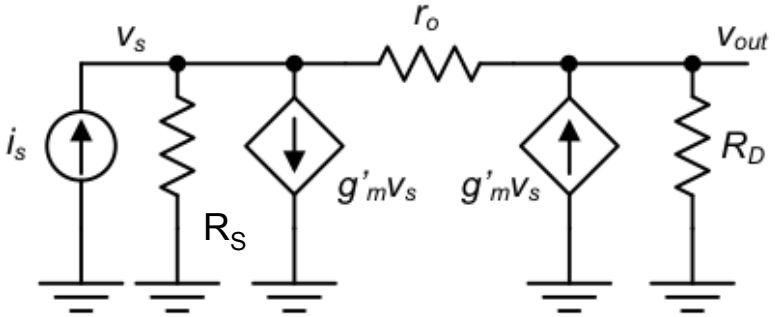
$$Z_{out} \cong r_o\left[1+g'_m\left(R_S \parallel \frac{1}{sC_S}\right)\right] \parallel \frac{1}{sC_D}$$

Typically $C_S/(g'_m r_o) << C_D$

If $g'_m R_s >> 1 \longrightarrow Z_{out} \cong g'_m r_o R_S \parallel \frac{g'_m r_o}{sC_s} \parallel \frac{1}{sC_D} \cong g'_m r_o R_S \parallel \frac{1}{sC_D}$

CG current transfer (1)

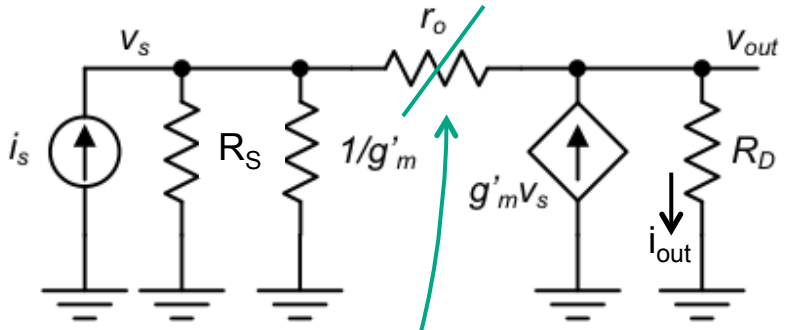




w.r.t. ($g'_m r_o >> 1$)

$$i_{out} = \frac{v_s}{r_o} - \frac{v_{out}}{r_o} + g'_m v_s \cong -\frac{R_D i_{out}}{r_o} + g_m' v_s$$

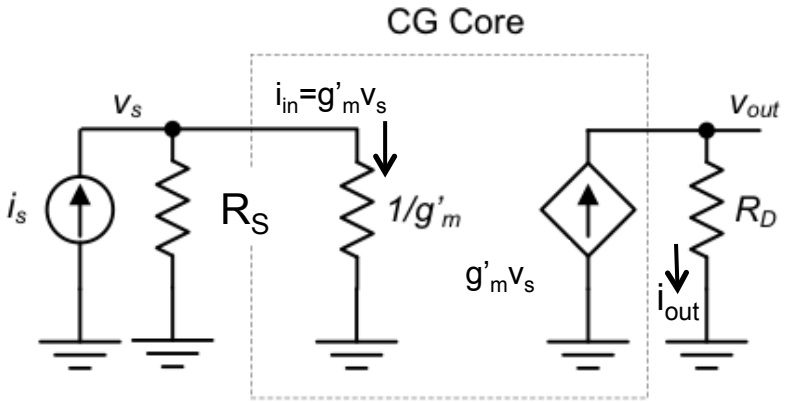
$$i_{out}\left(1 + \frac{R_D}{r_o}\right) \cong g'_m v_s$$



NOTE:

for $r_o >> R_D \rightarrow i_{out} \cong g_m' v_s$ ➡ The CG stage is approx. unilateral

CG current transfer (2)



CG stage model valid for:
$g'_m r_o >> 1$ and $r_o >> R_D$

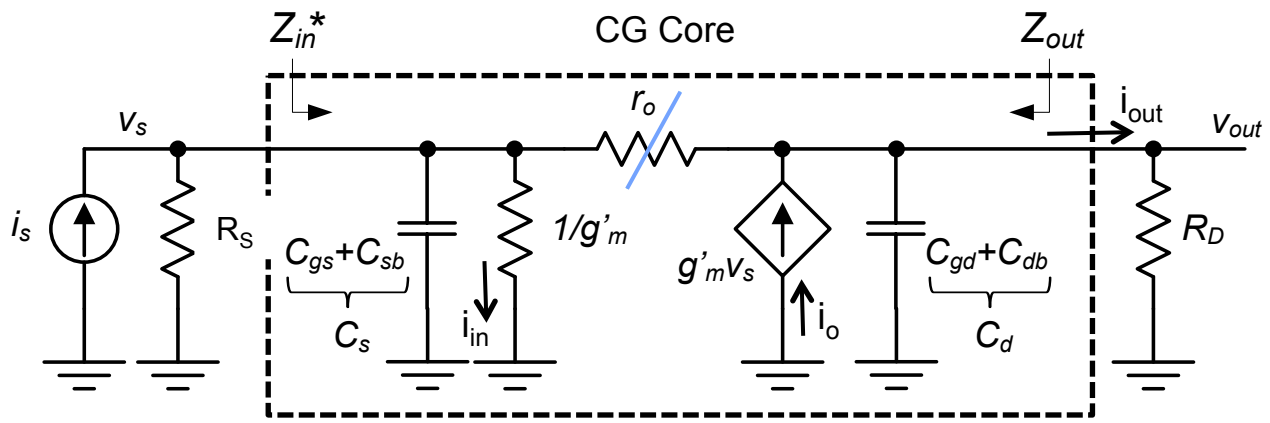
- At low frequency:
  - for $g'_m r_o >> 1$ and $r_o >> R_D$)

$$\frac{i_{out}}{i_s} = \frac{i_{out}}{i_{in}} \frac{i_{in}}{i_s} \cong \frac{R_S}{\frac{1}{g'_m} + R_S} \cong 1$$

Typically $g'_m R_S >> 1$

This is a current buffer !!!
$A_{I0} \cong 1$, R_{in} small, R_{out} large

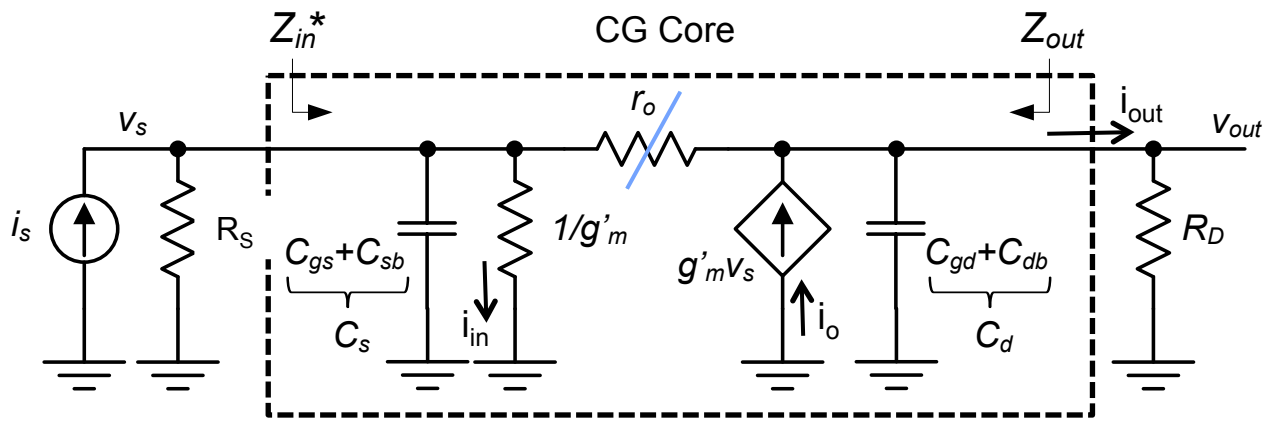
CG current transfer (3)



- At high frequency:
  - for $g'_m r_o >> 1$ and $r_o >> R_D$ $\left(since\ R_D > R_D \| \frac{1}{sC_D},\ r_o >> R_D\ implies\ r_o >> Z_D \right)$

$$\frac{i_o}{i_s} \cong \frac{g'_m v_s}{\left(\frac{1}{R_S} + sC_S + g'_m\right) v_s} = \frac{g'_m R_S}{1 + sR_S C_S + g'_m R_S} = \frac{A_{I0}}{1 - \frac{s}{p_1}} = \frac{g'_m R_S}{1 + g'_m R_S} \cdot \frac{1}{1 + s\frac{C_S}{g'_m + \frac{1}{R_S}}}$$

CG current transfer (4)

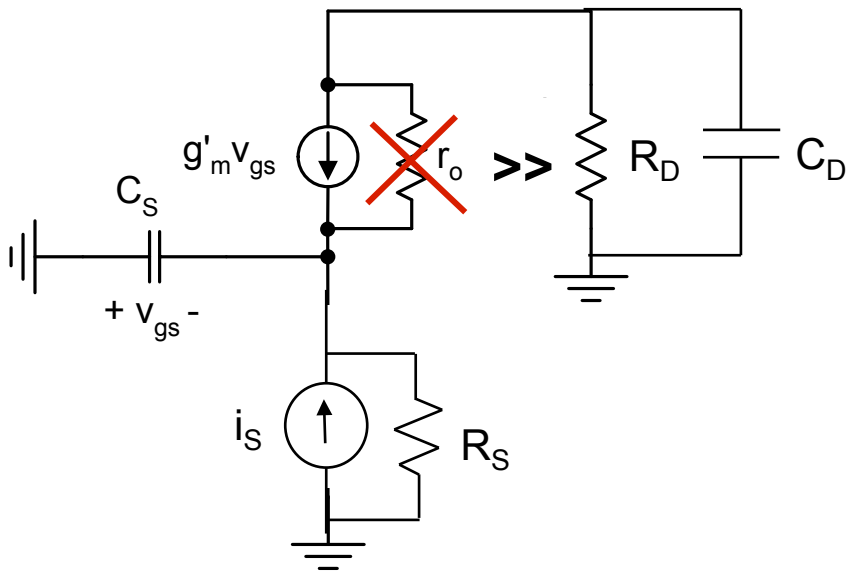


$$\frac{i_{out}}{i_s} = \frac{i_{out}}{i_o}\frac{i_o}{i_s} \cong \frac{\frac{1}{sC_D}}{\frac{1}{sC_D}+R_D}\cdot\frac{g'_m R_S}{1+g'_m R_S}\cdot\frac{1}{1+s\frac{C_S}{g'_m+\frac{1}{R_S}}} = \underbrace{\frac{1}{1+sC_D R_D}}_{\frac{1}{1-\frac{s}{p_2}}}\cdot\underbrace{\frac{g'_m R_S}{1+g'_m R_S}}_{A_{I0}}\cdot\underbrace{\frac{1}{1+s\frac{C_S}{g'_m+\frac{1}{R_S}}}}_{\frac{1}{1-\frac{s}{p_1}}}$$

$$\frac{i_{out}}{i_s} \cong \frac{1}{(1+sC_D R_D)\left(1+s\frac{C_S}{g'_m}\right)}$$

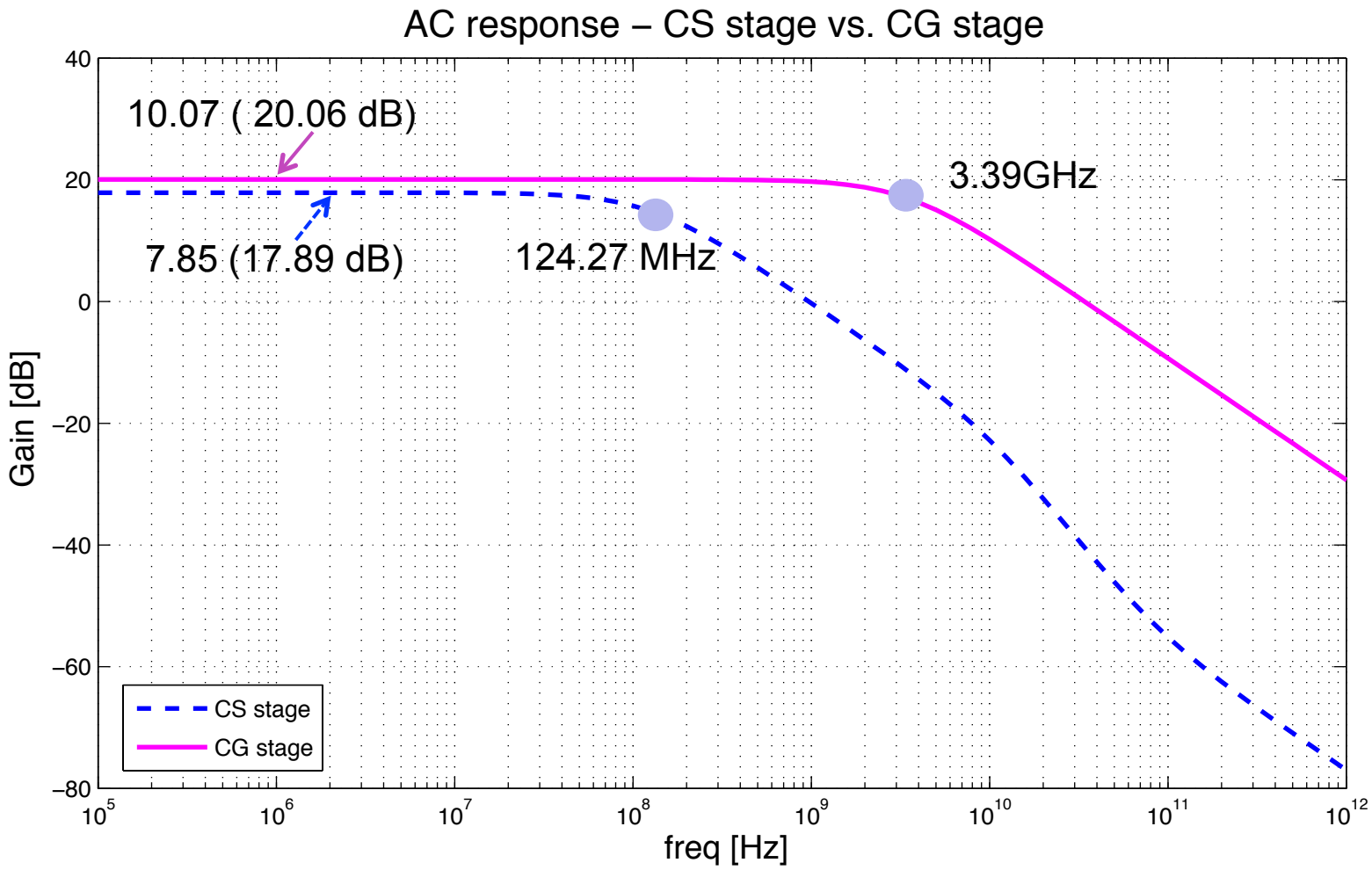
Typically $g'_m R_S >> 1$

CG Input-Output RC Time Constants



- For this specific configuration and assumptions ($r_o >> R_D$ and $g'_m r_o >> 1$) input and output are decoupled → "RC time constants" are = 1/poles
  - Input RC: $\sim C_S(1/g'_m)$ $(R_S >> 1/g'_m)$
  - Output RC: $R_D C_D$

CG Frequency Response



$A_{v0\_CS} \cong -g_m R_D$

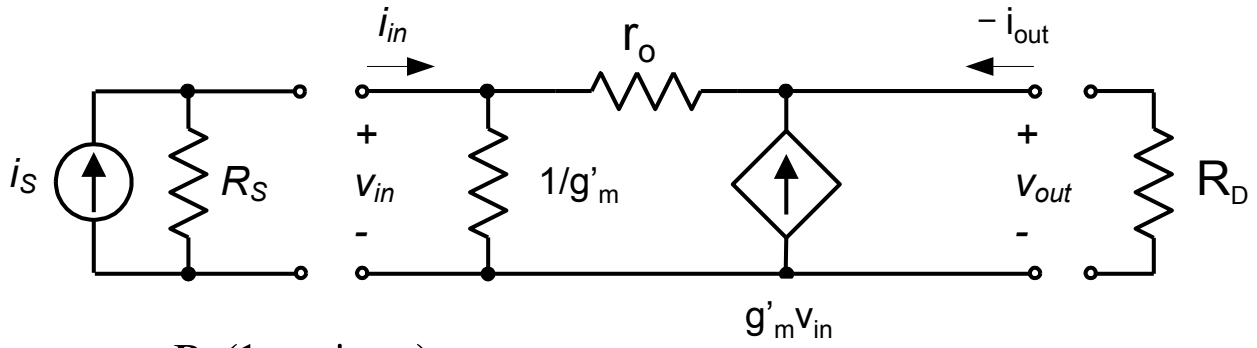
$A_{v0\_CG} \cong g'_m R_D$

CG Summary

- Current gain is about unity up to very high frequencies
  - The CG stage absorbs most of the current from the input source and it passes the current to the output terminal
- The CG does not contain a FB capacitance between input and output (no Miller effect)
  - The effect of large values of R_D on the frequency response in much less than in CS stage (for a desired BW we can extract more gain out of the CG stage)
- Input impedance is "typically" very low ($R_{in} \cong 1/g'_m$)
  - At least when the output is terminated with some reasonable impedance ($R_D << r_o$)
- Can achieve very high output resistance ($R_{out} \approx r_o g'_m R_S$)
- In summary, a common gate stage is ideal for turning a decent current source into a much better one
  - Seems like this is something we can use to improve our common source stage
    - Which is indeed nothing but a decent (voltage controlled) current source

"Aside"

- If we cannot assume $r_o >> R_D$, the unilateral model used for the CG stage falls apart. Computing the current transfer gain is a little harder.



$$\frac{i_{out}}{i_s} = \frac{R_S(1+g'_m r_o)}{R_D + r_o + R_S + g'_m r_o R_S}$$

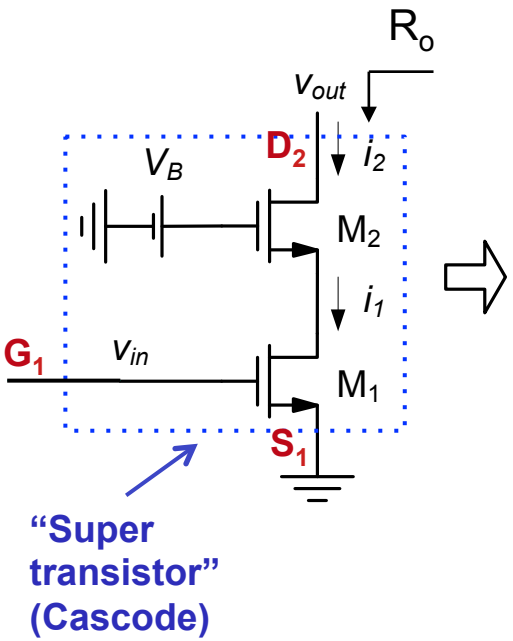
← pp.13-14 Murmann's Textbook

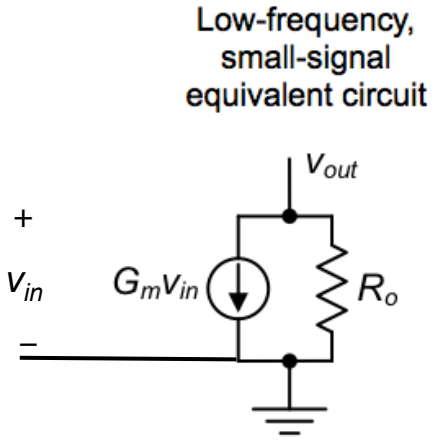
- The poles of the circuit are no longer isolated. However, computing the bandwidth using ZVTC is not too difficult.

$$\tau 1 = C_S \left[\left(\frac{1+\frac{R_D}{r_o}}{g'_m + \frac{1}{r_o}} \right) \| R_S \right] \qquad and \qquad \tau 2 = C_D \left[\left(R_s + r_o(1+g'_m R_s) \right) \| R_D \right]$$

Cascode Stage (CS + CG)

- One of the "most important" application of the CG.
- M_1 is a transconductor ($i_1=g_{m1}v_{in}$) and M_2 buffers the current fed by M_1 ($i_2 \approx i_1$)



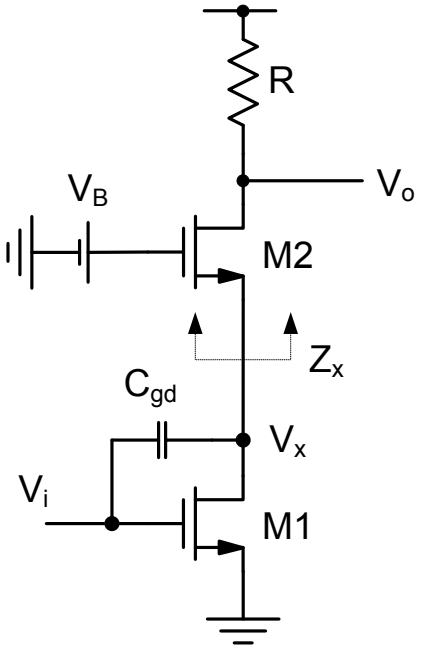


$$G_m = \frac{i_{out}}{v_{in}} = \frac{i_2}{i_1}\cdot\frac{i_1}{v_{in}} = \frac{i_2}{i_1}\cdot g_{m1} \cong g_{m1}$$

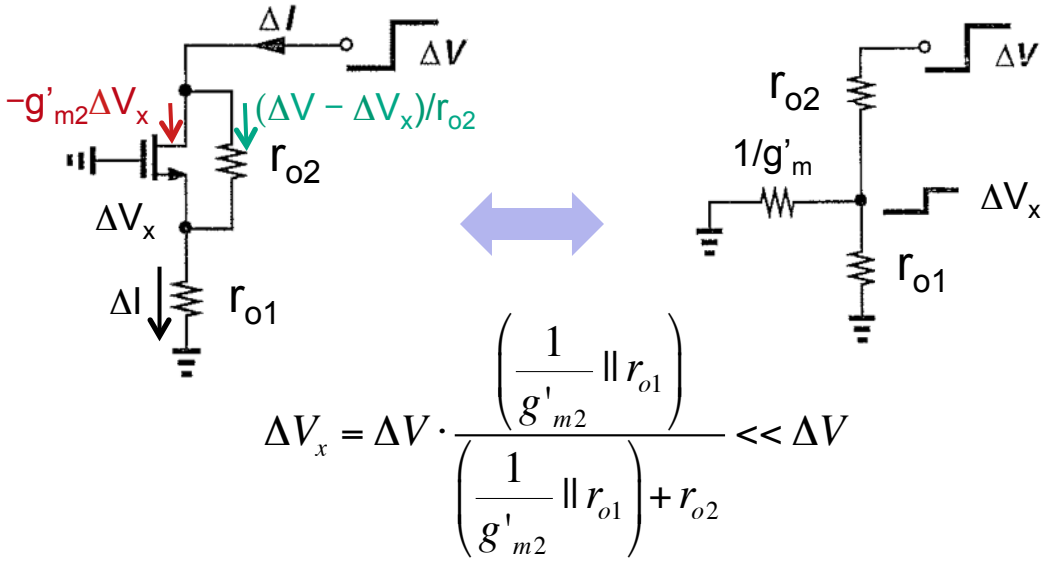
$$R_o \cong r_{o1}\cdot g'_{m2} r_{o2}$$

$$\underbrace{G_m R_o}_{\text{Intrinsic gain of cascode}} \cong g_{m1} r_{o1}\cdot g'_{m2} r_{o2} \propto \left(g_m r_o\right)^2$$

Low Frequency Benefits



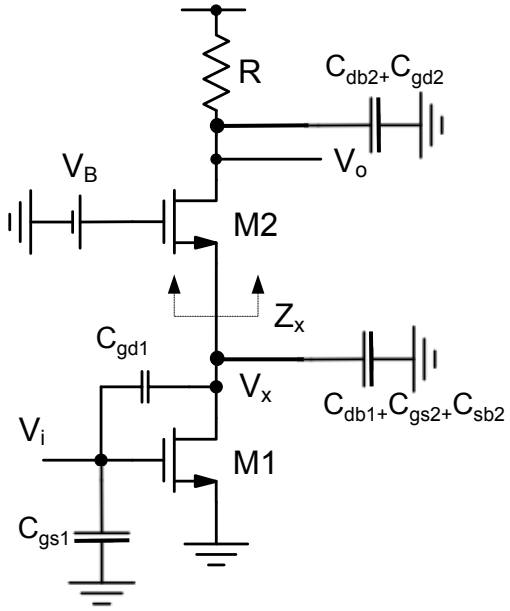
- Output resistance very high ($\approx g_m r_o^2$)
  - The cascode device "shields" the input device from voltage variations at the output node V_o



$$\Delta V_x = \Delta V \cdot \frac{\left(\frac{1}{g'_{m2}} \| r_{o1}\right)}{\left(\frac{1}{g'_{m2}} \| r_{o1}\right) + r_{o2}} << \Delta V$$

  - application: precision current source/mirror
- Intrinsic gain very high $(g_m r_o)^2$
  - application: OTA/OA
- Input resistance of CS stage ($R_{in} \approx \infty$)

High Frequency Benefits



$$\frac{v_x}{v_i} = -g_{m1}\left(Z_x \,\|\, r_{o1}\right) \cong -g_{m1}\left[\left(\frac{1}{g'_{m2}}\left(1+\frac{R}{r_{o2}}\right)\right) \| \, r_{o1}\right]$$

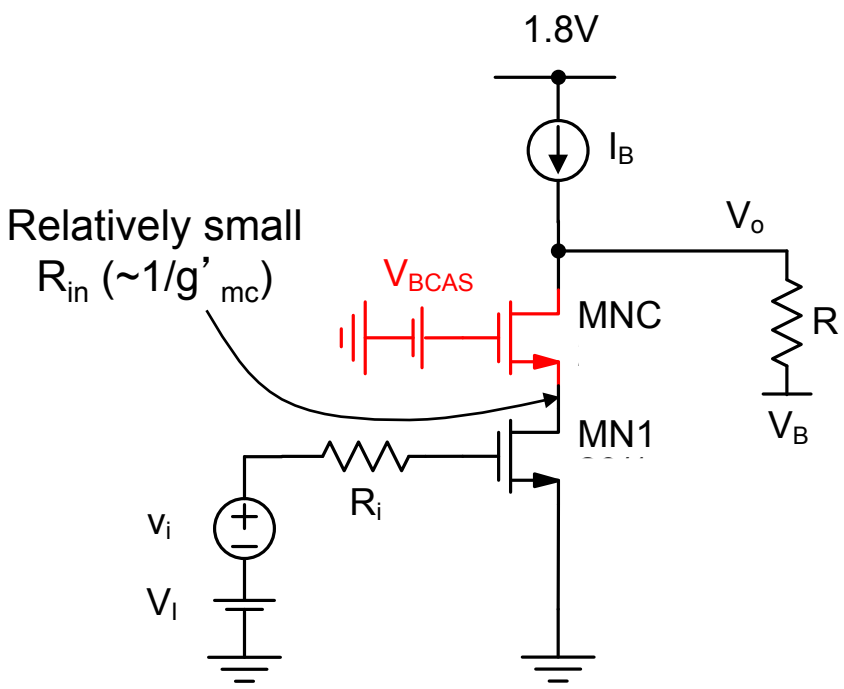
$g'_{m2}r_{o2} >> 1$

- For moderate value of R: v_x/v_i very close to −1
  - Mitigates Miller effect ($C_{in} \approx C_{gs1} + 2C_{gd1}$)
  - Even if R is large, there is often a load capacitance that provides a low impedance termination to help maintain t his feature (R is AC shorted by the load capacitance)
- For not so moderate values of R ($R \approx r_{o2}$): v_x/v_i very close to −2
  - Still mitigate Miller effect quite a bit ($C_{in} \approx C_{gs1}+3C_{gd1}$)
- Additional benefit
  - Cascode mitigates direct forward coupling from V_i to V_o at high frequencies (RHP zero at $z=+g_{m1}/C_{gd1}$)

$$I_{Cgd1} = sC_{gd1} \cdot (V_i - V_x)$$

if we could make $V_i \approx V_x \longrightarrow I_{Cgd1} \approx 0$
which would be the same as cancelling the zero !!

Example Revisited



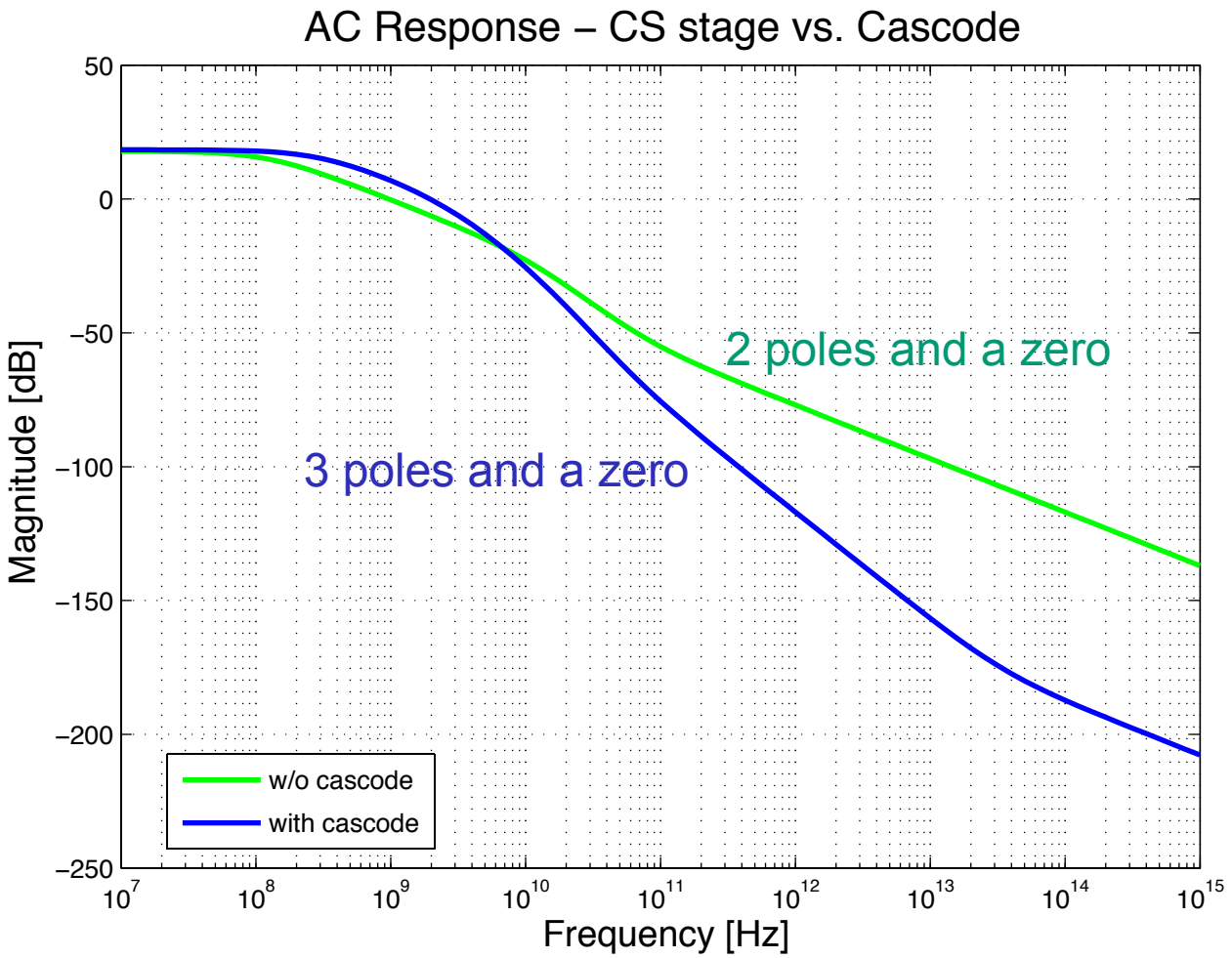
- What we expect to see after adding the cascode device
  - Bandwidth should increase (reduction of Miller effect)
    - Easy to compute using a ZVTC analysis
    - Non-dominant pole around some fraction of f_T of cascode device
    - Drain current of MN1 runs into a current divider between $1/g'_{mc}$ and total capacitance at this node (dominated by C_{gs} of MNC)

V_B = 0.9V; V_I = 0.627V; V_{DD} = 1.8V;

V_{BCAS}= 1.077V; I_B = 400μA; R = 2kΩ;

R_i = 10kΩ; W/L = 21.34 μm/0.18 μm

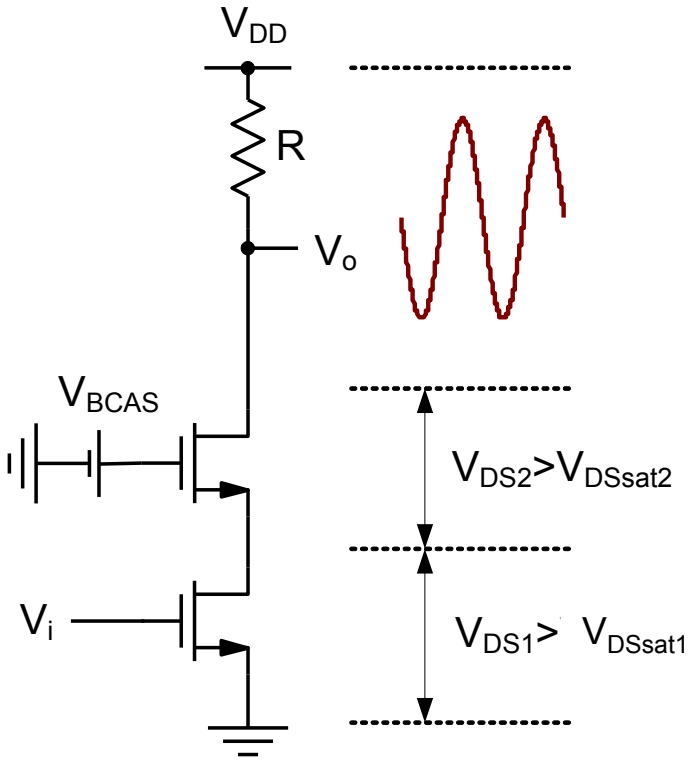
Simulated Frequency Response



3-dB bandwidth increased from 124.57 MHz to 291.69 MHz (≈2.34x)

|gain_cs| = 17.84 dB; |gain_cas| = 18.40 dB

Supply Headroom Issue (1)



- Even if we adjust V_{BCAS} such that V_{DS1} is small, adding a cascode reduces the available signal swing
- This can be a big issue when designing circuits with $V_{DD}\cong 1V$
  - Typically need each V_{DS}>~0.2V

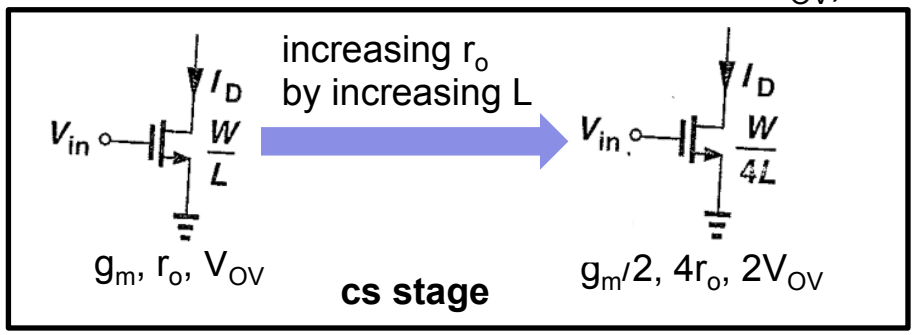
Supply Headroom Issue (2)

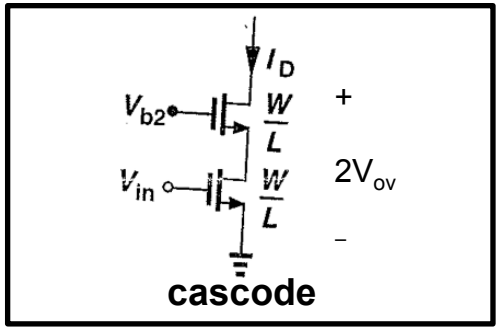
- Is the issue really as “bad” as it sounds ?
- For a given bias current, let’s compare the “price” of increasing gain using cascoding vs. the “price” of increasing gain augmenting the transistor’s length in a CS stage

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}V_{OV}^2 \qquad g_m = \frac{2I_D}{V_{OV}} \qquad r_o \propto \frac{L}{I_D}$$

Source: Razavi

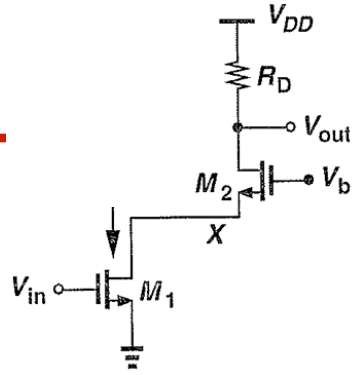
Example: let’s quadruple L (if we quadruple L, to maintain the same I_D we need to double V_{OV})





- **Very Interesting result:**
  - By quadruplicating L we consume an extra V_{OV} of headroom, (we consume 4x more area), and we get a 2x increase in the intrinsic gain ($\approx 2g_m r_o$)
  - By cascoding we also consume and extra V_{OV} of headroom, (we consume only 2x more area), but we get a significant better intrinsic gain ($\approx g_m r_o)^2$

Cascode Bias Analysis



Source: Razavi

- M_1 saturation: $V_x > V_{in} - V_{T1}$

  $V_x = V_B - V_{GS2} > V_{in} - V_{T1} \quad \longleftrightarrow \quad V_B > V_{in} - V_{T1} + V_{GS2}$

- M_2 saturation: $V_{out} - V_x > V_{GS2} - V_{T2}$

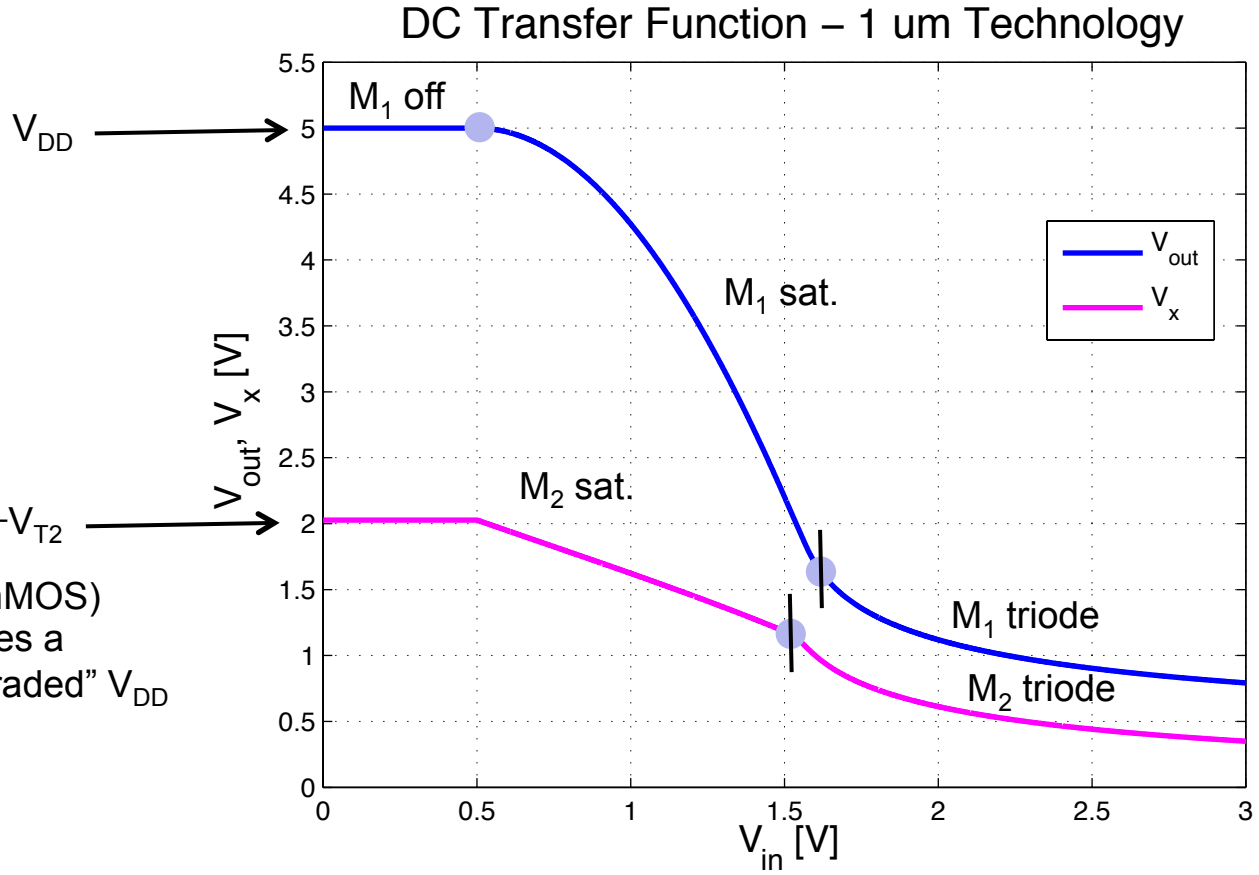
  $V_{out} > \underbrace{V_B - V_{GS2}}_{= V_x} + V_{GS2} - V_{T2} \longrightarrow V_{out} > \underbrace{V_{in} - V_{T1}}_{= V_{OV1}} + \underbrace{V_{GS2} - V_{T2}}_{= V_{OV2}}$

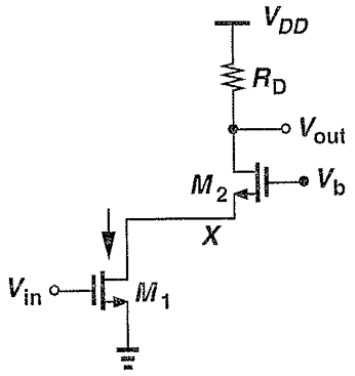
- The minimum output DC level for which both transistors operate in saturation is:

  $V_{out}(\text{min}) = V_{OV1} + V_{OV2}$

I/O DC characteristic of cascode stage

- *Example:* V_{DD}=5V, V_B = 3V, W/L = 20μm/1μm, R_D=5KΩ



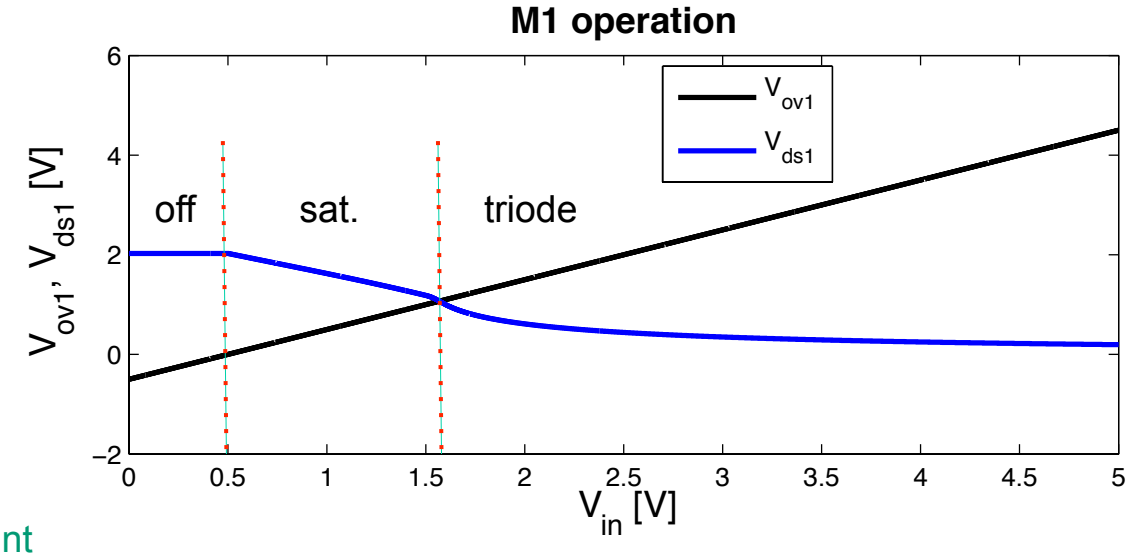


$V_{out}(max) = V_{DD}$

$V_{out}(min) = V_{OV1} + V_{OV2}$

- As V_{in} assumes sufficiently large values
  - V_x drops below V_{in} by V_{T1} forcing M_1 into triode
  - V_{out} drops below V_B by V_{T2} forcing M_2 into triode
- Depending of the device dimensions and the values of R_D and V_B one effect may occur before the other

Detailed Transistors operation



all M_2 current goes into charging cap. at node x