Common Source Stage
Miller Approximation
ZVTC Analysis
Backgate Effect

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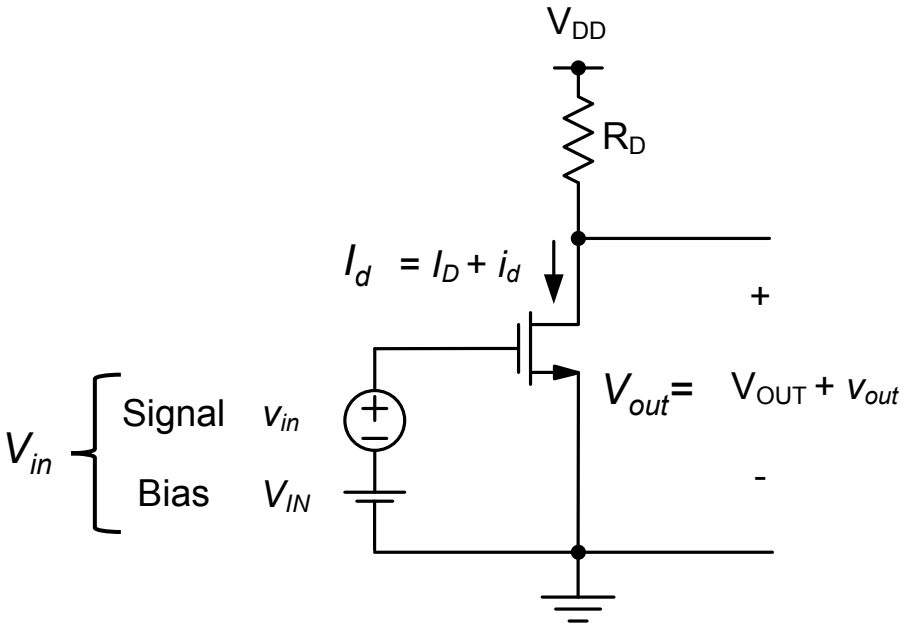
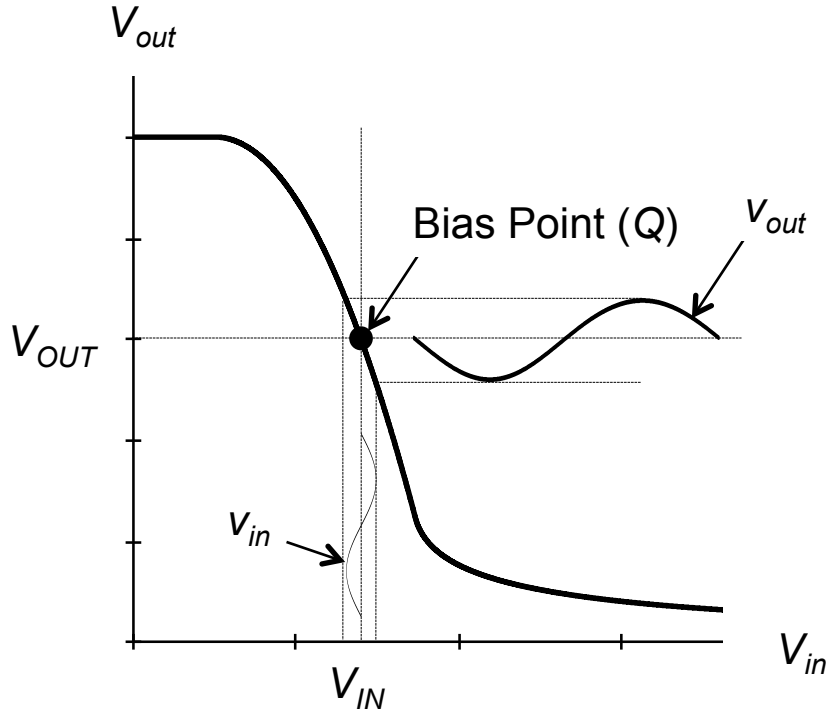
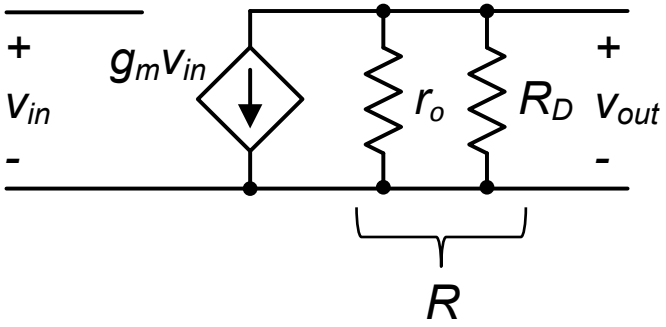
Sources:
most of the figures were provided by B. Murmann

CS with Resistive Load







$$A_v = -\underbrace{\frac{2I_D}{V_{OV}}}_{g_m} R_D \,\|\, r_o \cong -\frac{2I_D}{V_{OV}} R_D$$

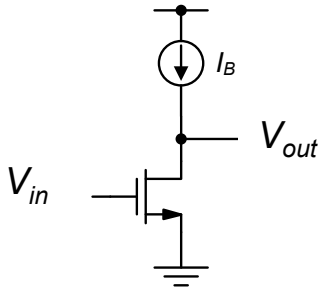
often but not always !!!

Does r_o matter ?

- r_o can be neglected in the gain calculation as long as the desired gain $|A_v|$ is much less than the intrinsic gain $g_m r_o$

$$|A_V| = g_m (R_D \| r_o) \longrightarrow \frac{1}{|A_V|} = \frac{1}{g_m R_D} + \frac{1}{g_m r_o} \longrightarrow$$

$$\longrightarrow g_m R_D = \frac{|A_V|}{1 - \frac{|A_V|}{g_m r_o}} \cong |A_V| \quad for \quad |A_V| << g_m r_o$$



Intrinsic Gain

$$g_m r_o \cong \frac{2I_D}{V_{OV}} \cdot \frac{1}{\lambda I_D} = \frac{2}{\lambda V_{OV}}$$

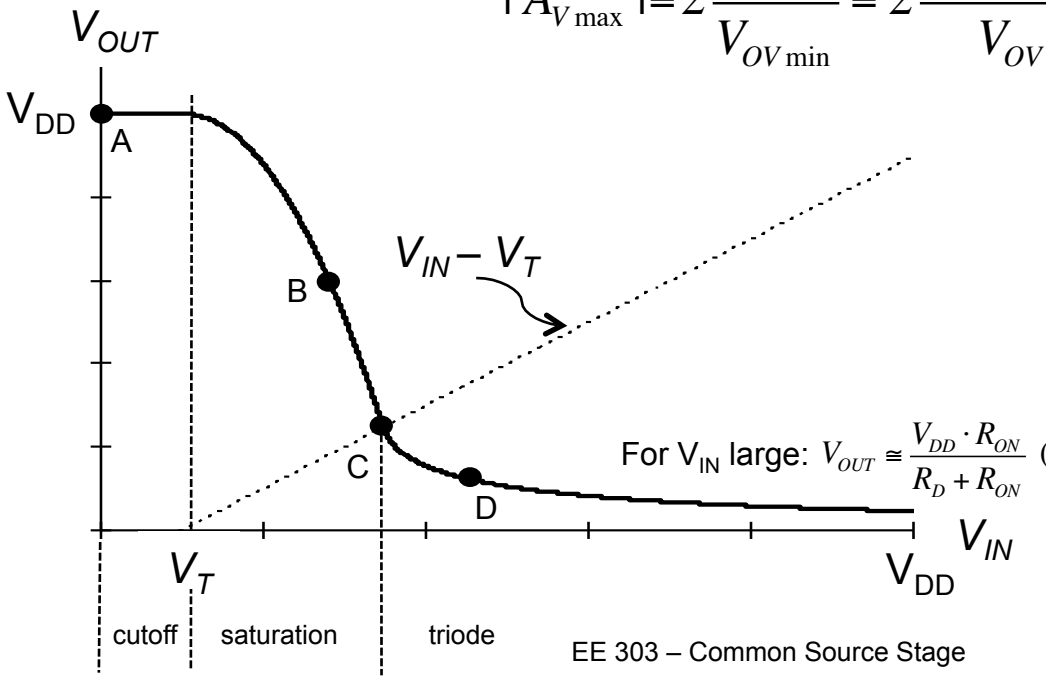
NOTE:
The small signal parameters (that is g_m and r_o) are determined by the DC bias point

Upper Bound on Gain

- In the basic common source stage R_D performs two "conflicting" tasks
  - it translates the device's drain current i_d into the output voltage v_{out}.
  - it sets the drain bias voltage (V_{DS}) of the MOSFET
- This creates an upper bound on the achievable small signal voltage gain

$$|A_V| \cong \frac{2I_D}{V_{OV}} R_D = 2\frac{V_{R_D}}{V_{OV}}$$

$$|A_{V\max}| = 2\frac{V_{RD\max}}{V_{OV\min}} = 2\frac{V_{DD} - V_{OV\min}}{V_{OV\min}} \cong 2\frac{V_{DD}}{V_{OV\min}}$$



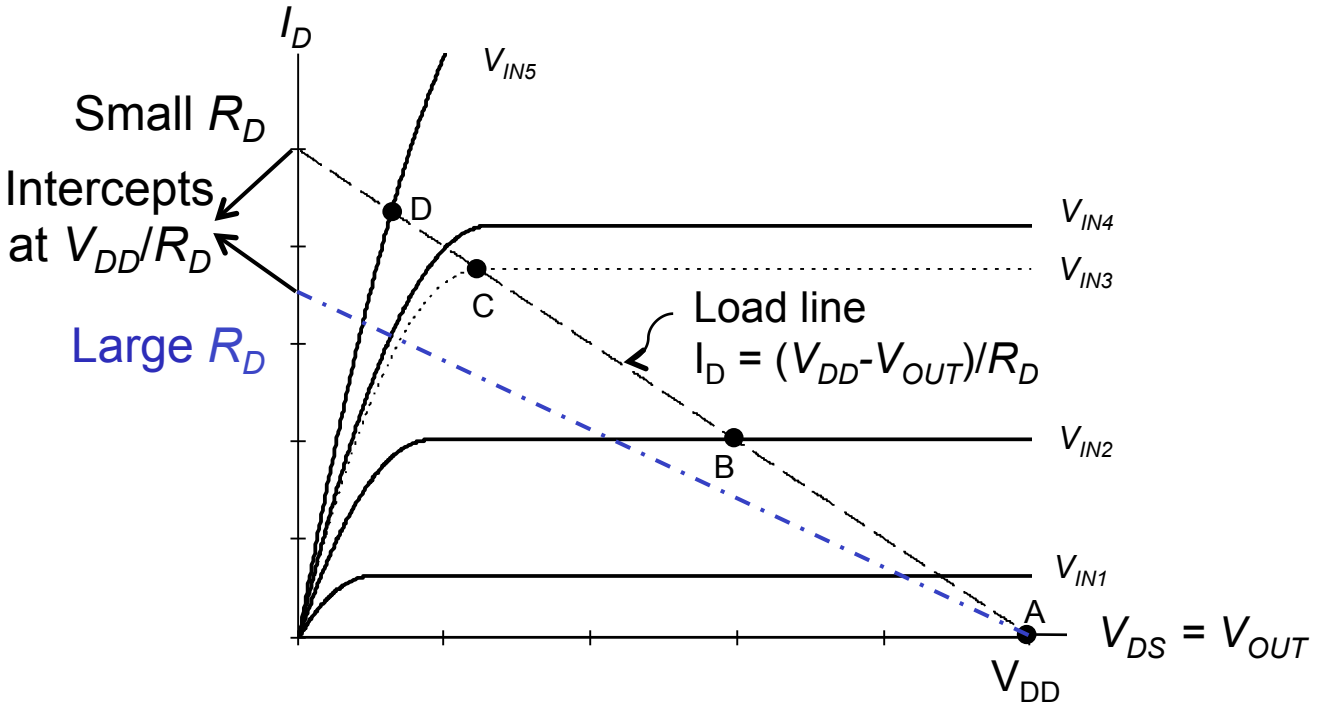
For V_{IN} large: $V_{OUT} \cong \frac{V_{DD} \cdot R_{ON}}{R_D + R_{ON}}$ $(resistive\ divider)$

NOTE:
only a limited range
of the VTC is useful
for amplification

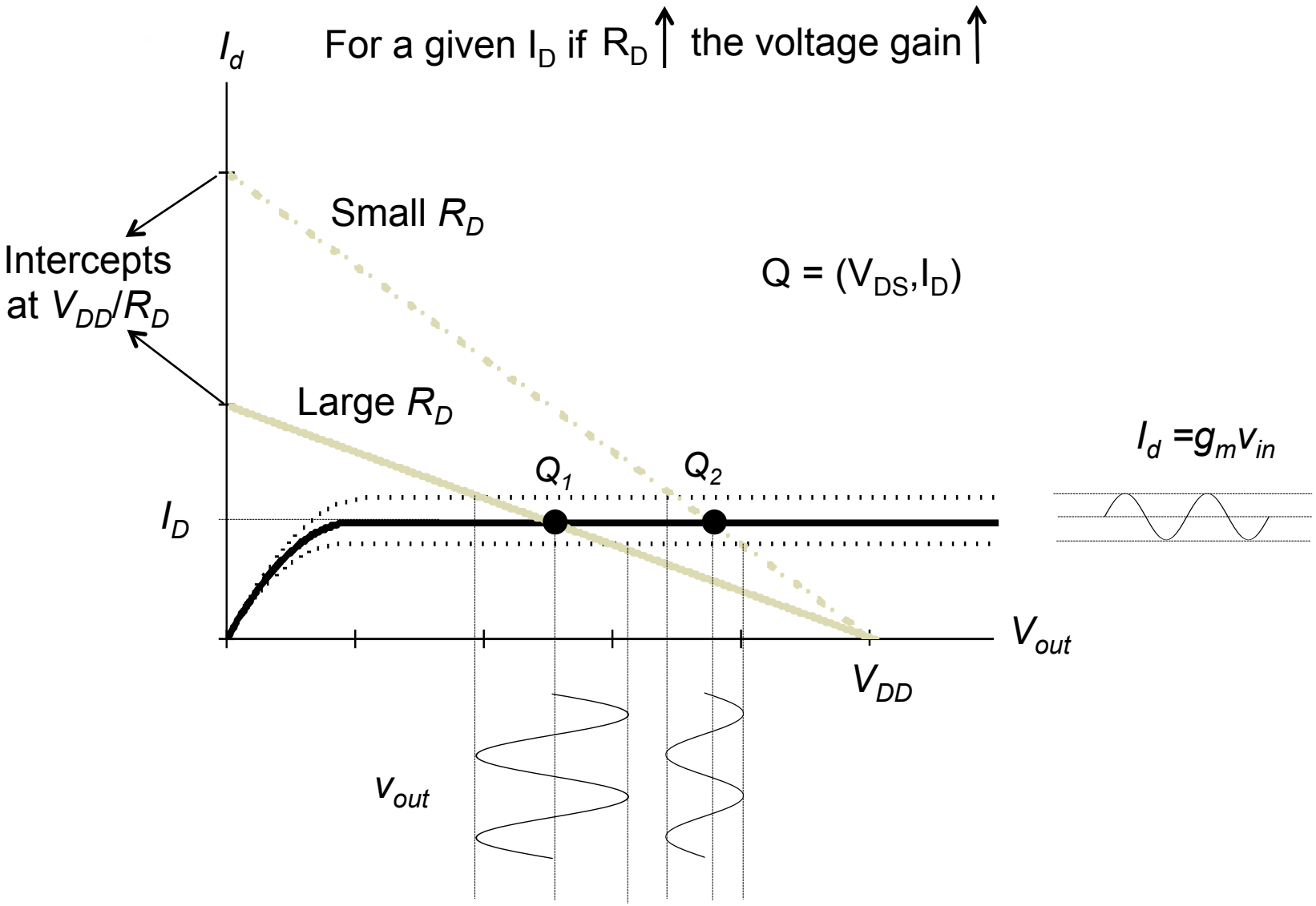
Voltage Gain and Drain Biasing Considerations (1)

$V_{IN}\uparrow \Leftrightarrow I_D\uparrow \Leftrightarrow V_{DS}=V_{DD}-R_D I_D\downarrow$

For a given I_D if $R_D\uparrow$ ($\Leftrightarrow V_{DS}\downarrow$) the bias point Q moves toward triode region

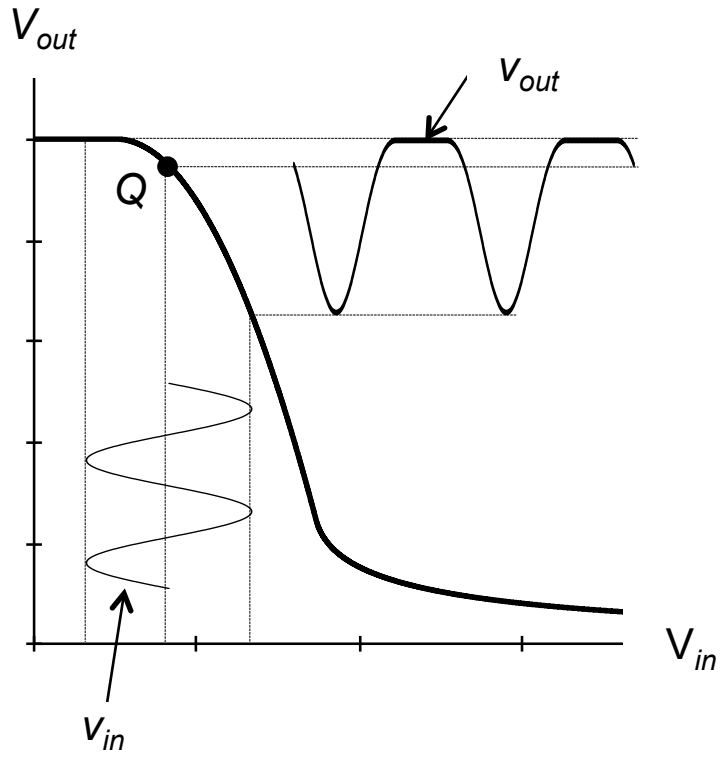


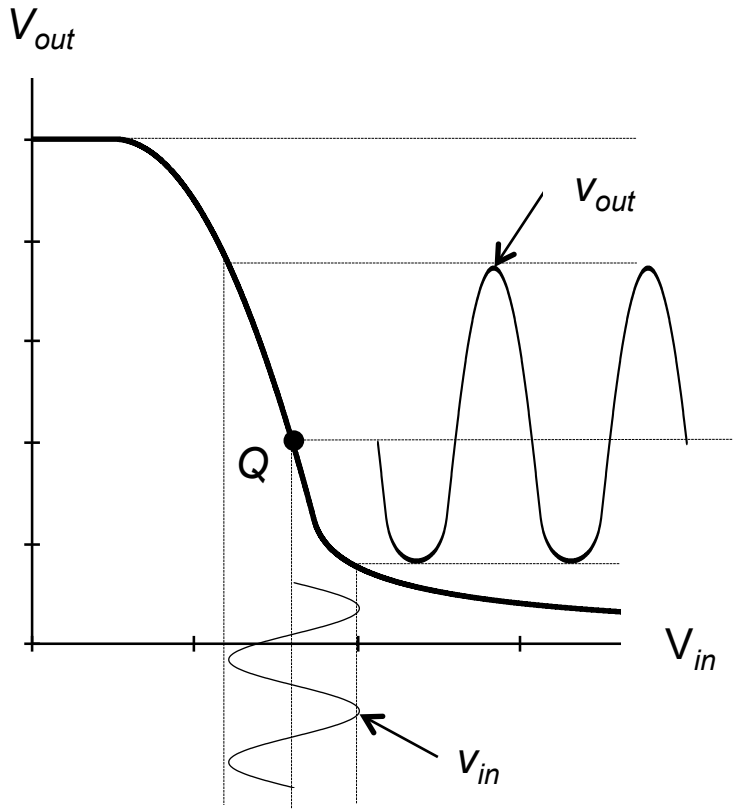
Voltage Gain and Drain Biasing Considerations (2)



Importance of choosing the "right" bias point

- Deciding the location of the bias point Q affects:
  - gain (the values of g_m and r_o depend on the DC bias)
  - allowable signal swing at the output



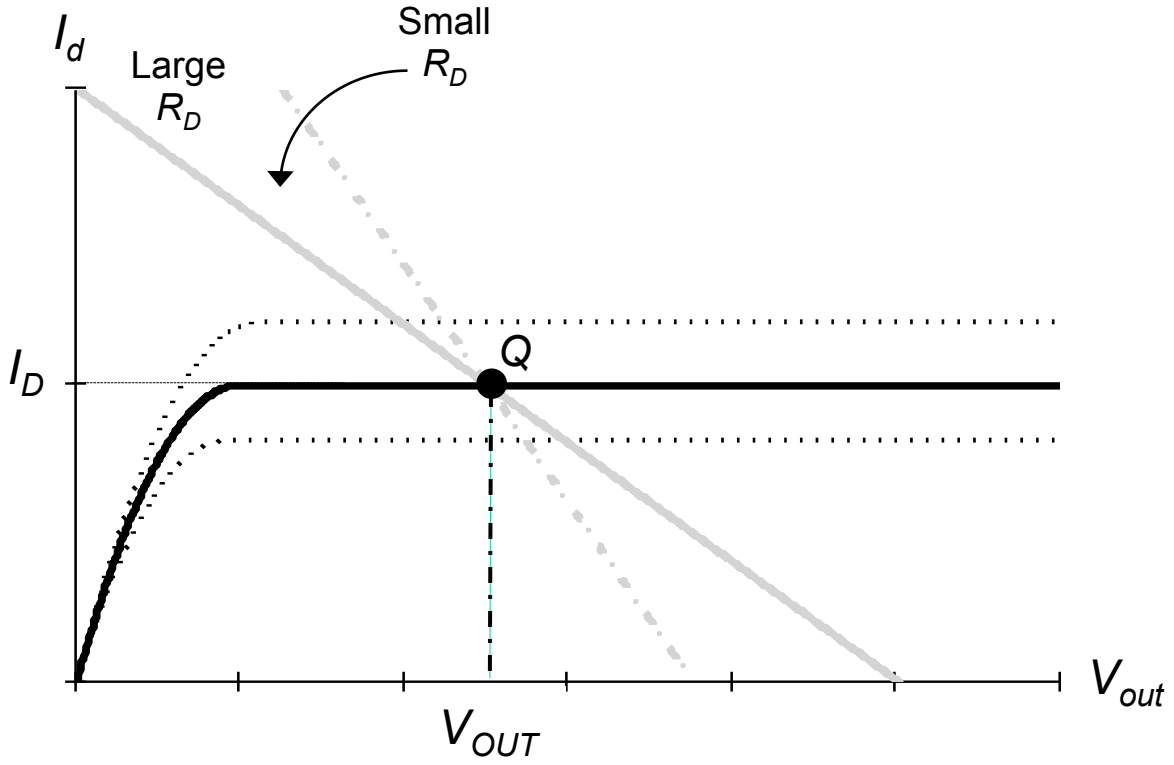


Can we overcome the upper bound on gain ?

- The upper bound comes from the fact that both gain and bias point depend on R_D
  - Want large R_D for large gain
  - Want small R_D to prevent device from entering triode region

$$|A_{V\max}| \cong 2\frac{V_{DD}}{V_{OV\min}}$$

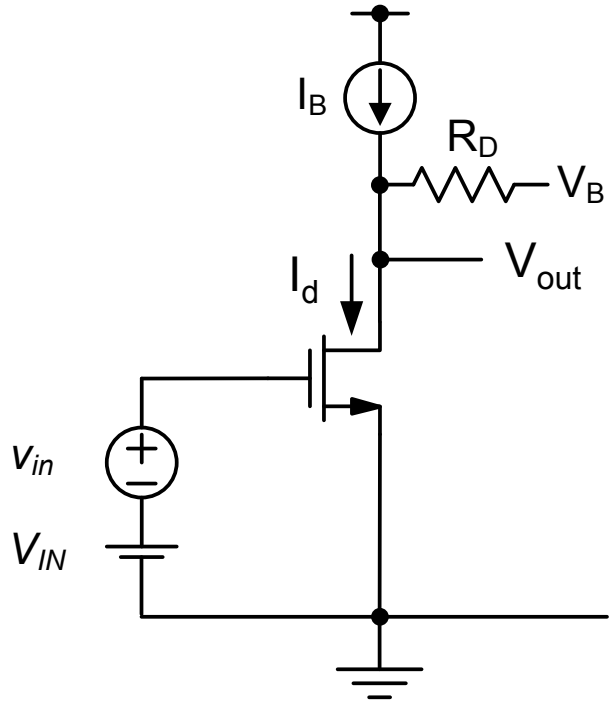
- We can overcome the upper bound, if we can find a way to set V_{OUT} independently of R_D

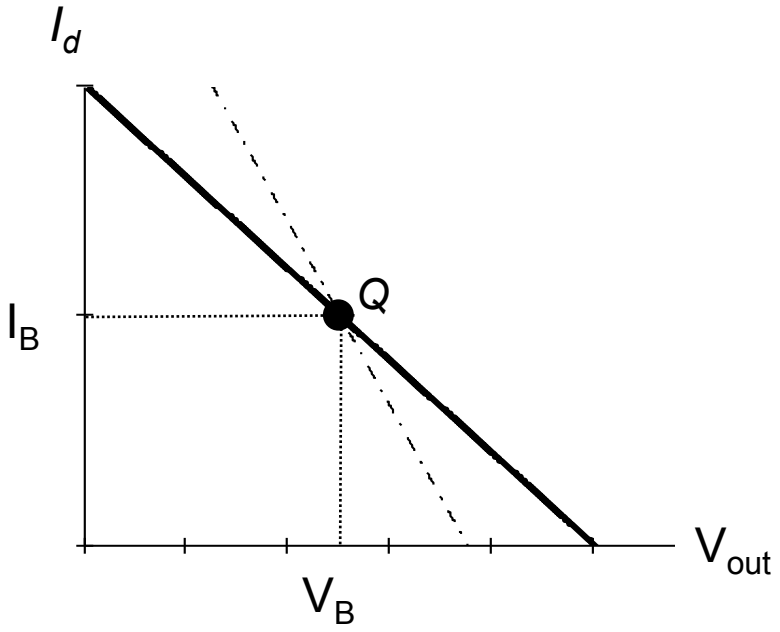


CS stage with improved drain biasing scheme

$$I_d = I_B + \frac{V_B - V_{out}}{R_D}$$

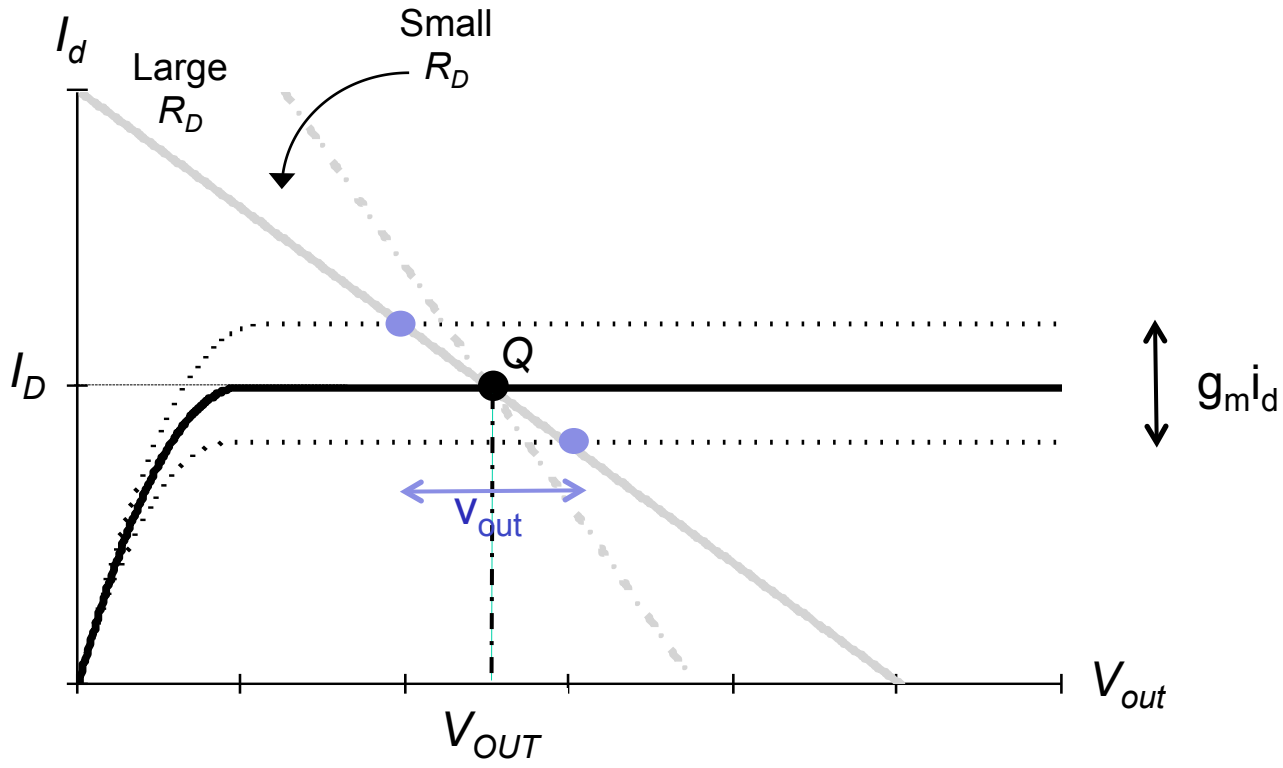
at the point $V_{out}=V_B$ we have $I_d=I_B$ regardless the value of R_D





We wish to set $I_B=I_D$ and $V_B=V_{OUT}$

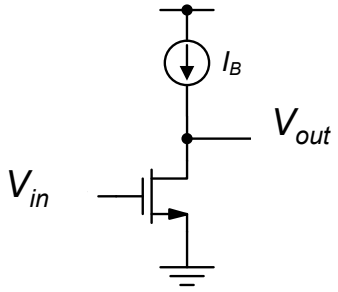
Plot for $I_B=I_D$



- We can increase R_D (and gain) without changing operating point

Infinite gain?

- It is tempting to think we can make R_D nearly "infinitely" large and get close to "infinite" gain
- This is not possible in practice for two reasons
  - Finite dI_d/dV_{ds} of the transistor

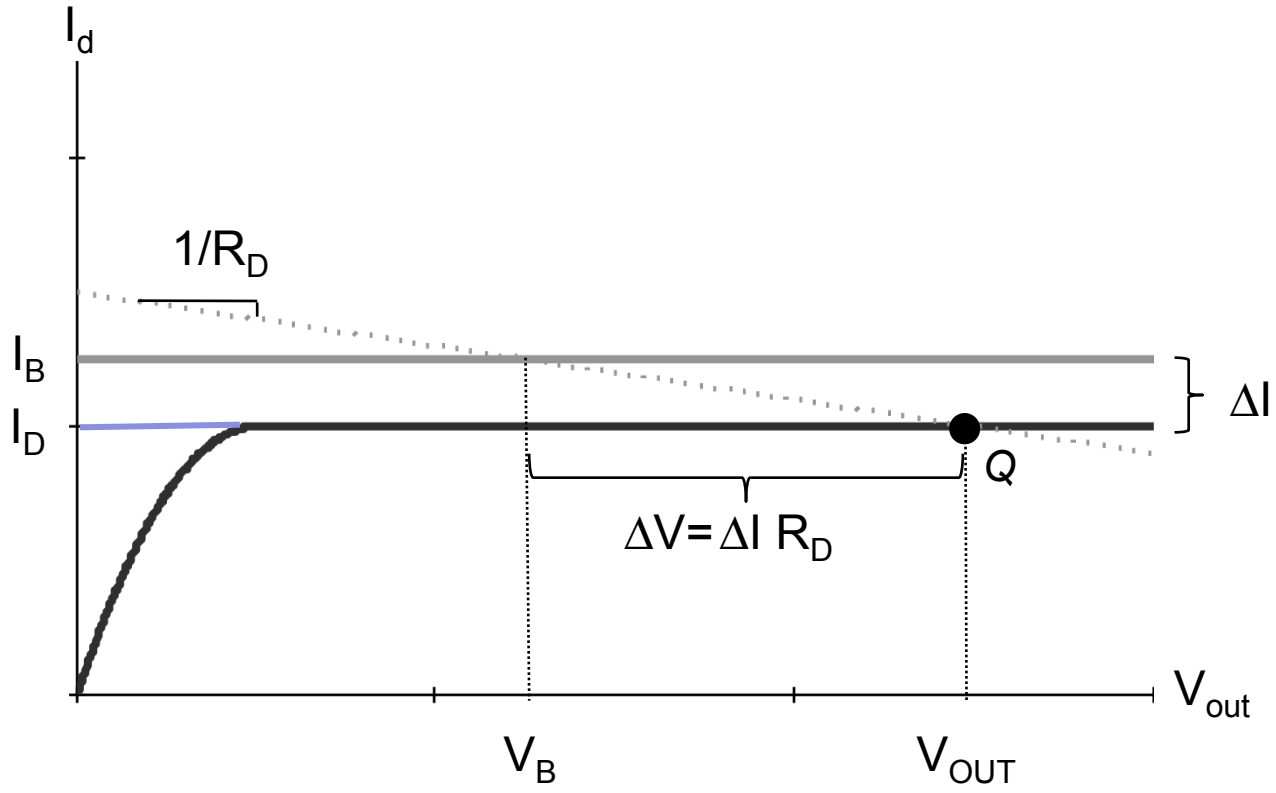


$$A_V = g_m r_o \cong \frac{2I_D}{V_{OV}} \cdot \frac{1}{\lambda I_D} = \frac{2}{\lambda V_{OV}}$$

  - Sensitivity to mismatch between I_D and I_B will render the circuit impractical

Bias point shift due to mismatch in I_B and I_D

- For large values of R_D, it becomes harder to absorb differences between I_D and I_B and still maintain an operating point that is close to the desired value



Solutions to bias point shift issue

- Limit R_D to values such that expected mismatch in bias currents causes acceptable bias point variations
- Feedback
  - Somehow sense V_{OUT} and adjust I_B (or I_D) such that the outputs sits at a proper operating point regardless of mismatch between I_D and I_B
  - More later …

- In a realistic circuit implementation, the auxiliary current source I_B can be built, for example, using a pMOS that operates in saturation
  - More later … (CS stage with current source load)

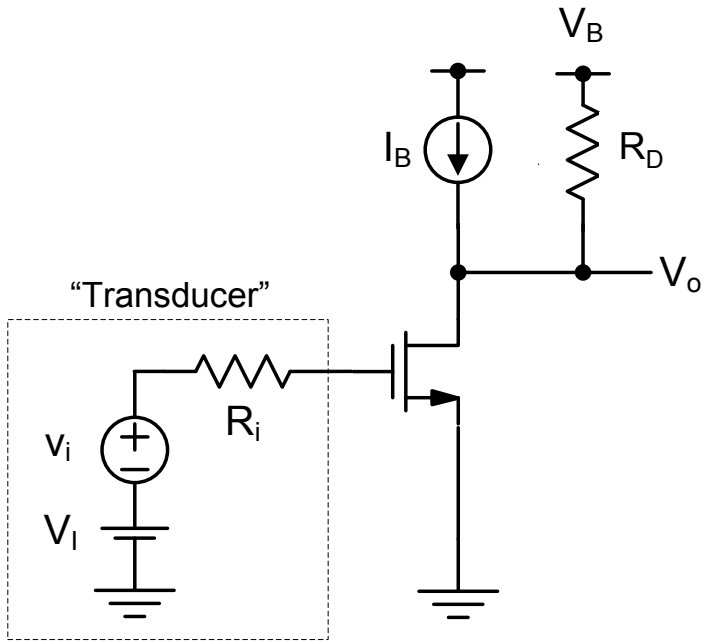
How fast can the CS stage go ?

- There are two perspectives on “how fast” a circuit can go
  - Which one of the two matters more is dependent on the application

- Time domain
  - Apply a transient at the input (e.g. a voltage step), measure how fast the output settles
- Frequency domain
  - Apply a sinusoid at the input, measure the gain and phase of the circuit transfer function across frequency

- Knowing the time domain response, we can estimate the frequency domain response, and vice versa

Common Source Stage revisited

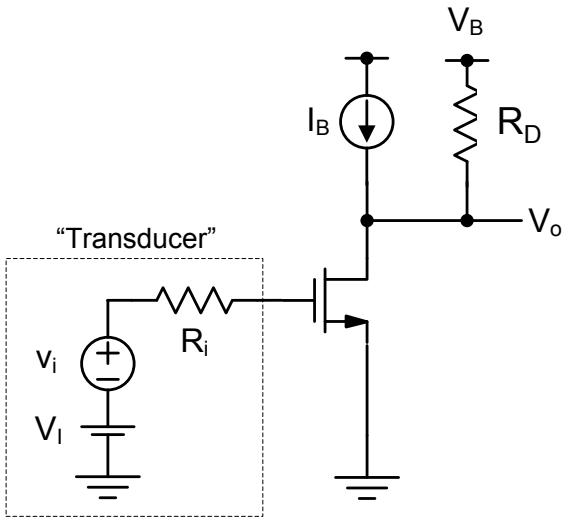


R_i models finite resistance in the driving circuit

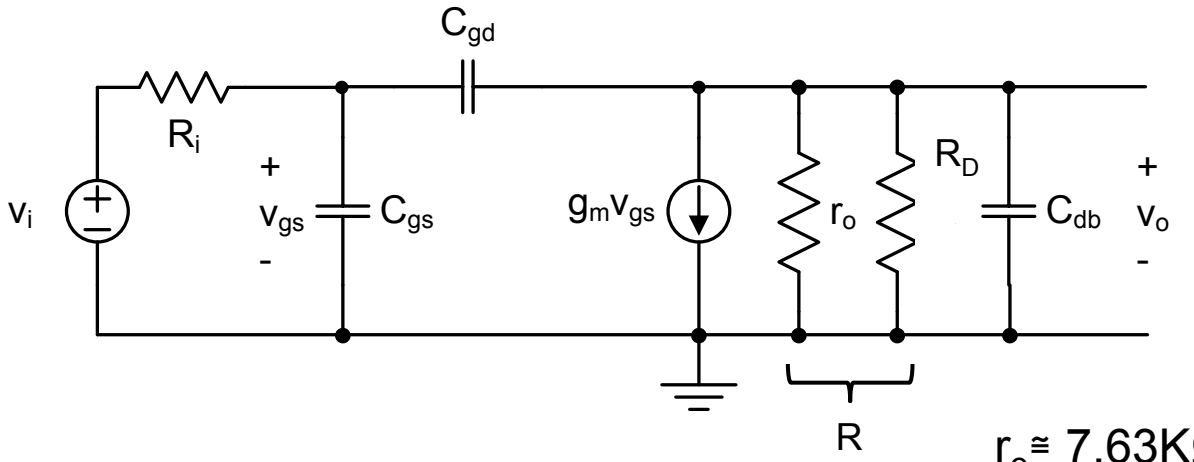
Matlab Design Script

```
%
% C. Talarico
% filename: csdesign.m
% Design of CS amplifier using gm/Id methodology
%

clc; clear all; close all;
addpath('~/gm_ID_starter_kit_2014');
load 180n.mat;

% specs.
av0 = 10; Id = 400e-6; Ri = 10e3; RD = 2e3; Vdd = 1.8; VB = Vdd/2;

% design choice
Ln = 0.18e-6

% calculations
gm = av0/RD
gm_id = gm/Id
wT = lookup(nch, 'GM_CGG', 'GM_ID', gm_id, 'L', Ln);
fT = wT/2/pi
cgd_cgg = lookup(nch, 'CGD_CGG', 'GM_ID', gm_id, 'L', Ln);
cdd_cgg = lookup(nch, 'CDD_CGG', 'GM_ID', gm_id, 'L', Ln);
cgg = gm/wT;
cgd = cgd_cgg*cgg
cdd = cdd_cgg*cgg;
cdb = cdd - cgd
cgs = cgg - cgd
gmro = lookup(nch, 'GM_GDS','GM_ID', gm_id, 'L', Ln)
ro = gmro/gm
% finding input bias
VI = lookupVGS(nch, 'GM_ID', gm_id, 'L', Ln)
% device sizing
id_w = lookup(nch, 'ID_W', 'GM_ID', gm_id, 'L', Ln)
W = Id/id_w

% neglecting ro is not a very accurate assumption
R = (1/RD + 1/ro)^-1
Av0 = gm*R
Av0db = 20*log10(gm*R)

% pole calculations (dominant pole assumption)
b1 = Ri*(cgs + cgd*(1+Av0))+R*(cdb+cgd);
b2 = Ri*R*(cgs*cdb + cgs*cgd + cdb*cgd);
fp1 = 1/2/pi/b1
fp2 = 1/2/pi*b1/b2
% zero calculation
fz = 1/2/pi/cgd*gm
```

What is the speed of the CS ?



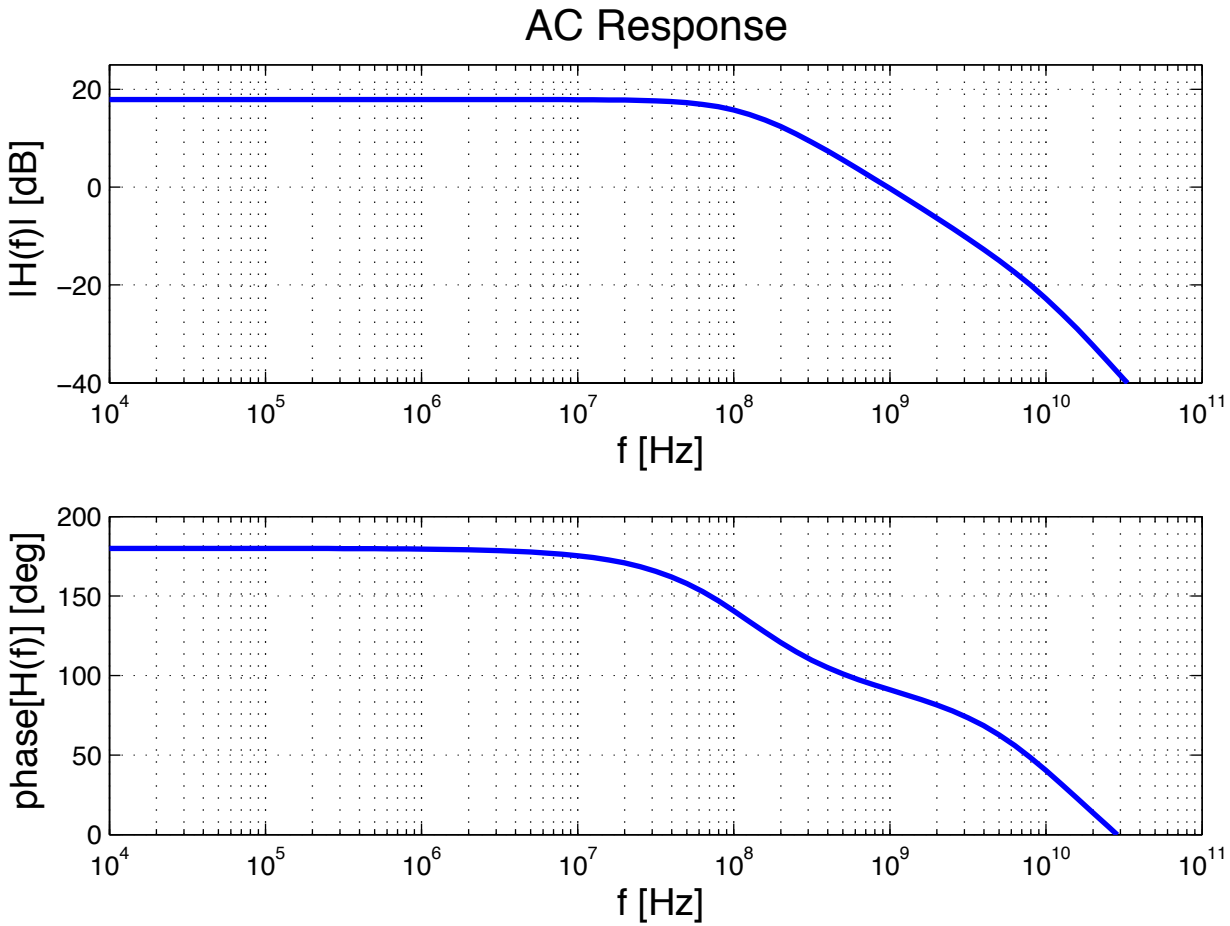
V_{DD} = 1.8 V
$V_B = V_{DD}/2$ = 0.9 V
R_i = 10KΩ
R_D = 2 KΩ
V_I = 0.627 V
I_B = 400 μA
W/L = 21.34 μm/0.18μm



C_{gd}≈10.28 fF
C_{gs}≈ 33.26 fF
C_{db}≈ 15.72 fF

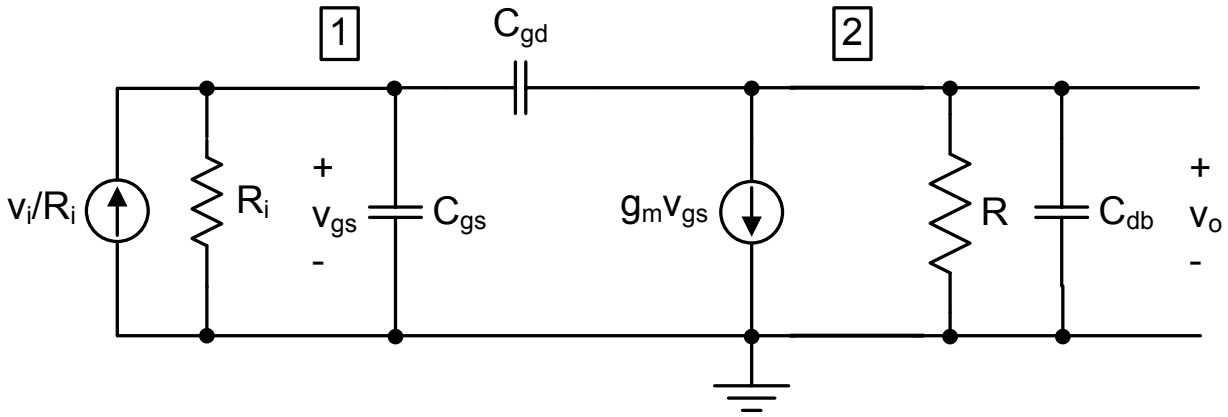
r_o≅ 7.63KΩ
$R = R_D||r_o$ ≅ 1.58KΩ

CS Frequency Response



- There seems to be two poles. Let's analyze the situation in detail.

Exact Analytical Analysis



Applying KCL at nodes 1 and 2, and solving for v_o/v_i yields

$$\frac{v_o(s)}{v_i(s)} = \frac{-g_m R\left(1 - s\frac{C_{gd}}{g_m}\right)}{1 + s\left[\left(C_{db} + C_{gd}\right)R + \left(C_{gs} + C_{gd}\right)R_i + g_m R_i R C_{gd}\right] + s^2 R_i R\left(C_{gs}C_{db} + C_{gd}C_{db} + C_{gs}C_{gd}\right)}$$

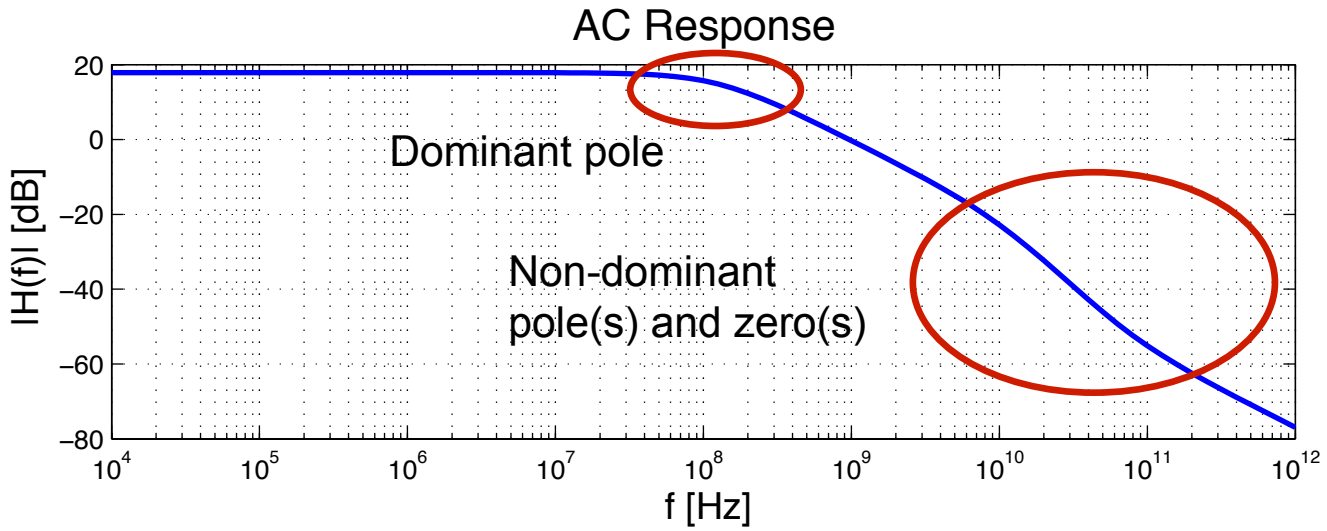
High “entropy” expression. Difficult to get any insight !!!

Issue

- We could in principle use this expression to plot the frequency response of the circuit and compute the 3-dB bandwidth
  - The result would match the Spice simulation result exactly
- There are two issues with going in this direction for hand analysis
  - The procedure is quite tedious…
    - Imagine how complex the equations would get for a multi-transistor circuit
  - The derived expression is useless for reasoning about the circuit from an intuitive design perspective
    - By looking at this equation we cannot easily tell what exactly limits the bandwidth, or how we can improve it

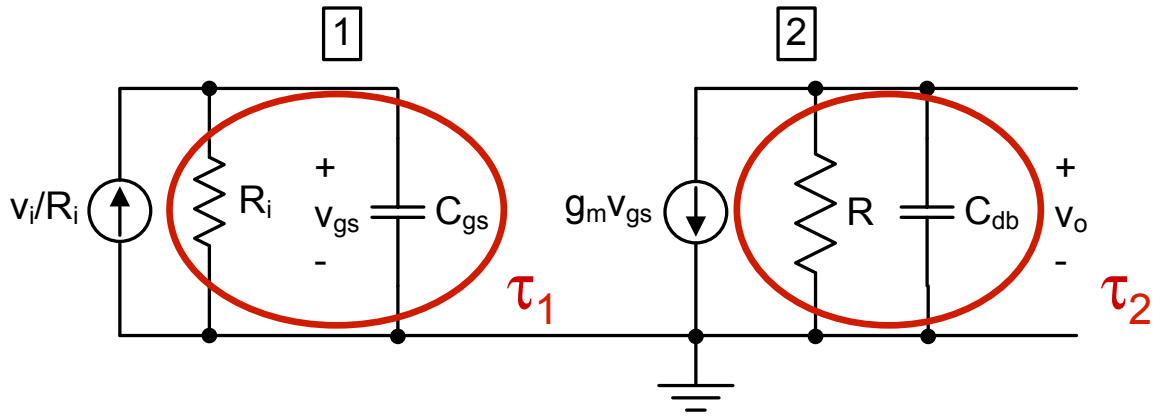
Simulation Result

- Want to have a method that let's us estimate the dominant pole quickly using intuitive methods
  - Without running into high entropy expressions that tell us things we are not interested in…
- Non-dominant, high-frequency poles and zeros may or may not be important
  - If they are, it may be OK to do a little more work



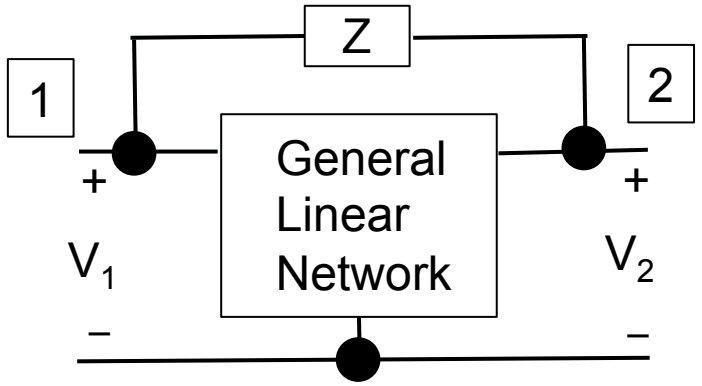
The Culprit

- The main reason for the high complexity in the derived expression is that C_{gd} "couples" nodes 1 and 2
- For C_{gd}=0, the circuit becomes

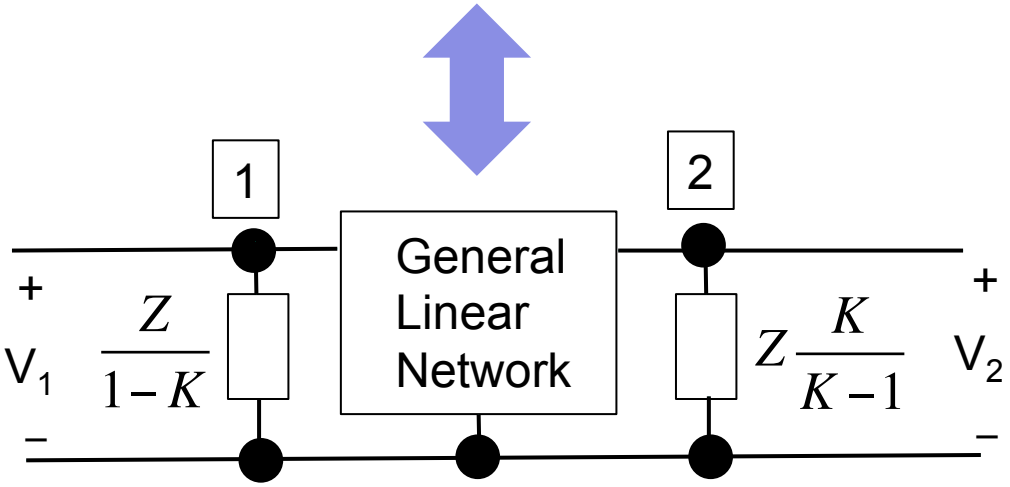


$$\frac{v_o(s)}{v_i(s)} = \frac{v_{gs}(s)}{v_i(s)} \cdot \frac{v_o(s)}{v_{gs}(s)} = \frac{1}{(1+sR_iC_{gs})} \cdot \frac{-g_mR}{(1+sRC_{db})} = -g_mR\frac{1}{(1+s\tau_1)(1+s\tau_2)}$$

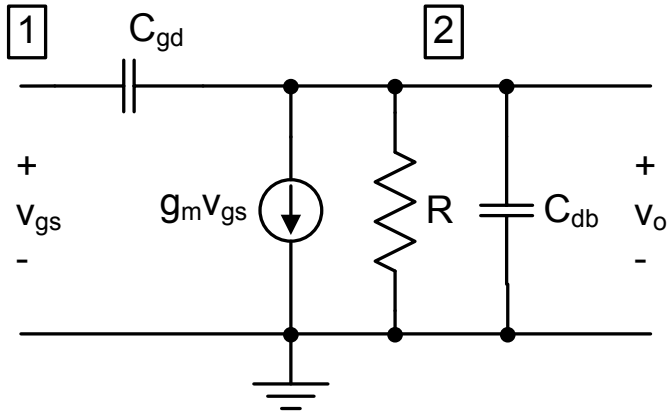
A Promising Trick: Miller Theorem



$$K \equiv \frac{V_2}{V_1}$$



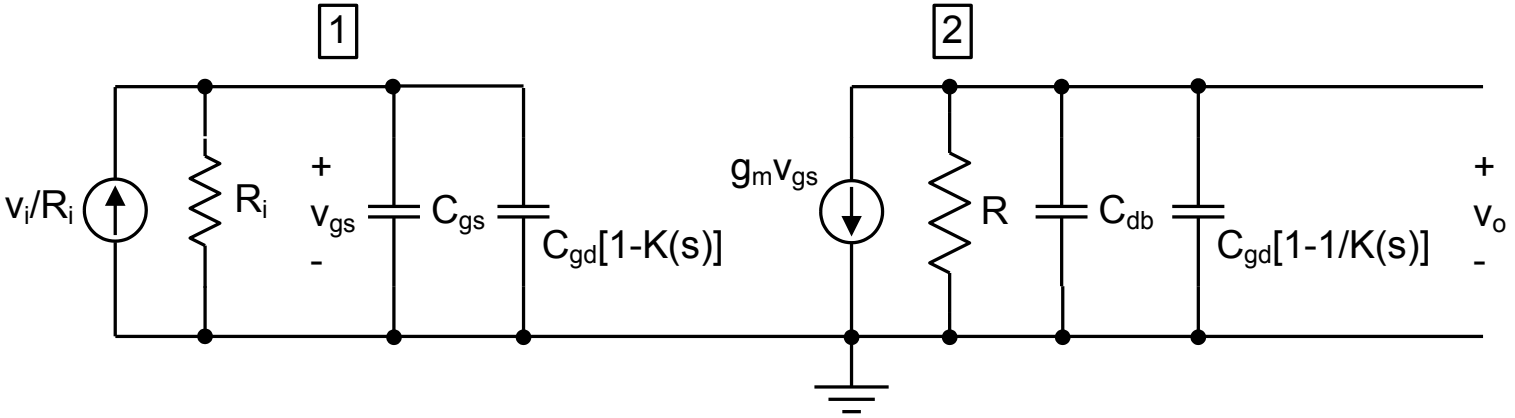
Finding K(s) for Our Circuit



Applying KCL at node 2, and solving for v_o/v_{gs} yields:

$$K(s) = \frac{v_o(s)}{v_{gs}(s)} = -g_m R \left(\frac{1 - s\frac{C_{gd}}{g_m}}{1 + sR(C_{gd} + C_{db})} \right)$$

Circuit After Applying Miller Theorem



$$K(s)=\frac{v_o(s)}{v_{gs}(s)}=-g_m R\left(\frac{1-s\dfrac{C_{gd}}{g_m}}{1+sR(C_{gd}+C_{db})}\right)$$

$$z=+\frac{g_m}{C_{gd}}$$

$$p=-\frac{1}{R(C_{gd}+C_{db})}$$

Intuitively, the zero is caused because at high frequency C_{gd} shorts the gate and drain of the device together, providing a direct path from the amplifier's input to output. Hence, as frequency increases beyond $|w_z|$, the circuit appears to have one less node and one less pole (with C_{gd} acting like a short, C_{gs}, C_{db}, are in parallel). Because the sign of w_z is negative, the zero is in the RHP and therefore causes phase lag (just like a pole) rather than phase lead.

Miller Approximation

As long as

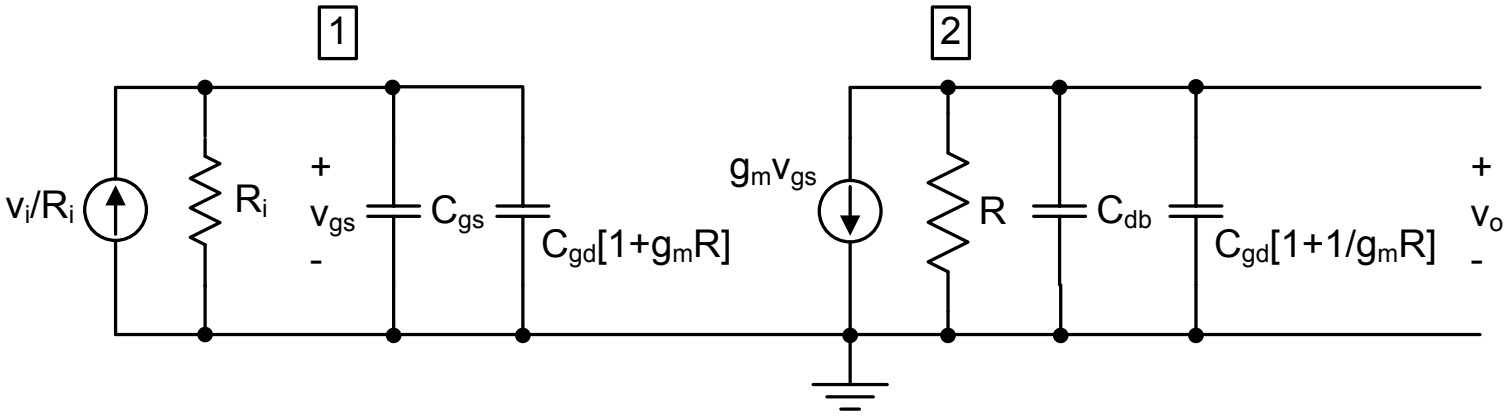
$$\omega << \omega_z = \frac{g_m}{C_{gd}} \qquad \text{and} \qquad \omega << \omega_p = \frac{1}{R\left(C_{gd} + C_{db}\right)}$$

- It is appropriate to approximate

$$K(s) = \frac{v_o(s)}{v_{gs}(s)} = -g_m R \left(\frac{1 - s\dfrac{C_{gd}}{g_m}}{1 + sR(C_{gd} + C_{db})} \right) \cong -g_m R$$

- Approximating the gain term K(s) with its low-frequency value K(0) is called the "Miller approximation"

Resulting Circuit Model



This circuit model suggests that there are two poles

$$p_1 = -\frac{1}{R_i\left[C_{gs} + C_{gd}\left(1 + g_m R\right)\right]} \qquad p_2 = -\frac{1}{R\left[C_{db} + C_{gd}\left(1 + 1/g_m R\right)\right]}$$

- The pole p_2 lies beyond the frequency range for which this model is valid; it must be discarded

$$\omega_{p2} = \frac{1}{R\left[C_{db} + C_{gd}\left(1 + 1/g_m R\right)\right]} \ll \omega_p = \frac{1}{R(C_{db} + C_{gd})}$$

How about p_1?

$$\omega_{p1} = \frac{1}{R_i\left[C_{gs} + C_{gd}\left(1 + g_m R\right)\right]} \overset{?}{<<} \omega_p = \frac{1}{R(C_{db} + C_{gd})}$$

$$\omega_{p1} = \frac{1}{R_i\left[C_{gs} + C_{gd}\left(1 + g_m R\right)\right]} \overset{?}{<<} \omega_z = \frac{g_m}{C_{gd}} = \frac{g_m R}{R C_{gd}}$$

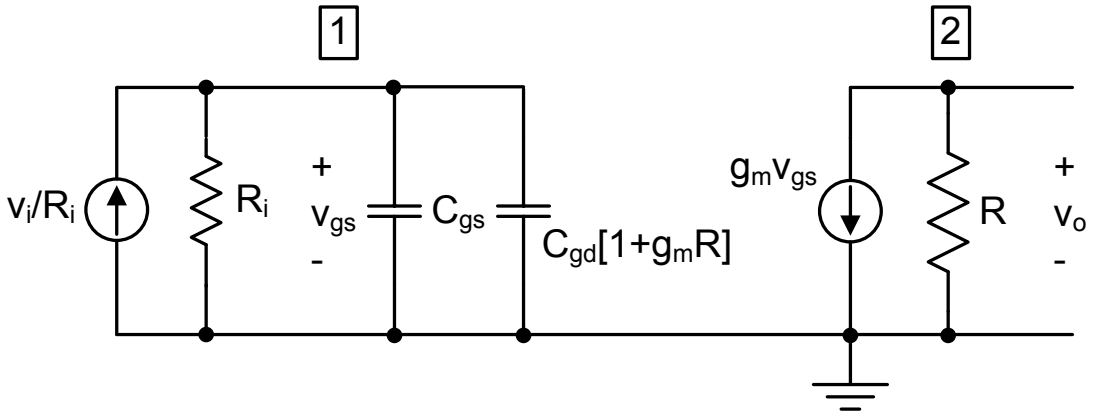
Whether or not these inequalities hold depends on the parameter values of the specific circuit in question

In our example, we have

- R_i=10kΩ > R=2kΩ, $g_m R \cong 7.92$, $C_{gs} > C_{db}, C_{gd}$

Conditions are met !!

Model for Dominant Pole Calculation



- Using calculated values from MATLAB script

$$f_{-3dB} = \frac{1}{2\pi}\frac{1}{R_i[C_{gs}+C_{gd}(1+g_mR)]}$$

$$= \frac{1}{2\pi}\frac{1}{10k\Omega[33.26fF+10.28fF(1+7.92)]} = 127.37MHz$$

- Simulation result was 124.56 MHz; **very good match** !! (less than 3% discrepancy)

Conclusions

- The Miller approximation is a great tool that allows us to calculate the bandwidth of our CS circuit example on the "back of an envelope"
- An important caveat is that the Miller approximation is only useful as long as the dominant time constant is with the input network of the circuit (node 1)
  - Usually the case when R_i is large, and there is no large capacitance attached to v_o
- For calculations, you will typically start by assuming that this condition is met, and later check and make sure that the obtained dominant pole frequency lies indeed far below the pole(s) and zero(s) of K(s)
  - With a little bit of experience you will be able to do this by "inspection"

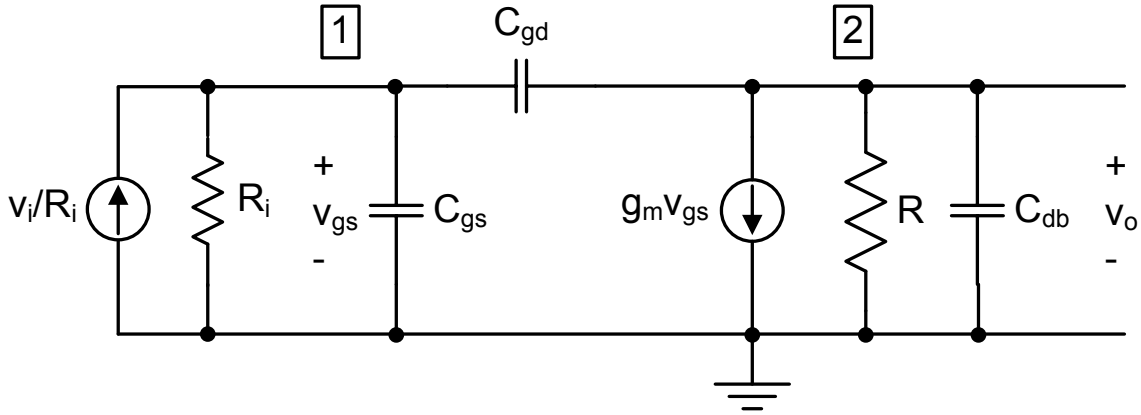
- Very important
  - The Miller approximation allows quick calculation of the dominant pole frequency only
  - It is unsuitable for estimating the non-dominant pole frequency

Dominant Pole Approximation: ZVTC Analysis

- Motivation:
  - we saw that the Miller approximation is a very useful tool that allows us to estimate the -3dB bandwidth of our CS stage quickly and intuitively
  - Wouldn't it be nice to have a similar technique that works for a broader class of circuits?

- The zero-value time constant (ZVTC) method is a tool that meets this demand
- We will continue to use the CS amplifier to illustrate this method, along with its mathematical underpinnings

Analysis Revisited (1)

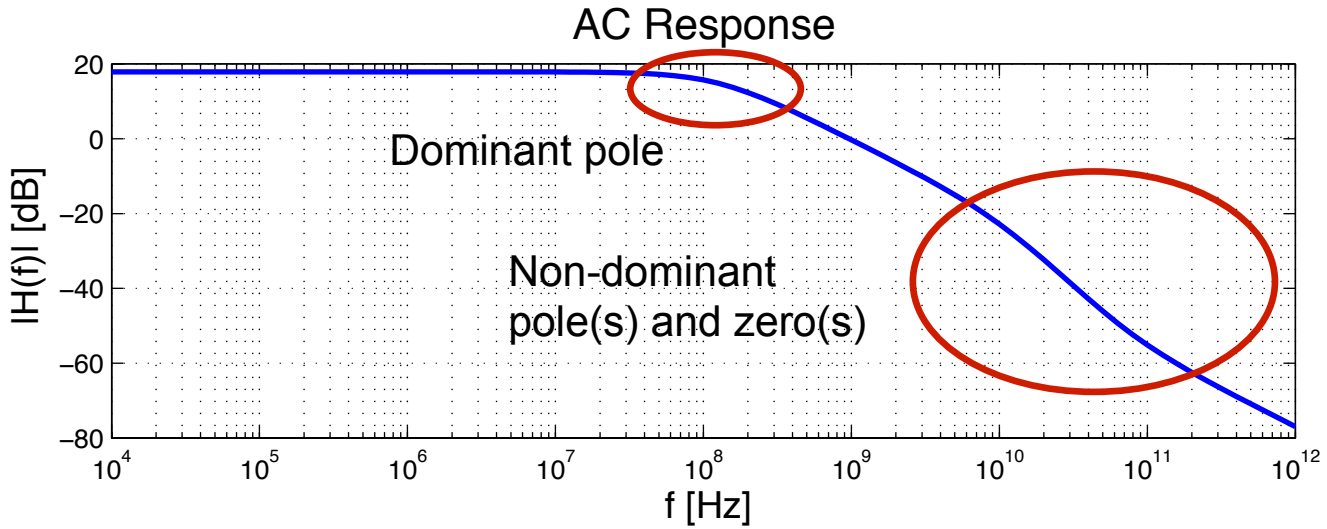


$$\frac{v_o(s)}{v_i(s)} = \frac{-g_m R\left(1 - s\dfrac{C_{gd}}{g_m}\right)}{1 + s\left[\left(C_{db} + C_{gd}\right)R + \left(C_{gs} + C_{gd}\right)R_i + g_m R_i R C_{gd}\right] + s^2 R_i R\left(C_{gs}C_{db} + C_{gd}C_{db} + C_{gs}C_{gd}\right)}$$

$$= a_{v0}\frac{\left(1 - \dfrac{s}{z}\right)}{1 + b_1 s + b_2 s^2}$$

Analysis Revisited (2)

- We know that
  - The transfer function of our circuit has a dominant pole that sets the -3dB bandwidth
  - The non-dominant pole and zero have little influence on the -3dB bandwidth of the circuit
- Can we somehow use this fact to simplify the analysis?
  - Without circuit-specific “tricks” like the Miller approximation



Dominant Pole Approximation (1)

- If our goal is to estimate the -3dB frequency only, we can discard the zero and write

$$\frac{v_o(s)}{v_i(s)} = \frac{a_{v0}\left(1-\frac{s}{z}\right)}{1+b_1 s+b_2 s^2} \cong \frac{a_{v0}}{1+b_1 s+b_2 s^2}$$

- Next, use the fact that $|p_2|>>|p_1|$, where p_2 is the non-dominant pole and p_1 is the dominant pole that sets the -3dB frequency

$$\frac{v_o(s)}{v_i(s)} \cong \frac{a_{v0}}{\left(1-\frac{s}{p_1}\right)\cdot\left(1-\frac{s}{p_2}\right)} = \frac{a_{v0}}{1-\frac{s}{p_1}-\frac{s}{p_2}+\frac{s^2}{p_1 p_2}} \cong \frac{a_{v0}}{1-\frac{s}{p_1}+\frac{s^2}{p_1 p_2}}$$

Dominant Pole Approximation (2)

- We can now compare to the original expression to find

$$\frac{v_o(s)}{v_i(s)} \cong \frac{a_{v0}}{1-\frac{s}{p_1}+\frac{s^2}{p_1 p_2}} \cong \frac{a_{v0}}{1+b_1 s+b_2 s^2} \quad \Rightarrow \mathrm{p}_1 \cong -\frac{1}{b_1} \quad \mathrm{p}_2 \cong \frac{1}{p_1 b_2} = -\frac{b_1}{b_2}$$

- This means that in order to estimate the -3dB bandwidth of the circuit, all we need to know is b_1!

$$\frac{v_o(s)}{v_i(s)} \cong \frac{a_{v0}}{1-\frac{s}{p_1}} \quad \Rightarrow \omega_{\text{-}3dB} \cong |p_1| \cong \left|\frac{1}{b_1}\right|$$

b_1 in Our Circuit

$$\frac{v_o(s)}{v_i(s)} = \frac{-g_m R\left(1 - s\frac{C_{gd}}{g_m}\right)}{1 + s\left[\left(C_{db} + C_{gd}\right)R + \left(C_{gs} + C_{gd}\right)R_i + g_m R_i R C_{gd}\right] + s^2 R_i R\left(C_{gs}C_{db} + C_{gd}C_{db} + C_{gs}C_{gd}\right)}$$

Looks familiar?

$$b_1 = \left(C_{db} + C_{gd}\right)R + \left(C_{gs} + C_{gd}\right)R_i + g_m R_i R C_{gd} = RC_{db} + RC_{gd} + R_i C_{gs} + \left(1 + g_m R\right)R_i C_{gd}$$

Plug in numbers for our example to see if this works…

$$b_1 = 1.58k\Omega \cdot 15.72\,fF + 1.58k\Omega \cdot 10.28\,fF + 10k\Omega \cdot 33.26\,fF + \left(1 + 7.92\right)10k\Omega \cdot 10.28\,fF$$
$$= 24.84\,ps + 16.24\,ps + 332.60\,ps + 916.98\,ps = 1290.7\,ps$$

$$f_{-3dB} = \frac{1}{2\pi}\frac{1}{1290.66\,ps} = 123.37\,MHz$$

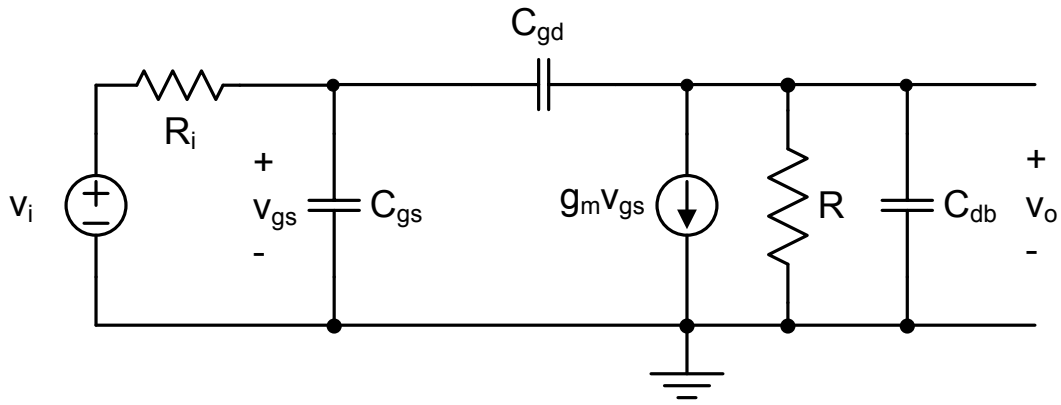
Very good match !
(Spice: 124.56 MHz, Miller: 127.37 MHz)

Zero-Value Time Constant Analysis

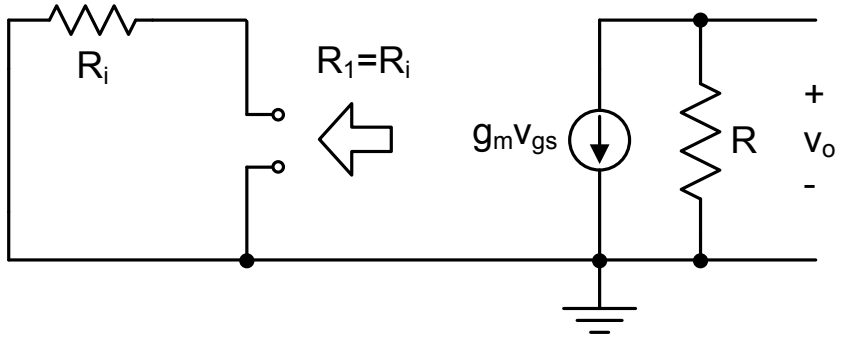
- A step-by-step circuit analysis method that allows us to determine b_1 (and only b_1) without solving for the complete transfer function!
- Here's how it works
  - Remove all but one capacitor (C_j)
  - Short independent voltage sources
  - Remove independent current sources
  - Calculate resistance seen by capacitor (R_j) and compute $t_j=R_jC_j$
  - Repeat above steps for all remaining capacitors in the circuit
  - The sum of all t_j is equal to b_1

$$b_1 = \sum \tau_j \qquad \Rightarrow \omega_{-3dB} \cong \left|\frac{1}{b_1}\right| = \frac{1}{\sum \tau_j}$$

Example (1)



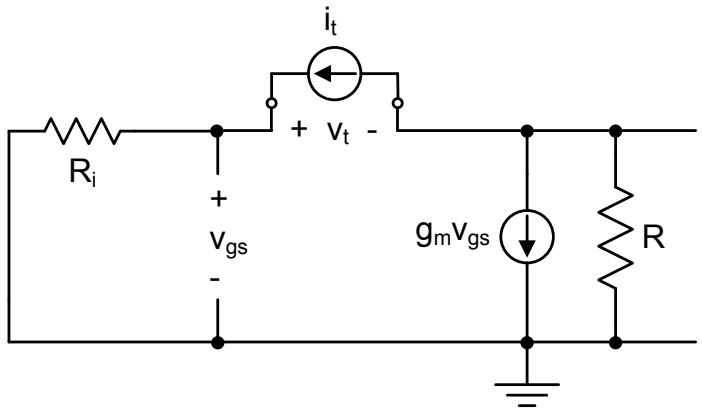
- Step 1:



$$\tau_1 = R_i C_{gs}$$

Example (2)

- Step 2:



A little more tricky, but any linear circuit method will do
(e.g. apply test current (i_t), write expression for v_t, find $R=v_t/i_t$

$$v_{gs} = R_i \cdot i_t$$

$$R_2 = \frac{v_t}{i_t} = \frac{v_{gs} + R(g_m v_{gs} + i_t)}{i_t} = \frac{i_t R_i + R(g_m i_t R_i + i_t)}{i_t} = R_i + R + g_m R R_i$$

"sum + product x g_m"

$$\tau_2 = (R_i + R + g_m R R_i) C_{gd}$$

Example (3)

- Step 3: $R_3 = R \qquad \tau_3 = RC_{db}$
- Step 4: Add up all time constants

$$\sum \tau_j = \tau_1 + \tau_2 + \tau_3 = R_i C_{gs} + \left(R + R_i + g_m R R_i\right) C_{gd} + RC_{db}$$

- Step 5: Compute estimate of -3dB frequency

$$\omega_{-3dB} \cong \frac{1}{\sum \tau_j}$$

- Exactly the same result we found on slide 37…

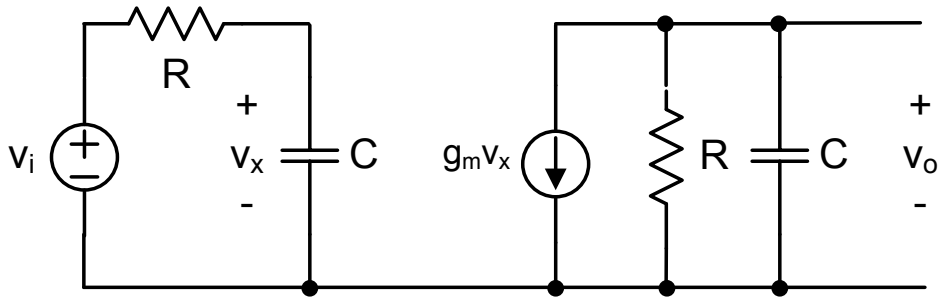
Important Notes on ZVTC (1)

- The key advantages of this method are
  - It provides an excellent shortcut for finding the -3dB frequency of a circuit
  - In addition, the method provides us with insight about the limiting time constants in our circuit!
- Whenever you apply the ZVTC method, it is important to remember the assumptions for which it is accurate
  - The circuit has a dominant pole
  - The circuit does not have any zeros in the vicinity of its -3dB frequency
- The time constants computed in the ZVTC method do not correspond to poles!
  - Remember that the sum of the time constants is equal to b_1

Important Notes on ZVTC (2)

- When the underlying assumptions are not precisely met, it may still be "OK" to work with ZVTC
  - Provided that you clearly understand what you are doing…
- Example 1: AC coupling caps or bypass caps
  - Meant to be "shorts" at high frequencies, and do not degrade the signal bandwidth
  - Typically OK to discard these caps to find the "upper corner frequency" of the circuit
- Example 2: Multiple poles of similar (or same) magnitude
  - See next page

Two-Pole Example (1)



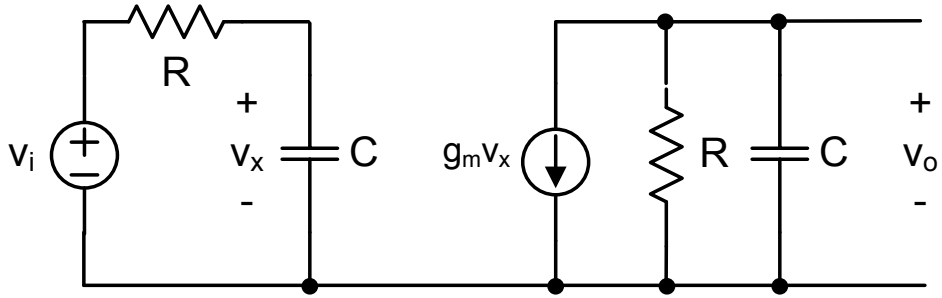
- Exact calculation of -3dB frequency

$$\frac{v_o(s)}{v_i(s)} = \frac{-g_m R}{(1+sRC)^2}$$

We do not have a dominant pole !!

$$\frac{1}{\sqrt{2}} = \frac{1}{1+\omega_{-3dB}^2 R^2 C^2} \qquad \Rightarrow \omega_{-3dB} = \frac{1}{RC}\sqrt{\sqrt{2}-1} = \frac{0.64}{RC}$$

Two-Pole Example (2)



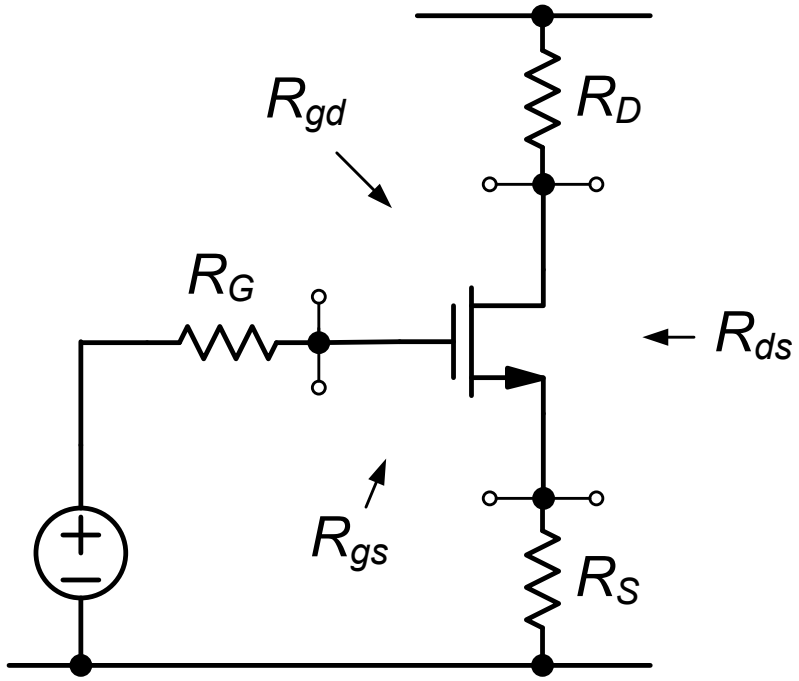
ZVTC method

$$\omega_{-3dB} \cong \frac{1}{\sum \tau} = \frac{1}{RC + RC} = \frac{0.5}{RC}$$

$$Error = \frac{0.5 - 0.64}{0.64} = -22\%$$

- ZVTC bandwidth estimates tend to be conservative
  - Actual bandwidth is almost always at least as high as estimate

Useful Expressions



$$R_{gs} = \frac{R_G + R_S}{1 + g_m R_S}$$

$$R_{ds} = r_0 \parallel \frac{R_D + R_S}{1 + g_m R_S}$$

$$R_{gd} = R_G + R_D + G_m R_G R_D$$

$$G_m = \frac{g_m}{1 + g_m R_S}$$

Hspice Deck

```
* Common source amplifier
* filename: commonsource.sp
* C. Talarico, Fall 2014

*** device model
.include ../ece696008.mod

*** useful options
.option post brief nomod accurate

*** netlist
vdd vdd 0 1.8
vb  vb 0 0.9
ib  vdd vo 400u
vi  vi  0   dc  0.627
+           ac  1
mn1 vo  vg  0   0   nmos   w=21.34u  l=0.18u
RD  vb vo  2k
Ri  vi vg  10K

*** analysis
.op
.ac dec 10 100 1T
.pz v(vo) vi
*** measurements
.measure AC av0 find V(vo) at 1K
.measure AC av0db find vdb(vo) at 1K
.measure AC f3db when Vdb(vo)='av0db - 3'

.end
```

Plotting Hspice Results in Matlab

```
%
% cs_plot.m
%
clear all; close all;
format short eng
addpath('/usr/local/MATLAB/personal/HspiceToolbox');
y = loadsig('./commonsource.ac0');
lssig(y)

figure(1);
subplot(2,1,1);
freq = evalsig(y,'HERTZ');
vo = evalsig(y,'v_vo');
magdb = 20*log10(abs(vo));
phase = 180*unwrap(angle(vo))/pi;
semilogx(freq, magdb,'linewidth',2, 'color', 'b', 'linestyle', '-');
grid on;
ylabel(' |H(f)| [dB]', 'Fontsize', 14);
xlabel(' f [Hz]', 'Fontsize', 14);
title('AC Response', 'Fontsize', 16);
xmin = 1e4;
xmax = 1e11;
xlim([xmin xmax]);
ymax = 25;
ymin = -40;
ylim([ ymin ymax]);
subplot(2,1,2);
semilogx(freq, phase,'linewidth',2, 'color', 'b', 'linestyle', '-');
grid on;
ylabel(' phase[H(f)] [deg]', 'Fontsize', 14);
xlabel(' f [Hz]', 'Fontsize', 14);
xmin = 1e4;
xmax = 1e11;
xlim([xmin xmax]);
ymax = 200;
ymin = 0;
ylim([ ymin ymax]);
av0 = abs(vo(1))
av0db = magdb(1)
f3db = interp1(magdb, freq, magdb(1)-3, 'spline')
```

Simulated DC Operating Point

```
element  0:mn1
 model    0:nmos
 region     Saturati
  id       392.1556u
  ibs        0.
  ibd        0.
  vgs      627.0000m
  vds      915.6889m
  vbs        0.
  vth      486.0140m
  vdsat    115.1878m
  vod      140.9860m
  beta      42.1550m
  gam eff  585.0614m
  gm         4.9201m
  gds      127.1176u
  gmb        1.1709m
  cdtot     29.5868f
  cgtot     43.5028f
  cstot     56.0268f
  cbtot     49.5585f
  cgs       30.8630f
  cgd       10.2858f
```

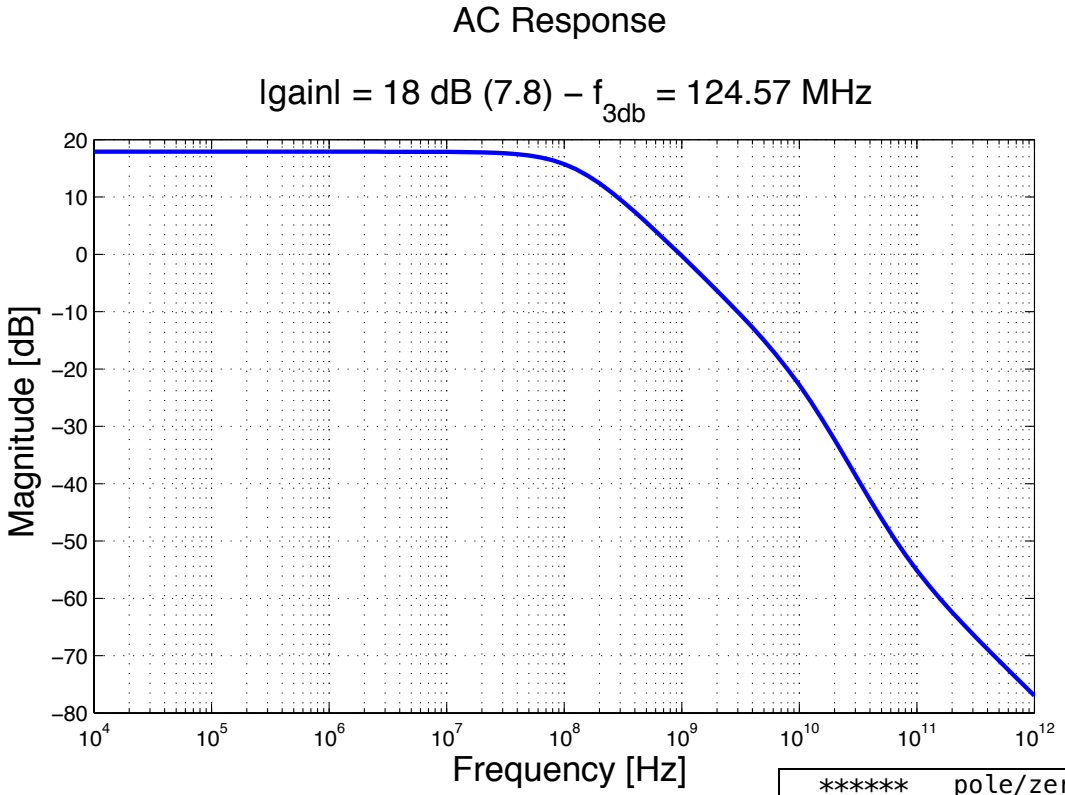
$\texttt{cdtot} \equiv C_{gd} + C_{db}$
$\texttt{cgtot} \equiv C_{gs} + C_{gd} + C_{gb}$
$\texttt{cstot} \equiv C_{gs} + C_{sb}$
$\texttt{cbtot} \equiv C_{gb} + C_{sb} + C_{db}$
$\texttt{cgs} \equiv C_{gs}$
$\texttt{cgd} \equiv C_{gd}$

Good Agreement !

Design values:

$g_m = 5mS$
$c_{dd} = 26$ fF
$c_{gg} = 43.53$ fF
$c_{gd} = 10.28$ fF
$c_{gs} = c_{gg} - c_{gd} = 43.53 - 10.28 = 33.36$ fF

Simulated AC Response




```
% pole calculations (dominant pole assumption)
b1 = Ri*(cgs + cgd*(1+Av0))+R*(cdb+cgd);
b2 = Ri*R*(cgs*cdb + cgs*cgd + cdb*cgd);
fp1 = 1/2/pi/b1
fp2 = 1/2/pi*b1/b2
% zero calculation
fz = 1/2/pi/cgd*gm
```

The design is essentially right on target !!
Typical discrepancies are no more than 10%-20%

```
******   pole/zero analysis
input =  0:vi           output = v(vo)

      poles (rad/sec)                poles ( hertz)
real            imag            real            imag
-784.661x       0.              -124.883x       0.
-67.7746g       0.              -10.7867g       0.

      zeros (rad/sec)                zeros ( hertz)
real            imag            real            imag
469.117g        0.              74.6622g        0.
```

- Calculated values: $|A_{V0}| \cong 7.92$ (17.98 dB); fp1≅123.30MHz; fp2≅12.37GHz; fz≅77.43GHz

Matlab Script to plot the Simulation Results

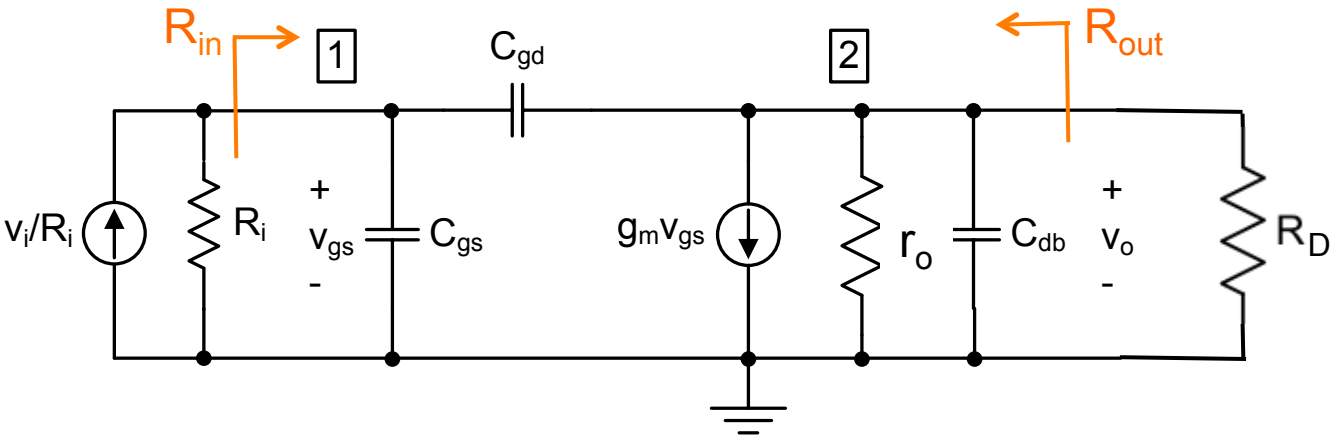
```
%
% cs_cuteplot.m
%
clear all; close all;
format short eng
addpath('/usr/local/MATLAB/personal/HspiceToolbox');
y = loadsig('./commonsource.ac0');
lssig(y)

figure(1);
freq = evalsig(y,'HERTZ');
vo = evalsig(y,'v_vo');
magdb = 20*log10(abs(vo));
phase = 180*unwrap(angle(vo))/pi;
semilogx(freq, magdb,'linewidth',2, 'color', 'b', 'linestyle', '-');
grid on;
ylabel(' Magnitude [dB]', 'Fontsize', 16);
xlabel(' Frequency [Hz]', 'Fontsize', 16);
xmin = 1e4;
xmax = 1e12;
xlim([xmin xmax]);
av0 = abs(vo(1))
av0db = magdb(1)
f3db = interp1(magdb, freq, magdb(1)-3, 'spline')
% Annotate title
str1 = sprintf('AC Response\n');
str2 = sprintf('|gain| = %0.2g dB (%0.2g) - f_{3db} = %3.2f MHz', av0db, av0, f3db*1e-6);
str = {str1, str2};
title(str, 'fontsize', 16);
```

Practical Design Considerations (1)

- If the load capacitance is modest and the source resistance is high, the Miller effect is likely to be the major limitation in the amplifier BW
  - BW can be improved by sizing the transistor as small as possible. For a fixed current this implies that the device will exhibit a relatively large $V_{OV.}$ This has two drawbacks:
    - To keep the transistor in saturation we need a higher DC voltage drop across the transistor (reduced headroom)
    - Mobility degradation
- If the load capacitance is large and the source resistance is low, the output time constant will dominate and become the major limitation in the amplifier BW
  - Large device width and small values of V_{OV} are preferred (having the device operating near sub threshold gives the best gain-BW tradeoff)
- For low-gain, high frequency, it may be desirable to use resistor loads (if they do not require much silicon area) because they have less parasitic capacitances associated with them.

CS summary

- The CS stage is a “decent” (voltage controlled) current source (⟺ “decent” trans-conductance amplifier)
- The CS stage can be used to realize a basic voltage amplifier, but it makes a good voltage amplifier only when terminated with a high impedance
  - $R_{in} = \infty$ (very high)
  - $R_{out} = r_o$ (moderately high)

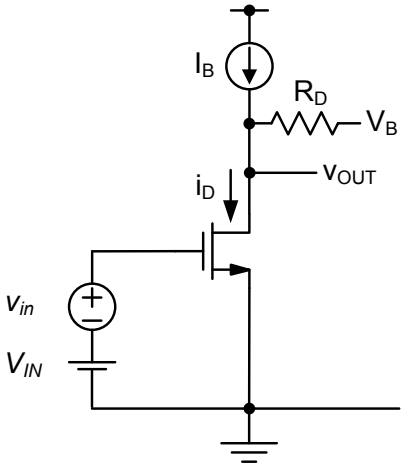


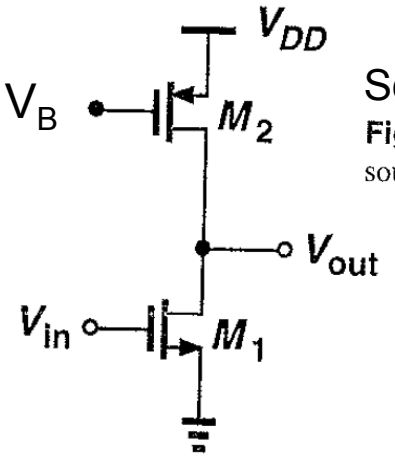
More CS stage variations …

- CS with Current-Source Load (practical implementation)
- CS with Diode-Connected Load (“ratiometric” CS stage)
- CS with Degeneration

CS with Current-Source Load

- Realistic implementation of the CS basic stage with improved drain biasing scheme ⟶ Use a pMOS operating in saturation as load





Source: Razavi

Figure 3.14 CS stage with current-source load.

$$A_V = -g_{m1}(r_{o1} \parallel r_{o2})$$

$$R_{in} = \infty$$

$$R_{out} = r_{o1} \parallel r_{o2}$$

Design Considerations

- The upper side of the output signal swing $V_{DD}-|V_{DS2min}| = V_{DD} - (|V_{GS2}|-|V_{T2}|)$ can be improved by increasing the width of M_2
- If r_{o2} is not sufficiently large (for the desired gain), the length of M_2 can be increased. Increasing L_2 while keeping W_2 constant increases r_{o2} and hence the voltage gain, but at the cost of a higher $|V_{DS2}|$ required to maintain M_2 in saturation. To maintain the same overdrive voltage both W and L must be increased.
  - The penalty is the large capacitance ($C_{gs2}+C_{db2}$) introduced by M_2 at the output node

$$V_{OV} = \sqrt{2\frac{\mu C_{ox}}{I_D}\left(\frac{L}{W}\right)}$$

- The intrinsic gain of M_1 can be increased by increasing L_1. Since r_o is proportional to L/I_D the intrinsic gain increases because λ depends more strongly on L than g_m does:

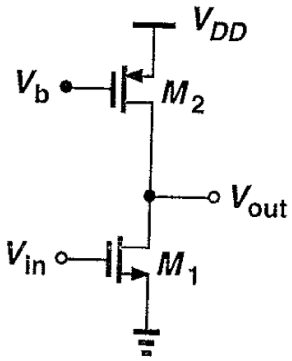
$$g_{m1}r_{o1} = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)_1 I_D}\cdot\frac{1}{\lambda I_D}$$

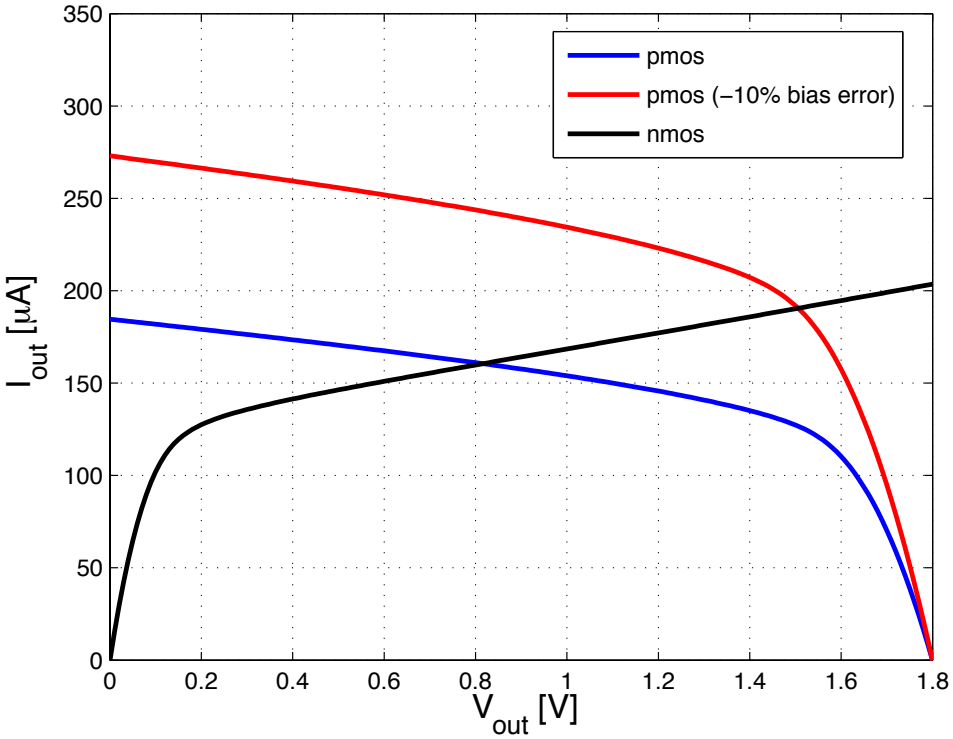
NOTE: $g_m r_o$ decreases as I_D increases

However, if W_1 is not increased proportionally, the overdrive voltage $V_{GS1}-V_{T1}$ increases, limiting the "lower side" (V_{DS1min}) of the output signal swing

Issue

- The output bias voltage V_{OUT} of the circuit is not well defined. The stage is reliably biased only if a feedback loop forces V_{OUT} to a known value. To be continued …
- Since the current through the two MOS must stay the same, even a small error will cause a large shift of the bias voltage V_{OUT} and push one of the transistor away from saturation

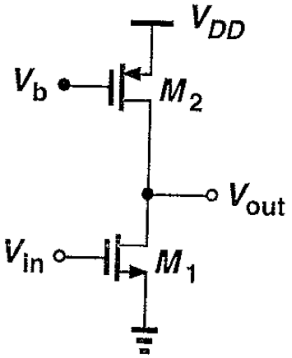




CS with current source load - Example (1)

- V_{DD}=1.8V; I_D=150µA; V_{OUT}=0.8V

  L = 0.18µm



V_{GS1} = 0.68 V
g_{m1} = 1.5 mS
W_1 = 4.94µm
r_{o1} = 23.23 KΩ
A_V = 19.57

$|V_{GS2}|$ = 0. 84 V
g_{m2} = 0.76 mS
W_2 = 4.94µm
r_{o2} = 28.90 KΩ

```
%
% C. Talarico
% filename: cscs_design.m
% Design bias for CS with current source load
%

clc; clear all; close all;
addpath('~/gm_ID_starter_kit_2014');

% The NMOS
load 180n.mat;
Ln = 0.18e-6
Vds = 0.8
Ibias = 150e-6
for Vgs=0.5:0.01:0.9
  Id = lookup(nch, 'ID', 'VGS', Vgs, 'VDS', Vds, 'L', Ln);
  if (Id >= Ibias)
    Id
    Vgs1=Vgs
    break
   end
end
gm1 = lookup(nch, 'GM', 'VGS', Vgs, 'VDS', Vds, 'L', Ln)
gm_id = gm1/Id
id_w = lookup(nch, 'ID_W', 'GM_ID', gm_id, 'L', Ln)
W1 = Id/id_w
gmro1 = lookup(nch, 'GM_GDS','GM_ID', gm_id, 'L', Ln)
ro1 = gmro1/gm1

% The PMOS
load 180p.mat
Ln = 0.18e-6
Vds = 0.8
Ibias = 150e-6
for Vgs=0.5:0.01:1.2
  Id = lookup(pch, 'ID', 'VGS', Vgs, 'VDS', Vds, 'L', Ln);
  if (Id >= Ibias)
    Id
    Vgs2=Vgs
    break
   end
end
gm2 = lookup(pch, 'GM', 'VGS', Vgs, 'VDS', Vds, 'L', Ln)
gm_id = gm2/Id
id_w = lookup(pch, 'ID_W', 'GM_ID', gm_id, 'L', Ln)
W2 = Id/id_w
gmro2 = lookup(pch, 'GM_GDS','GM_ID', gm_id, 'L', Ln)
ro2 = gmro2/gm2

AV = gm1/(1/ro1+1/ro2)
```

CS with current source load - Example (2)

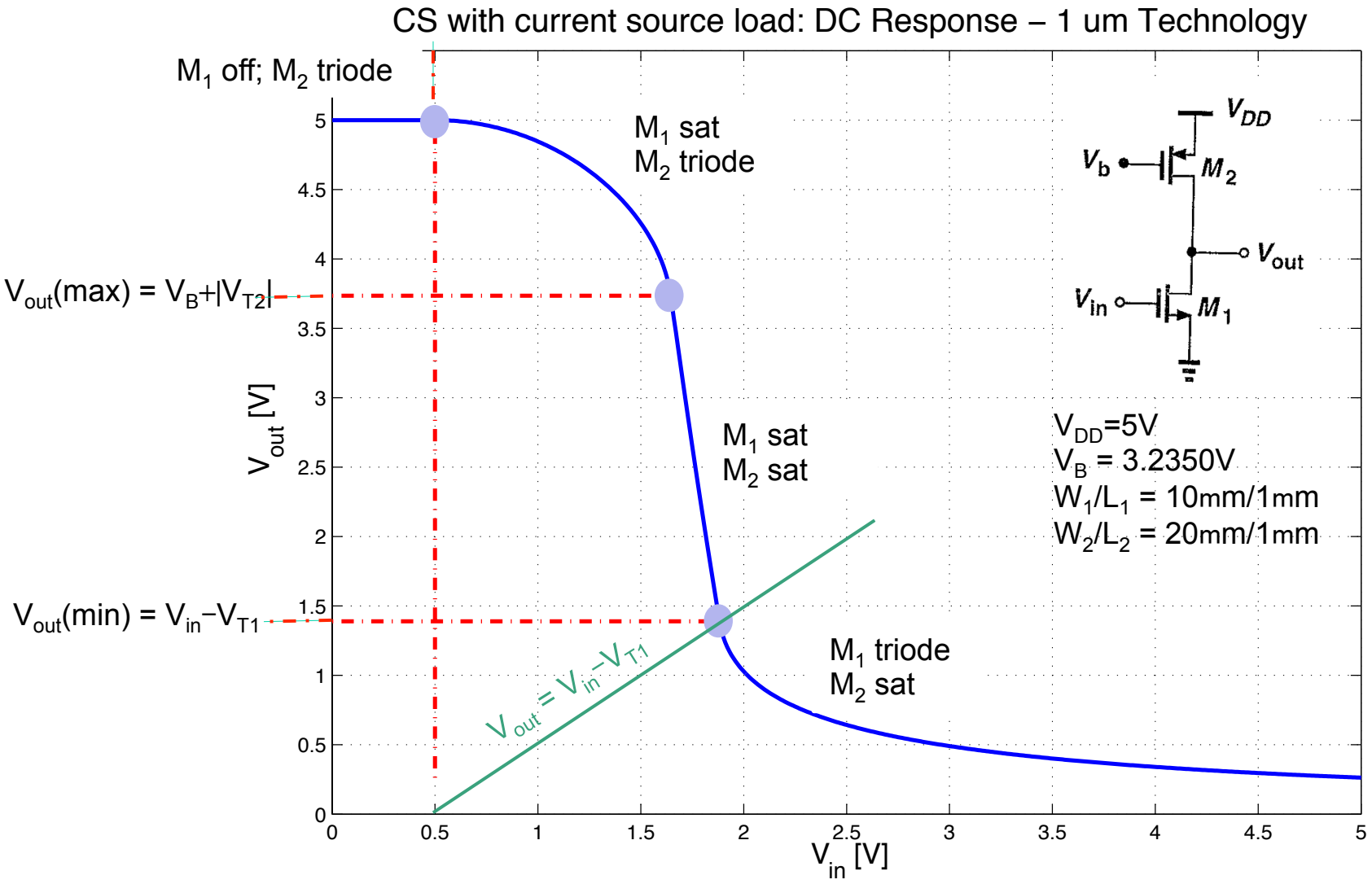
```
* cs with current source load
* filename: cscs.sp
* C. Talarico, Fall 2014

*** device model
.include ../ece696008.mod

*** useful options
.option post brief nomod
.param supply = 1.8

*** circuit
vdd vdd 0 'supply'
vi  vi  0   dc  0.68
+           ac  1
vb  vb 0 0.96
m1 vo  vg  0   0     nmos   w=4.94u  l=0.18u
m2 vo  vb  vdd  vdd  pmos   w=4.94u  l=0.18u
Ri  vi vg  10K
*** analysis and measurements
.op
.ac dec 10 100 1T
.measure AC av0 find V(vo) at 1K
.measure AC av0db find vdb(vo) at 1K
.measure AC f3db when Vdb(vo)='av0db - 3'

.alter amplifier with error
* -10% error
vb  vb 0 '0.9*0.96'

.end
```

```
element  0:m1       0:m2
 model    0:nmos     0:pmos
 region     Saturati   Saturati
  id       160.5067u -160.5067u
  ibs        0.          0.
  ibd        0.          0.
  vgs      680.0000m -840.0000m
  vds      816.2602m -983.7398m
  vbs        0.          0.
  vth      485.7988m -498.1706m
  vdsat    144.4580m -277.1348m
  vod      194.2012m -341.8294m
  beta       9.9652m    2.7793m
  gam eff  583.1781m  531.4120m
  gm         1.5079m  800.3570u
  gds       43.5979u   33.7757u
  gmb      355.1684u  247.3357u
  cdtot      7.1177f    7.6254f
  cgtot     10.1191f   10.7026f
  cstot     13.2586f   13.4306f
  cbtot     11.9484f   11.4786f
  cgs        7.2275f    7.3157f
  cgd        2.3756f    3.1800f


 av0=  19.4891
 av0db=  25.7959
 f3db= 217.4707x
```

```
element  0:m1       0:m2
 model    0:nmos     0:pmos
 region     Saturati     Linear
  id       190.5148u -190.5148u
  ibs        0.          0.
  ibd        0.          0.
  vgs      680.0000m -936.0000m
  vds        1.5059  -294.0804m
  vbs        0.          0.
  vth      479.7683m -507.9848m
  vdsat    147.7910m -337.7712m
  vod      200.2317m -428.0152m
  beta       9.9623m    2.7282m
  gam eff  583.1781m  531.4120m
  gm         1.6650m  676.2354u
  gds       43.9788u  236.7371u
  gmb      388.5510u  222.4197u
  cdtot      6.7171f    8.8003f
  cgtot     10.1208f   10.7526f
  cstot     13.2634f   13.4761f
  cbtot     11.5480f   12.3472f
  cgs        7.2314f    7.3253f
  cgd        2.3750f    3.2680f


 av0=   5.9311
 av0db=  15.4628
 f3db= 568.4082x
```

−10% error on V_B !!

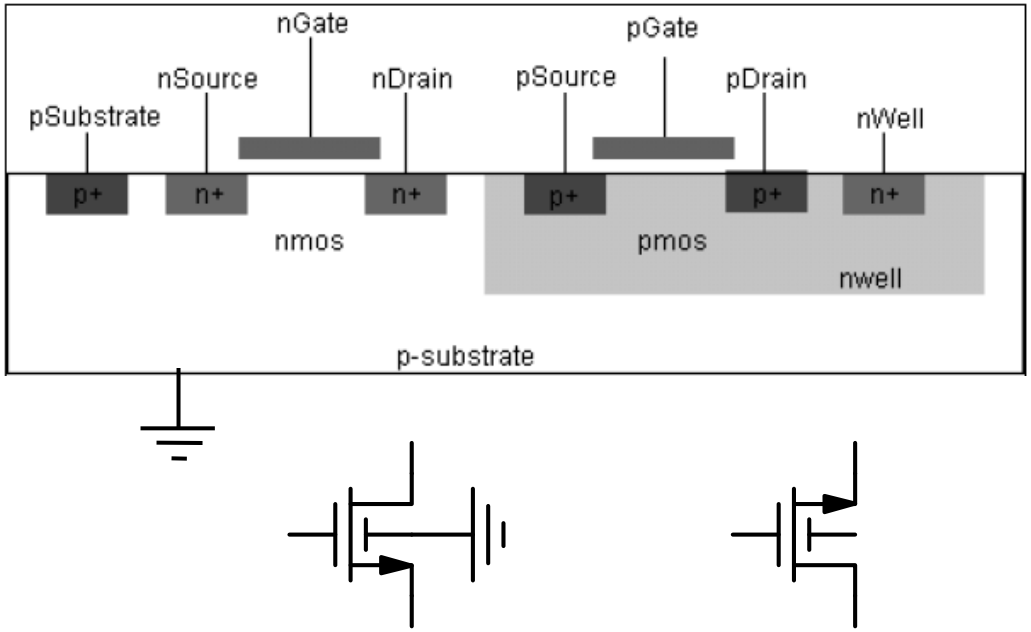
CS with current source load - Signal swing



Bulk Terminal and Backgate Effect

- Bulk Connection
- Bulk Connection Scenarios
- Well Capacitance (PMOS)
- Backgate Effect
- Modified small signal model

Bulk Connection



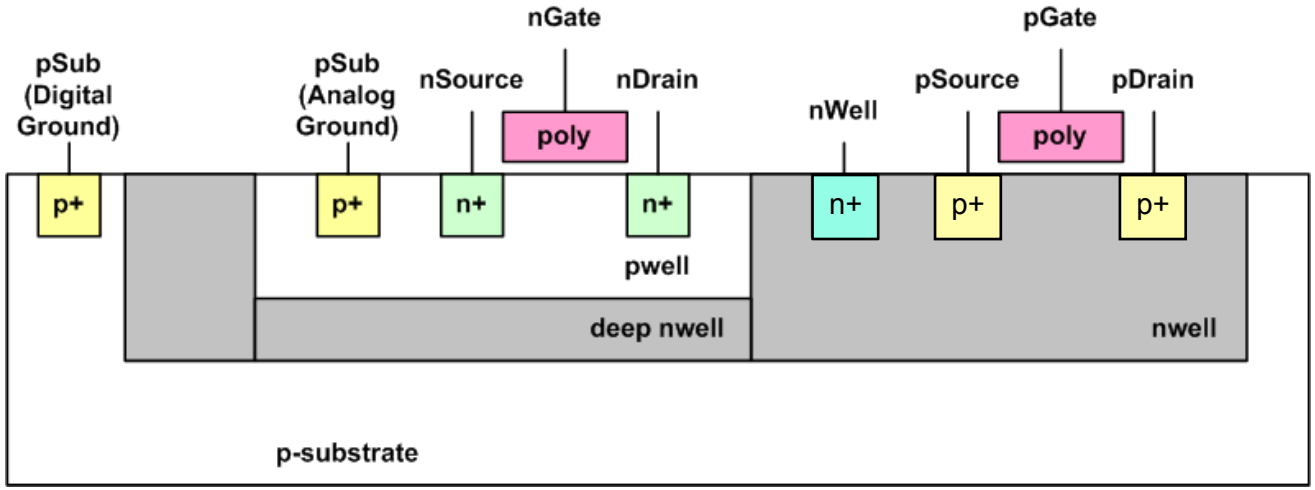
*Be aware:

- Ask the technology folks
- Know what it means!

In our technology (N-well), only the PMOS device has an isolated bulk connection

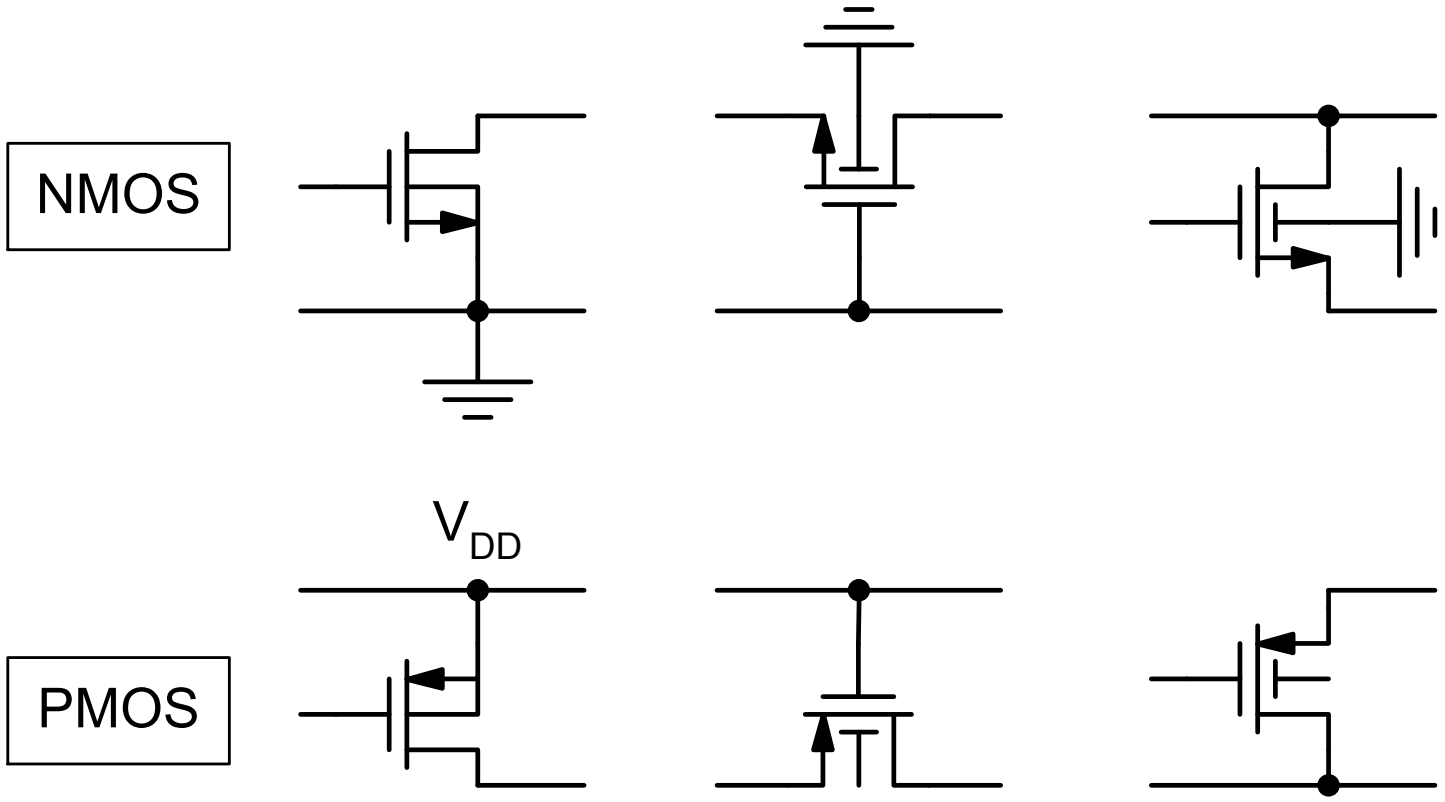
Newer technologies* (e.g. 0.13mm CMOS) also tend to have NMOS devices with isolated bulk ("tripple-well" process)

Aside: Modern Triple-Well Process



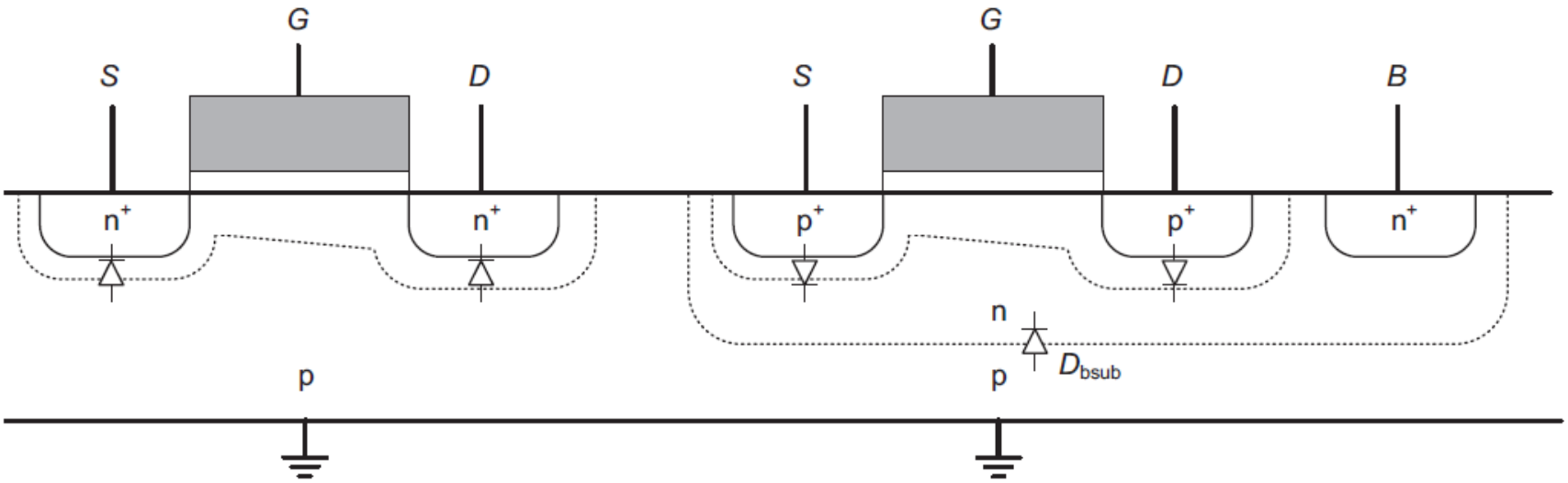
Courtesy
Shoichi Masui

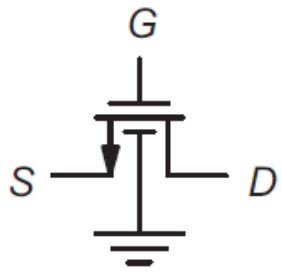
Bulk Connection Scenarios

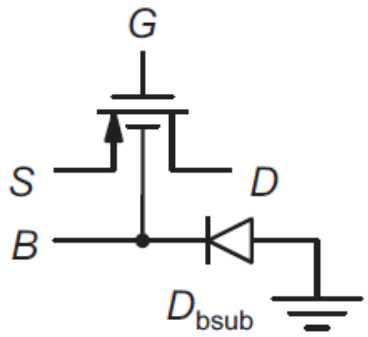


Can connect bulk to source or V_{DD}

Well Capacitance (PMOS)



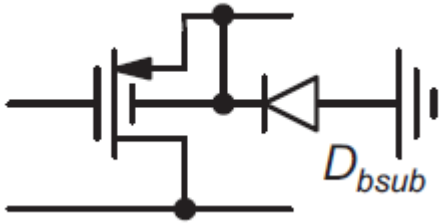


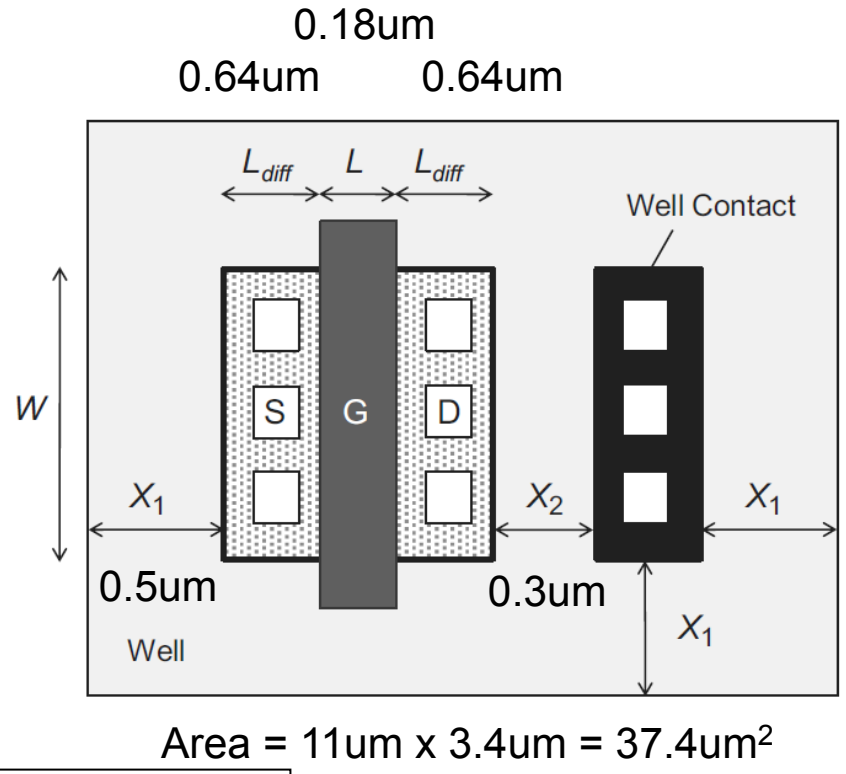


NMOS PMOS

Example

10/0.18

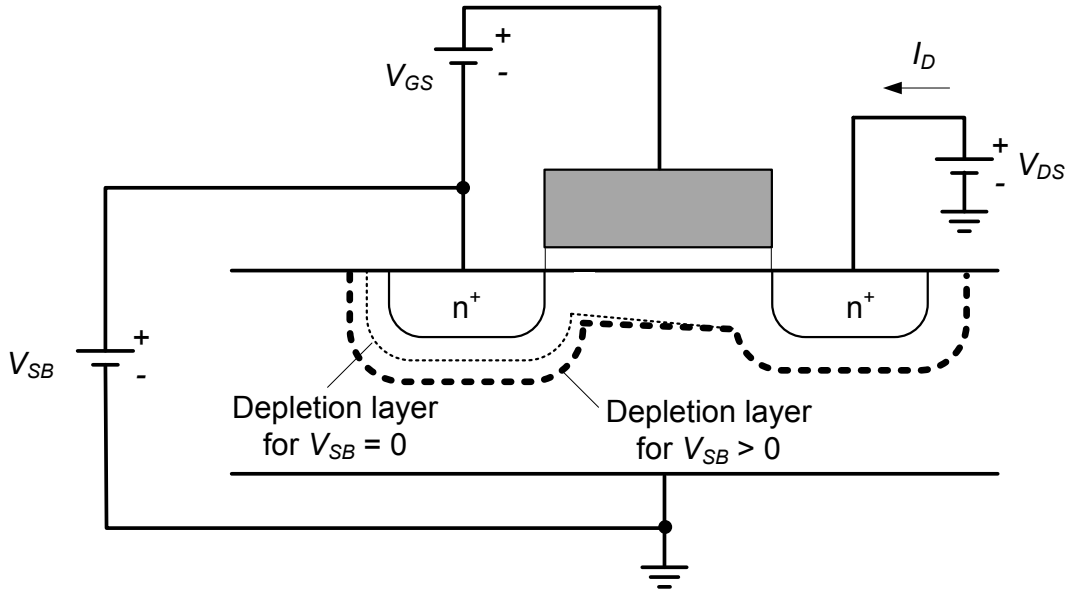




Area = 11um x 3.4um = 37.4um^2

```
* HSpice Netlist
.model dwell d cj0=2e-4 is=1e-5 m=0.5

*    d   g   s   b
mp1  0  in  out  out   pmos      L=0.18um   W=10um
*    a   k                      area
d1   0  out           dwell      37.4p
```

Backgate Effect (1)



- With positive V_{SB}, depletion region around source grows
- Increasing amount of negative fixed charge in depletion region tends to "repel" electrons coming from source
  - Need larger V_{GS} to compensate for this effect (i.e. Vt increases)

Backgate Effect (2)

- This effect is usually factored in as an effective increase in V_t
- Detailed analysis shows

$$V_t = V_{t0} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right)$$

- A change in V_t also means a change in drain current
  - Define small-signal backgate transconductance

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = -\frac{\partial I_D}{\partial V_{SB}}$$

$$\frac{g_{mb}}{g_m} = -\frac{\partial V_t}{\partial V_{SB}}\underbrace{\frac{\partial I_D}{\partial V_t}\frac{\partial V_{GS}}{\partial I_D}}_{-1} = \frac{\partial V_t}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{V_{SB} + 2\phi_f}}$$

MOS "Level 1" Equations (Saturation)

$$I_{DS} = \frac{KP}{2} \cdot \frac{W}{L_{eff}} \cdot \left(V_{GS} - V_t\right)^2 \cdot \left(1 + \lambda V_{DS}\right)$$

$$V_t = V_{TO} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right)$$

$$KP \equiv \mu C_{OX}^{'}$$

$$GAMMA \equiv \gamma = \frac{\sqrt{2\varepsilon_S q N_{bulk}}}{C_{OX}^{'}}$$

$$2\phi_f = \frac{2kT}{q} \ln \frac{N_{bulk}}{n_i}$$

$$C_{OX}^{'} = \frac{\varepsilon_{OX}}{t_{OX}}$$

$$L_{eff} = L_{mask} - 2X_{J-lateral}$$

SPICE Parameter Names:

VTO

TOX

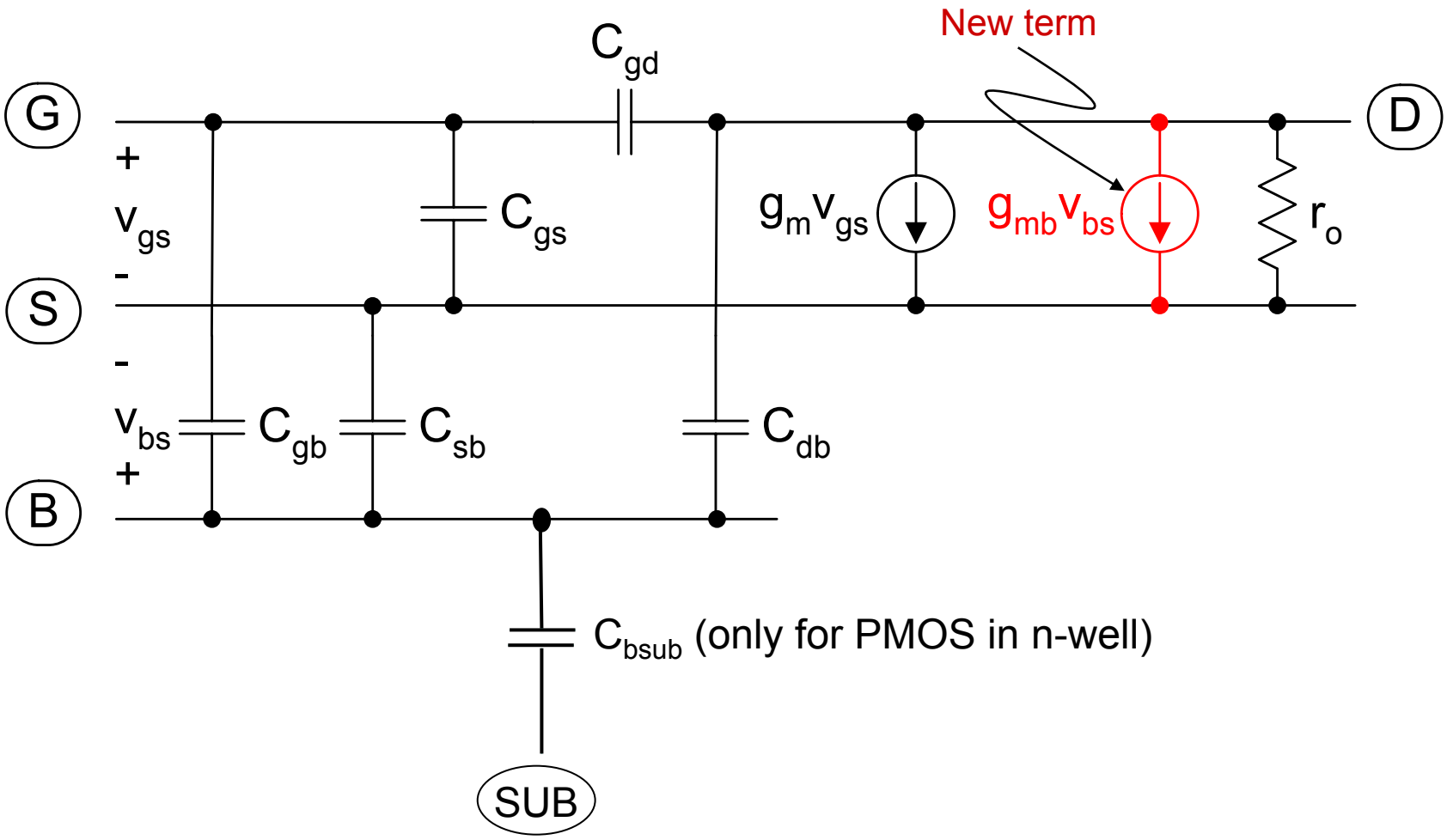
KP

LAMBDA (λ)

GAMMA (Υ)

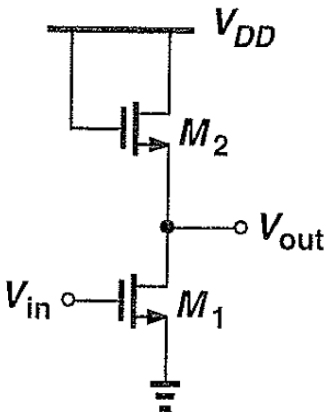
PHI ($2\Phi_f$)

Modified Small Signal Model



CS with Diode-Connected Load

Source: Razavi



$$A_V = -g_{m1}\left(r_{o1} \parallel \frac{1}{g_{m2}+g_{m2b}} \parallel r_{o2}\right) \equiv -\frac{g_{m1}}{g_{m2}+g_{m2b}} = -\frac{g_{m1}}{g_{m2}} \cdot \frac{1}{1+\eta}$$

$$R_{in} = \infty$$

$$\eta = \frac{g_{m2b}}{g_{m2}}$$

$$R_{out} = r_{o1} \parallel \frac{1}{g'_{m2}} \parallel r_{o2} \cong \frac{1}{g'_{m2}} \cong \frac{1}{g_{m2}} \quad with\ g'_{m2} = g_{m2} + g_{m2b}$$

Figure 3.9 CS stage with diode-connected load.

$$A_V \cong -\frac{g_{m1}}{g_{m2}} \cdot \frac{1}{1+\eta} = -\frac{\sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)_1 I_D}}{\sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)_2 I_D}} \cdot \frac{1}{1+\eta} = -\frac{\sqrt{\left(\frac{W}{L}\right)_1}}{\sqrt{\left(\frac{W}{L}\right)_2}} \cdot \frac{1}{1+\eta}$$

The gain is “ratiometric”

As long as M_1 stay in saturation (M_2 is diode connected so as long as is ON, it is always in saturation) the gain is not affected by “fluctuations” of the bias current and bias voltages

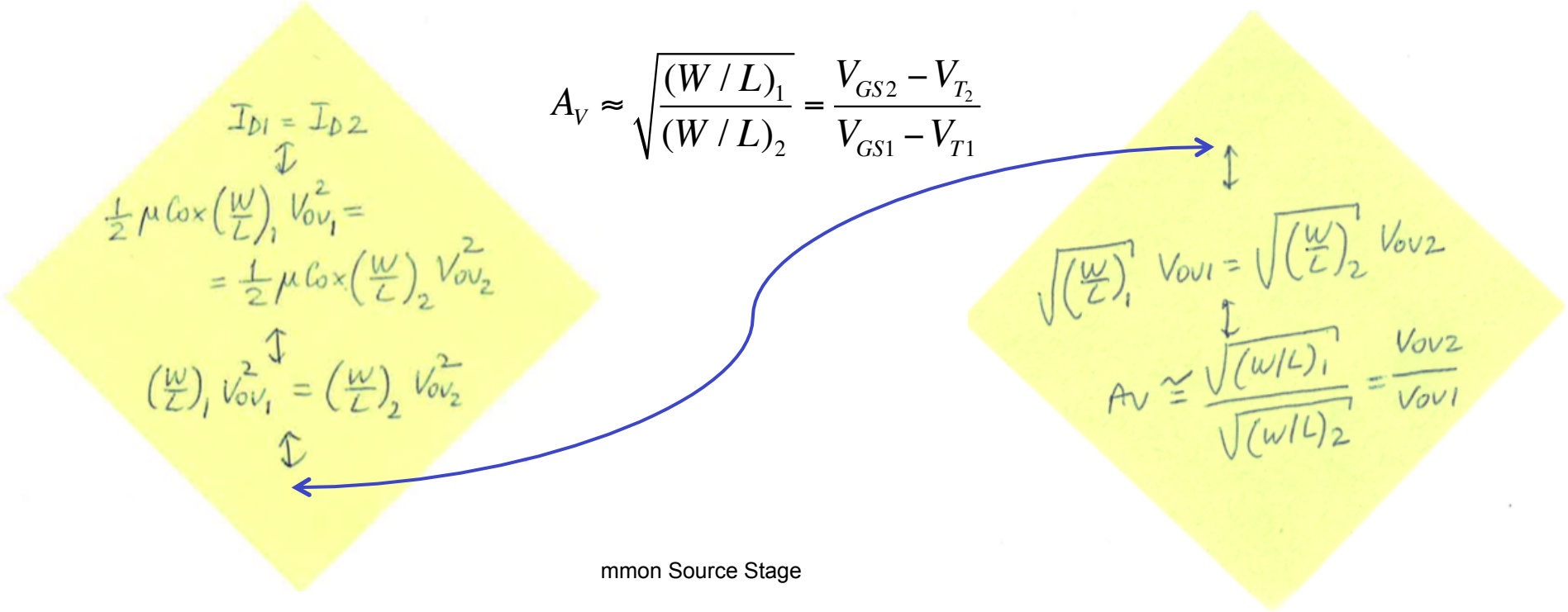
↓

The input-output characteristic is relatively linear

Design Considerations (1)

- High gain requires a “strong” input device (M_1) and a “weak” load device (M_2)
- Issues:
  - For high gain we need: “very” wide M_1 (large input capacitance) or “very” long M_2 (large load capacitance)
  - For high gain, the allowable voltage swing is significantly limited

$$A_V \approx \sqrt{\frac{(W/L)_1}{(W/L)_2}} = \frac{V_{GS2} - V_{T_2}}{V_{GS1} - V_{T1}}$$



Design Considerations (2)

- For square law devices, the output signal swing can be predicted analytically
  - $V_{out}(\max) = V_{DD} - V_{T2}$
  - $V_{out}(\min) = V_{DD} - V_{T2} - \dfrac{V_{DD} - V_{T1}}{\sqrt{1 + \beta_2 / \beta_1}}$

NOTE:
This clearly shows why for high gain (β_2 small, β_1 large) the "negative" signal swing gets "significantly" limited

Equate the equation of I_D for M_1 (edge triode region) and the equation of I_D for M_2 (saturation) and solve for V_{out}

- The stage is relatively linear even for large signals

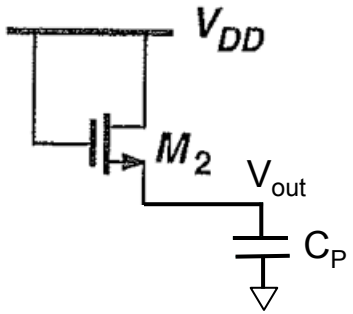
$$\frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)_1 (V_{in} - V_{T1})^2 = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)_2 (V_{DD} - V_{out} - V_{T2})^2$$

$$\sqrt{\left(\frac{W}{L}\right)_1}(V_{in} - V_{T1}) = \sqrt{\left(\frac{W}{L}\right)_2}(V_{DD} - V_{out} - V_{T2})$$

NOTE:
The eq. of V_{out} vs. V_{in} is a straight line

CS with diode connected load: I/O DC sweep (1)

- For M_1 in cut off ($V_{in} < V_{T1}$), the output voltage "settle" to $V_{out} = V_{DD} - V_{T1}$



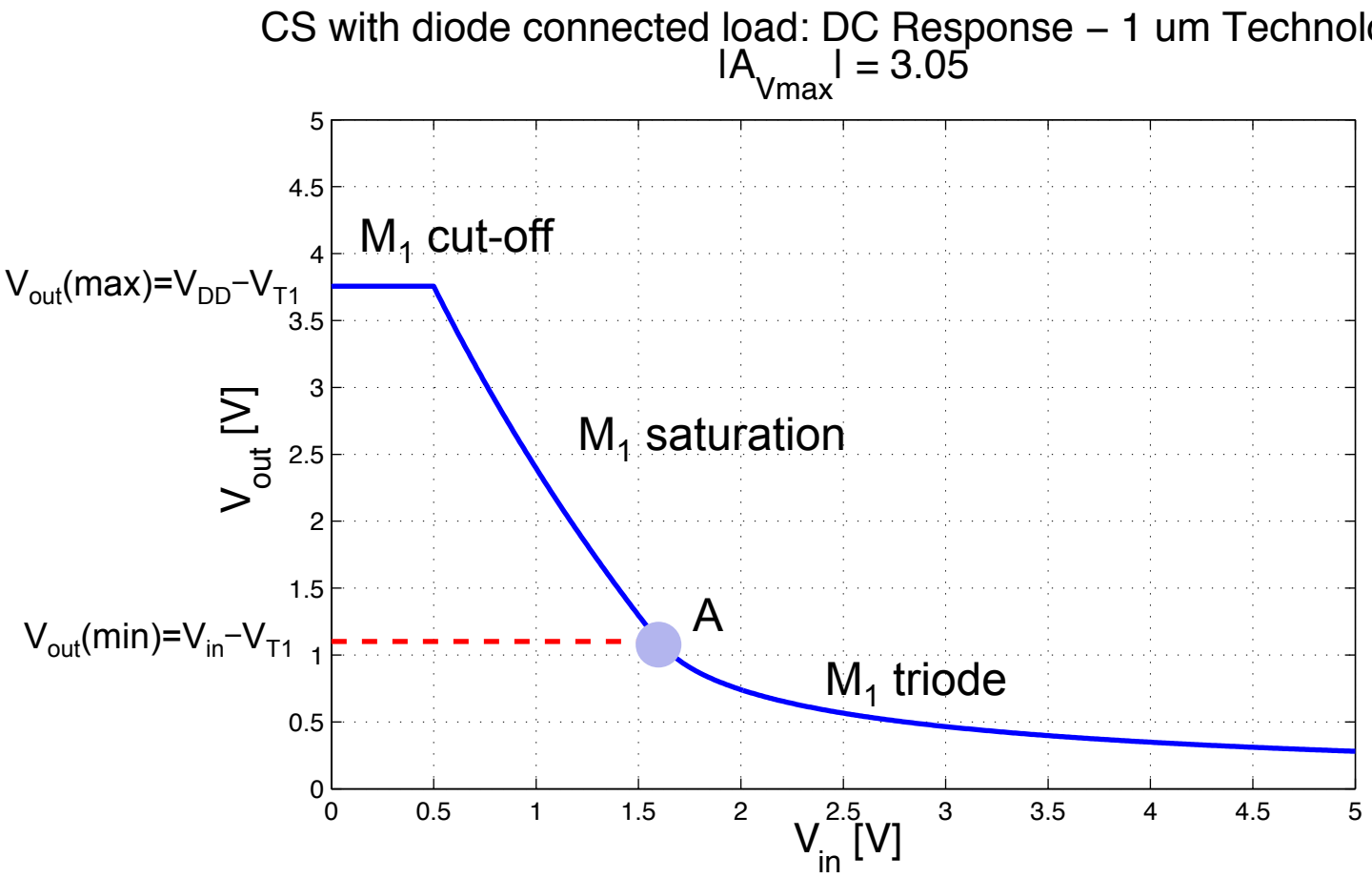
Digital folks like to say:
NMOS pass a "degraded" VDD

- For $V_{in} > V_{T1}$ the device M_1 enters saturation and V_{out} follows an approximately straight line

$$V_{out} \approx V_{in} \cdot \sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

- As V_{in} exceeds $V_{out}+V_{T1}$ (beyond point A), M_1 enters triode region, and the characteristics becomes non linear

CS with diode connected load: I/O DC sweep (2)



W_1/L_1 = 200µm/1µm; W_2/L_2 = 20µm/1µm; $A_V \cong \sqrt{10} \cong 3.16$

Hspice Deck

```
* CS with diode connected load
* filename: csdiode.sp
* C. Talarico, Fall 2014

*** device model
.model simple_nmos nmos kp=50u vto=0.5 lambda=0.1 cox=2.3e-3 capop=2
+ cgdo=0.5n cgso=0.5n cj=0.1m cjsw=0.5n pb=0.95 mj=0.5 mjsw=0.95
+ acm=3 cjgate=0 hdif=1.5u gamma=0.6 PHI=0.8


*** useful options
.option post brief nomod accurate

*** long_channel device
vdd vdd 0 5
* load device
mn2 vdd vdd vo 0   simple_nmos   w=20u  l=1u
* amplifing device
mn1 vo  vi  0   0  simple_nmos   w=200u l=1u
vi  vi  0   dc  1
+           ac  1
*** large signal analysis (sweep Vi)
.OP
.dc vi 0 5 0.01

.end
```

Matlab Script

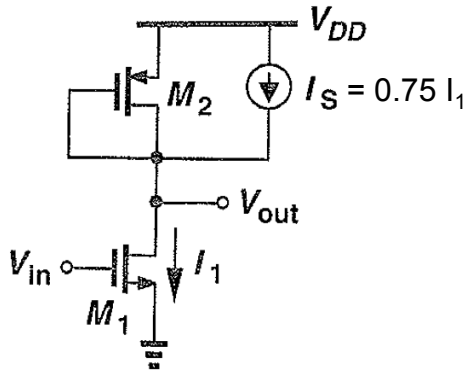
```
%
% csdiode_plot.m
%
clear all; close all;
format short eng
addpath('/usr/local/MATLAB/personal/HspiceToolbox');
x = loadsig('./csdiode.sw0');
lssig(x)

figure(1);
vo = evalsig(x,'v_vo');
vi = evalsig(x,'v_vi');

vth1 = 0.5;
plot(vi, vo,'linewidth',2, 'color', 'b', 'linestyle', '-');
grid on;
ylabel(' V_{out} [V]', 'Fontsize', 16);
xlabel(' V_{in} [V]', 'Fontsize', 16);
xmin = 0;
xmax = 5;
xlim([xmin xmax]);
ymax = 5;
ymin = 0;
ylim([ ymin ymax]);
% compute when M1 enters triode region
for i=1:length(vi)
  if vo(i)+vth1-vi(i) < 0
     index = i;
     break
  end
end
% horizontal line at Vi for which M1 enter triode
pointA = vo(index-1); % take index-1 for margin
line([min(vi) vi(index)], [pointA pointA], 'linestyle', '--', ...
    'linewidth', 2, 'color', 'r');
% compute gain
h = 0.01;
Y = diff(vo)/h;
AV = min(Y)  % gain is negative
str1 = sprintf('CS with diode connected load: DC Response - 1 um Technology');
str2 = sprintf('|A_{Vmax}| = %0.2f', abs(AV));
str = {str1, str2};
```

Diode connected load vs. resistive load

- Advantages
  - "Ratiometric"
    - Gain depends on ratio of similar parameters
    - Effect of process and temperature variations is reduced
    - First order cancellation of nonlinearities
- Disadvantage
  - Reduced swing

Improving the CS with Diode-Connected Load

Source: Razavi



Add a current source across the diode connected load

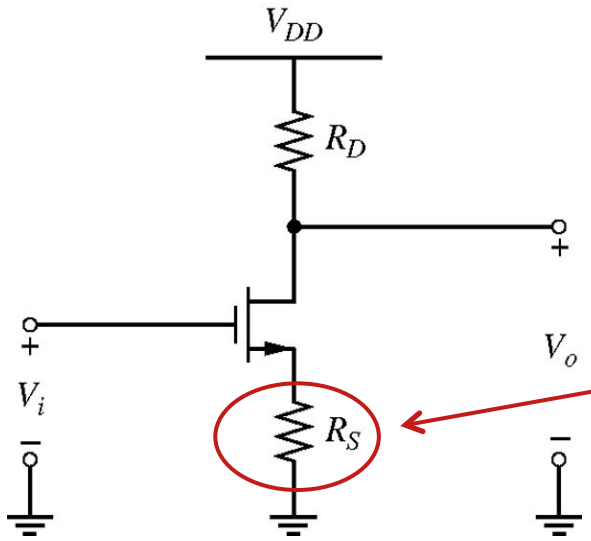
- Since $I_{D2} = I_1/4$ we have: $A_V \cong -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{4\mu_n (W/L)_1}{\mu_p (W/L)_2}} = -4\,\frac{|V_{GS2} - V_{T2}|}{V_{GS1} - V_{T1}}$

- For a given overdrive voltage this circuit achieves a gain 4x that of the original stage. Alternatively, for a given gain, we need b_1/b_2 4x smaller, so this helps in terms of swing. (For a gain of 10, the overdrive of M_2 needs to be only 2.5 x that of M_1 instead of 10 x like in the original circuit).

CS with Source Degeneration

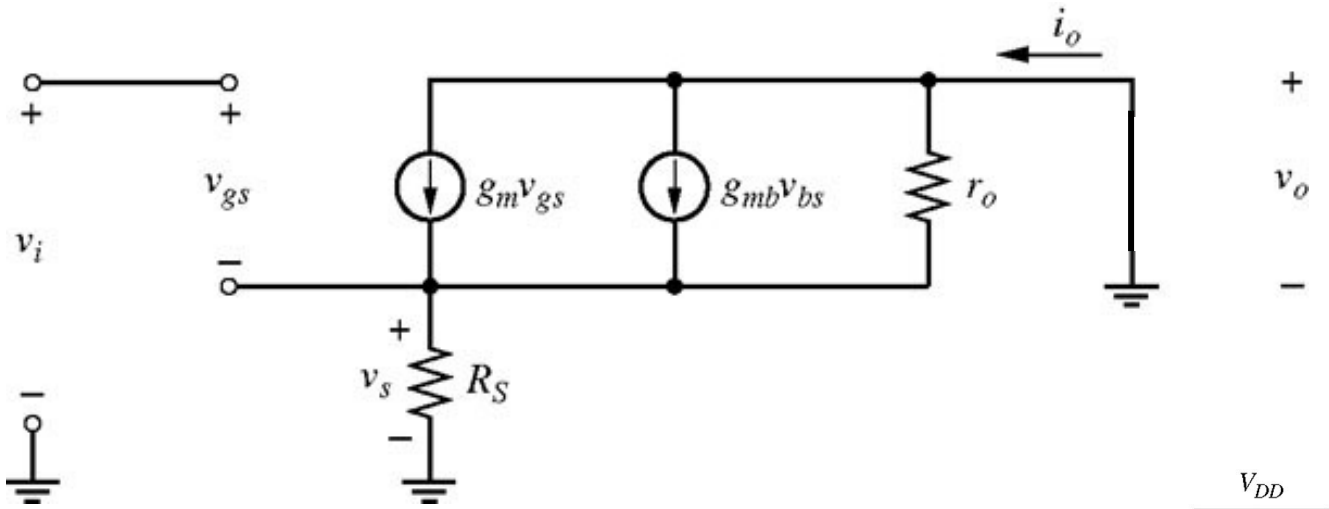
- Examining the effect of source degeneration is important because it is widely used to increase the output resistance of MOS current sources

- However, source degeneration in MOS transistors amplifiers in not widely used (as emitter degeneration in bipolar transistors)
  - The g_m of MOS transistors is much lower than that of bipolar transistors, so a further reduction in the effective transconductance G_m is usually not desirable
  - Although degeneration increases the input resistance in the bipolar case, in the MOS case Ri $\cong \infty$ even without degeneration



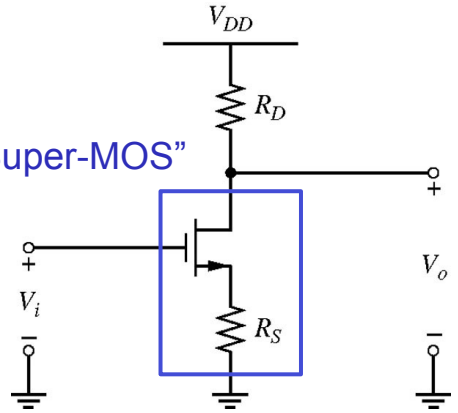
This is a local series FB more later …

Effective transconductance of CS with degeneration



$$G_m = \frac{i_o}{v_i} = \frac{g_m}{1 + g'_m R_S + \frac{R_S}{r_o}} \approx \frac{g_m}{1 + g'_m R_S}$$

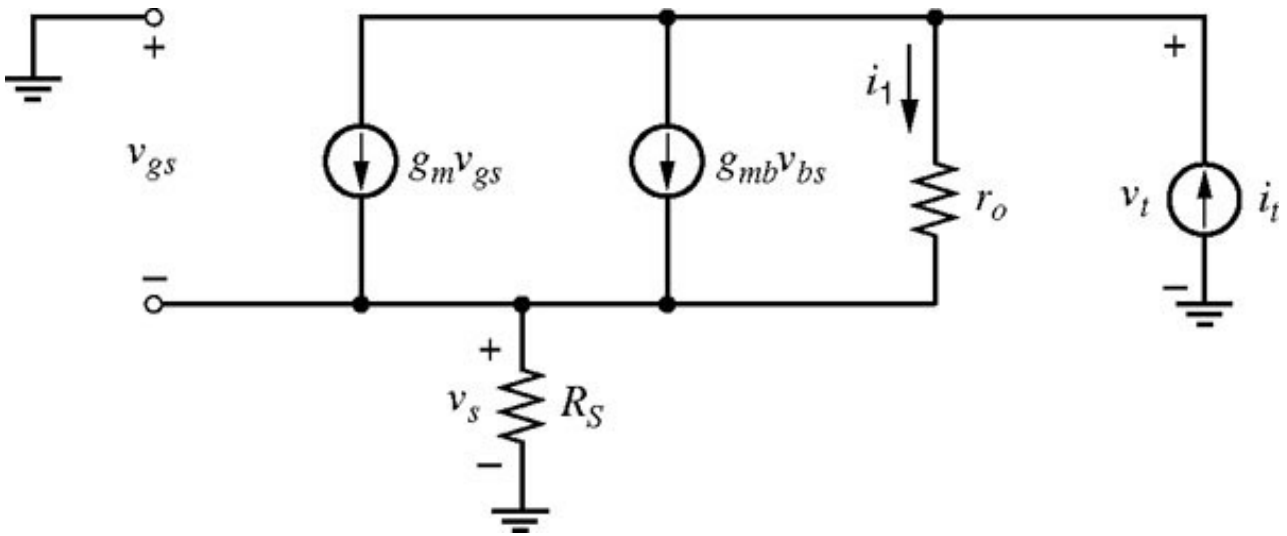
$r_o >> R_s$



"Super-MOS"

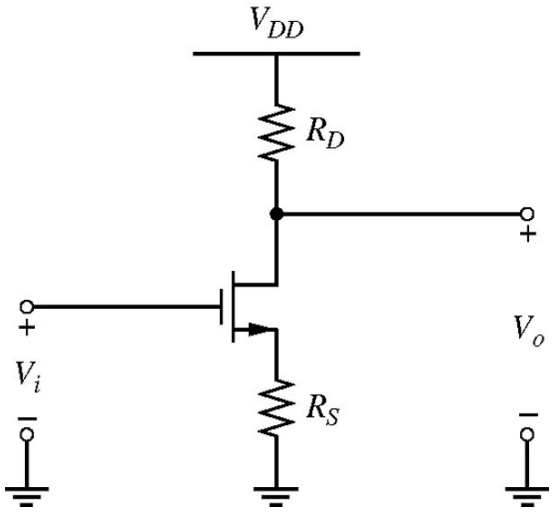
Not necessarily true!!
Think of the case where R_S is obtained via another transistor.

Output Resistance of CS with degeneration



$$R_o = \frac{v_t}{i_t} = R_S + r_o\left[1 + g'_m R_S\right] \cong r_o\left[1 + g'_m R_S\right]$$

Gain of CS with degeneration (1)

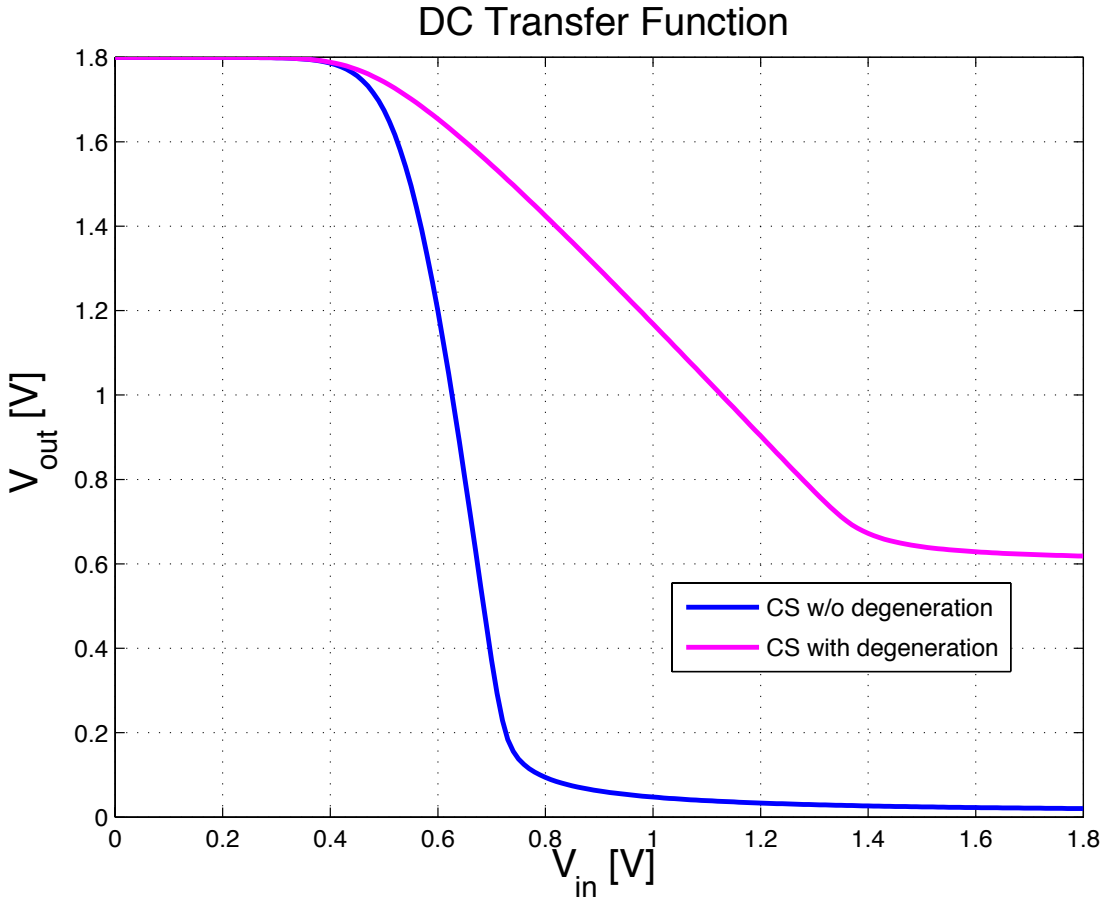


$$A_V = -G_m(R_o \parallel R_D) \cong -G_m R_D \cong -\frac{g_m R_D}{1 + g'_m R_S}$$

- For $R_S >> 1/g'_m$ (and $g'_m \cong g_m$) $\Rightarrow$ $A_V \cong -\frac{R_D}{R_S}$

- The degeneration "soften" (i.e., it linearizes) the drain current I_D dependency on V_{in}. A fraction of V_{in} appears across R_S rather than as gate-source overdrive, thus leading to a smoother variation of I_D
- The linearization is obtained at the cost of lower gain and higher noise (more on noise later …)

Gain of CS with degeneration (2)



V_{DD}=1.8V; R_D=2KΩ; R_S=1KΩ; W/L=21.34μm/0.18μm

BW of CS with Degeneration

f_{-3db}(CS with degeneration) ≈ f_{-3dB}(CS w/o degeneration) × (1 + g'_m × R_S)

Why? we need to know more about FB.
To be continued …

Summary of CS with degeneration

- The source degeneration introduces series negative FB
- Compared to the basic CS stage
  - Gain is reduced by a factor ≈ $1+g_mR_S$
  - R_S controls the magnitude of the signal v_{gs}. It ensures that v_{gs} does not become too large and causes unacceptably high non linear distortion.
  - Input Resistance is increased by a factor ≈ $1+g_mR_S$ (but since $R_{in}\approx\infty$ this is not a big deal)
  - Output Resistance is increased by a factor ≈ $1+g_mR_S$
  - BW is increased by a factor ≈ $1+g_mR_S$