Extrinsic Capacitance

Claudio Talarico
Gonzaga University
Fall 2014

Source:
most slides provided by B. Murmann
Extrinsic Capacitance

- Overlap capacitance (Cov)
  - Gate to source and gate to drain

- Junction capacitance
  - Source to bulk (Csb) and drain to bulk (Cdb)
Overlap Capacitance

- Two components
  - Direct overlap \( \sim C_{ox}WL_{overlap} \)
  - Additional component due to fringing field
    - Non-negligible in modern technology (gate thickness is large compared to other feature sizes)

- Simple model equation \( C_{ov} = C_{ov}' \cdot W \)

- Stanford’s EE114 technology:
  - \( C_{ov}' = 0.5 \text{fF/\mu m} \) for both NMOS and PMOS
  - Spice model parameters: CGSO=0.5n, CGDO=0.5n

\[ C_{ov-GS} = CGSO \cdot W \]
\[ C_{ov-GD} = CGDO \cdot W \]
Junction Capacitance (1)

For long channel transistors the side of the perimeter abutted to the gate is shielded by the electrons in the channel

\[ AS = W \cdot L_{\text{diff}} \]
\[ PS = W + 2L_{\text{diff}} \]
\[ AD = W \cdot L_{\text{diff}} \]
\[ PD = W + 2L_{\text{diff}} \]

Extrinsic Capacitance

\[ C_{j\text{db}} = \frac{AD \cdot CJ}{\left(1 + \frac{VDB}{PB}\right)^{MJ}} + \frac{PD \cdot CJSW}{\left(1 + \frac{VDB}{PBSW}\right)^{MJSW}} \]

\[ C_{j\text{sb}} = \frac{AS \cdot CJ}{\left(1 + \frac{VSB}{PB}\right)^{MJ}} + \frac{PS \cdot CJSW}{\left(1 + \frac{VSB}{PBSW}\right)^{MJSW}} \]

\[ C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{\phi_B}}} \]
\[ C_{j0} = \frac{\varepsilon_s q N_A N_D}{\sqrt{2 N_A + N_D} \phi_B} \]
Geometry parameters for calculating junction cap.

- \( PS = 2 \times L_{\text{diff}} \text{(source)} + W \)
- \( PD = 2 \times L_{\text{diff}} \text{(drain)} + W \)
- \( AS = W \times L_{\text{diff}} \text{(source)} \)
- \( AD = W \times L_{\text{diff}} \text{(drain)} \)
Junction Capacitance (2)

\[ C_{jdb} = \frac{AD \cdot CJ}{1 + \frac{V_{DB}}{PB}} \left(1 + \frac{V_{DB}}{PB}\right)^{MJ} + \frac{PD \cdot CJSW}{1 + \frac{V_{DB}}{PB}} \left(1 + \frac{V_{DB}}{PB}\right)^{MJSW} \]

\[ C_{jsb} = \frac{AS \cdot CJ}{1 + \frac{V_{SB}}{PB}} \left(1 + \frac{V_{SB}}{PB}\right)^{MJ} + \frac{PS \cdot CJSW}{1 + \frac{V_{SB}}{PB}} \left(1 + \frac{V_{SB}}{PB}\right)^{MJSW} \]

<table>
<thead>
<tr>
<th>EE114 Technology</th>
<th>CJ</th>
<th>CJSW</th>
<th>MJ</th>
<th>MJSW</th>
<th>PB</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>0.1 fF/µm²</td>
<td>0.5 fF/µm</td>
<td>0.5</td>
<td>0.33</td>
<td>0.95V</td>
</tr>
<tr>
<td>PMOS</td>
<td>0.3 fF/µm²</td>
<td>0.35 fF/µm</td>
<td>0.5</td>
<td>0.33</td>
<td>0.95V</td>
</tr>
</tbody>
</table>

Extrinsic Capacitance
### MOS transistor’s caps: Summary

<table>
<thead>
<tr>
<th></th>
<th>Subthreshold</th>
<th>Triode</th>
<th>Saturation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{gs}$</td>
<td>$C_{ov}$</td>
<td>$\frac{1}{2}WL C_{ox} + C_{ov}$</td>
<td>$\frac{2}{3}WL C_{ox} + C_{ov}$</td>
</tr>
<tr>
<td>$C_{gd}$</td>
<td>$C_{ov}$</td>
<td>$\frac{1}{2}WL C_{ox} + C_{ov}$</td>
<td>$C_{ov}$</td>
</tr>
<tr>
<td>$C_{gb}$</td>
<td>$\left(\frac{1}{C_{CB}} + \frac{1}{WLC_{ox}}\right)^{-1}$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$C_{sb}$</td>
<td>$C_{jsb}$</td>
<td>$C_{jsb} + \frac{1}{2}C_{CB}$</td>
<td>$C_{jsb} + \frac{2}{3}C_{CB}$</td>
</tr>
<tr>
<td>$C_{db}$</td>
<td>$C_{jdb}$</td>
<td>$C_{jdb} + \frac{1}{2}C_{CB}$</td>
<td>$C_{jdb}$</td>
</tr>
</tbody>
</table>

$$C_{CB} = \frac{\varepsilon_{si}}{X_d} \cdot WL$$

Xd is the width of the depletion region at the silicon interface.

Extrinsic Capacitance
MOS Capacitance Simulation

- Note gradual transition in capacitance values

![Graph showing capacitance values vs. gate voltage](image)
Small Signal Model with Capacitances

\[ G \quad + \quad V_{gs} \quad - \quad S \quad B \]

\[ C_{gd} \quad C_{gs} \quad g_m V_{gs} \quad r_o \]

\[ C_{gb} \approx 0 \quad C_{sb} \quad C_{db} \]
Transit Frequency with Extrinsic capacitances

\[
\frac{I_{\text{out}}}{I_{\text{in}}} \bigg|_{\omega=\omega_T} = 1
\]

\[
\omega_T = \frac{g_m}{C_{gs} + C_{gd}}
\]
## Parameter Summary (1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Purpose</th>
<th>EE 114 Technology</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>NMOS</td>
<td>PMOS</td>
<td></td>
</tr>
<tr>
<td>KP</td>
<td>$\mu C_{ox}$</td>
<td>50 $\mu$A/V$^2$</td>
<td>25 $\mu$A/V$^2$</td>
<td></td>
</tr>
<tr>
<td>COX</td>
<td>$\varepsilon_{ox}/t_{ox}$</td>
<td>2.3 fF/µm$^2$</td>
<td>2.3 fF/µm$^2$</td>
<td></td>
</tr>
<tr>
<td>VTO</td>
<td>Threshold Voltage</td>
<td>0.5 V</td>
<td>−0.5 V</td>
<td></td>
</tr>
<tr>
<td>LAMBDA</td>
<td>Channel length modulation</td>
<td>0.1 V$^{-1}$µm/L</td>
<td>0.1 V$^{-1}$µm/L</td>
<td></td>
</tr>
<tr>
<td>CGDO, CGSO</td>
<td>Gate-drain/source overlap capacitance per length</td>
<td>0.5 fF/µm</td>
<td>0.5 fF/µm</td>
<td></td>
</tr>
<tr>
<td>CJ</td>
<td>Zero bias area capacitance</td>
<td>0.1 fF/µm$^2$</td>
<td>0.3 fF/µm$^2$</td>
<td></td>
</tr>
<tr>
<td>CJSW</td>
<td>Zero bias sidewall capacitance</td>
<td>0.5 fF/µm</td>
<td>0.35 fF/µm</td>
<td></td>
</tr>
</tbody>
</table>
## Parameter Summary (2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Purpose</th>
<th>EE 114 Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>NMOS</td>
</tr>
<tr>
<td>PB</td>
<td>Junction Potential</td>
<td>0.95 V</td>
</tr>
<tr>
<td>MJ</td>
<td>Area Junction Grading Coefficient</td>
<td>0.5</td>
</tr>
<tr>
<td>MJSW</td>
<td>Area Junction Grading Coefficient</td>
<td>0.33</td>
</tr>
<tr>
<td>HDIF</td>
<td>Half-length of S/D diffusion (=\frac{L_{\text{diff}}}{2})</td>
<td>1.5 µm</td>
</tr>
<tr>
<td>GAMMA</td>
<td>Bulk Threshold Parameter</td>
<td>0.6 V(^{1/2})</td>
</tr>
<tr>
<td>PHI</td>
<td>Surface Potential (2\Phi_t)</td>
<td>0.8 V</td>
</tr>
</tbody>
</table>

- **Extrinsic Capacitance**

---

Needed Later
Common Source Amplifier (Revisited)

\[ V_B = 2.5V \]
\[ V_I = 1.394V \]
\[ I_B = 500m\text{A} \]
\[ W/L = 20\mu\text{m}/1\mu\text{m} \]
\[ R = 5k\Omega \]
\[ R_i = 50k\Omega \]
Small-Signal Model

\[ C_{gd} = W \cdot C'_{ov} = 20 \cdot 0.5 \text{fF} = 10 \text{fF} \]

\[ C_{gs} = \frac{2}{3} WLC_{ox} + C_{ov} = \frac{2}{3} \cdot 20 \cdot 1 \cdot 2.3 \text{fF} + 10 \text{fF} = 40.67 \text{fF} \]

\[ C_{db} = \frac{AD \cdot CJ}{1 + \frac{V_{DB}}{PB}}^{MJ} + \frac{PD \cdot CJSW}{1 + \frac{V_{DB}}{PB}}^{MJ,SW} = \frac{60 \cdot 0.1 \text{fF}}{1 + \frac{2.5}{0.95}^{0.5}} + \frac{26 \cdot 0.5 \text{fF}}{1 + \frac{2.5}{0.95}^{0.33}} = 11.6 \text{fF} \]
Extrinsic capacitance

. AC SPICE Simulation

- Extrinsic caps reduce bandwidth from 103 MHz to 32 MHz!
- There also seems to be a second pole.