Extrinsic Capacitance

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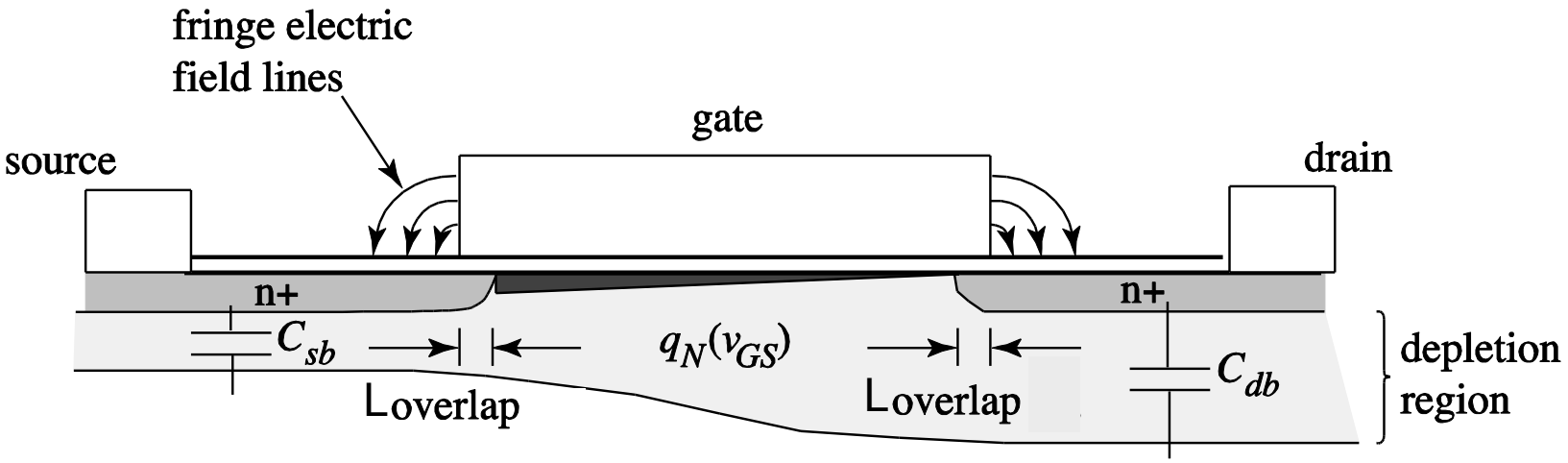
Source:
most slides provided by B. Murmann

Extrinsic Capacitance

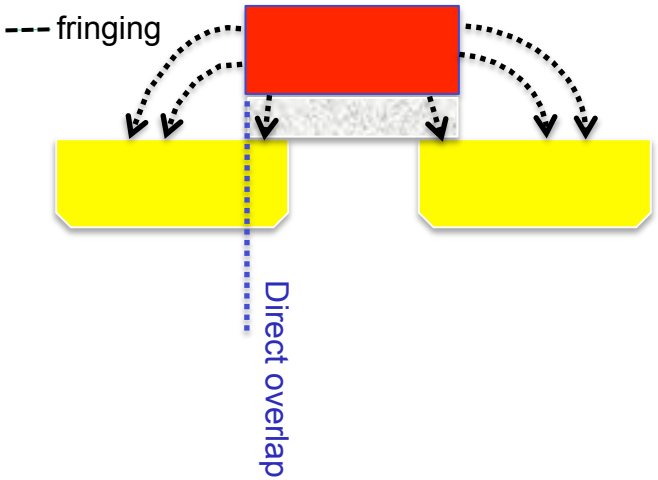


- Overlap capacitance (Cov)
  - Gate to source and gate to drain
- Junction capacitance
  - Source to bulk (Csb) and drain to bulk (Cdb)

Overlap Capacitance

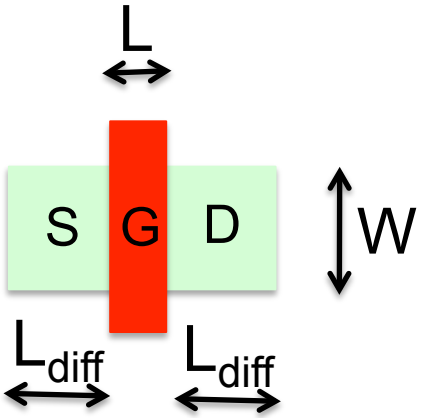
- Two components
  - Direct overlap ~ $C_{ox}WL_{overlap}$
  - Additional component due to fringing field
    - Non-negligible in modern technology (gate thickness is large compared to other feature sizes)
- Simple model equation $C_{ov} = C_{ov}' \cdot W$
- Stanford's EE114 technology:
  - C_{ov}' = 0.5fF/μm for both NMOS and PMOS
  - Spice model parameters: CGSO=0.5n, CGDO=0.5n

C_{ov}' = overlap capacitance per unit length



$$C_{ov-GS} = CGSO \cdot W$$
$$C_{ov-GD} = CGDO \cdot W$$

Junction Capacitance (1)



$$AS = W \cdot L_{diff}$$

$$PS = W + 2L_{diff}$$

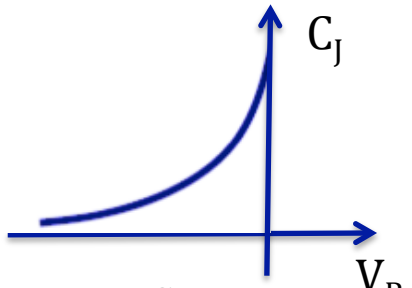
$$AD = W \cdot L_{diff}$$

$$PD = W + 2L_{diff}$$

For long channel transistors the side of the perimeter abutted to the gate is shielded by the electrons in the channel

$$Cjdb = \frac{AD \cdot CJ}{\left(1 + \frac{VDB}{PB}\right)^{MJ}} + \frac{PD \cdot CJSW}{\left(1 + \frac{VDB}{PBSW}\right)^{MJSW}}$$

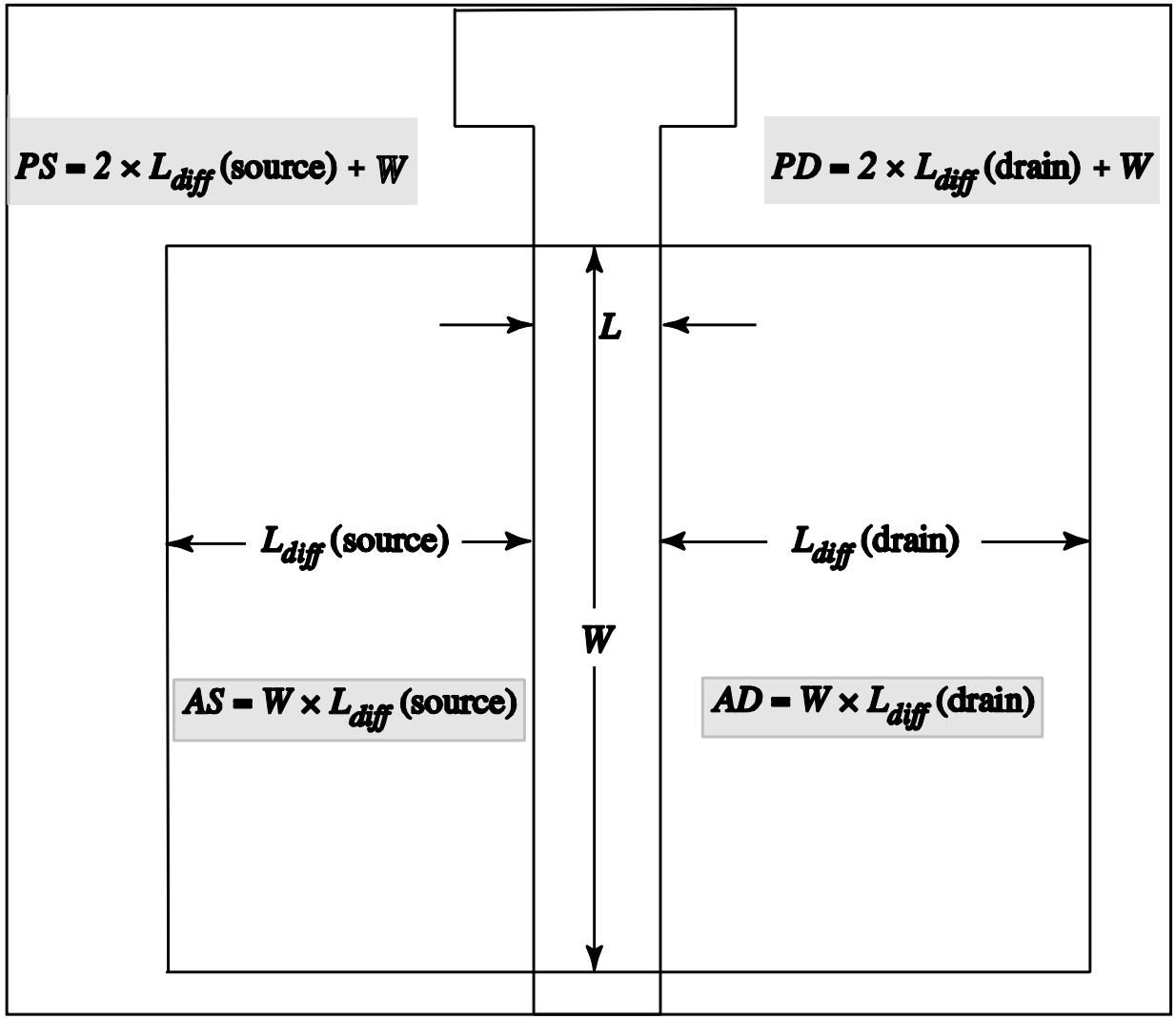
$$Cjsb = \frac{AS \cdot CJ}{\left(1 + \frac{VSB}{PB}\right)^{MJ}} + \frac{PS \cdot CJSW}{\left(1 + \frac{VSB}{PBSW}\right)^{MJSW}}$$



$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{\phi_B}}}$$

$$C_{j0} = \sqrt{\frac{\varepsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D} \frac{1}{\phi_B}}$$

Geometry parameters for calculating junction cap.



Junction Capacitance (2)

$$C_{jdb} = \frac{AD \cdot CJ}{\left(1+\frac{V_{DB}}{PB}\right)^{MJ}} + \frac{PD \cdot CJSW}{\left(1+\frac{V_{DB}}{PB}\right)^{MJSW}}$$

$$C_{jsb} = \frac{AS \cdot CJ}{\left(1+\frac{V_{SB}}{PB}\right)^{MJ}} + \frac{PS \cdot CJSW}{\left(1+\frac{V_{SB}}{PB}\right)^{MJSW}}$$

EE114 Technology	CJ	CJSW	MJ	MJSW	PB
NMOS	0.1 fF/μm^2	0.5 fF/μm	0.5	0.33	0.95V
PMOS	0.3 fF/μm^2	0.35 fF/μm	0.5	0.33	0.95V

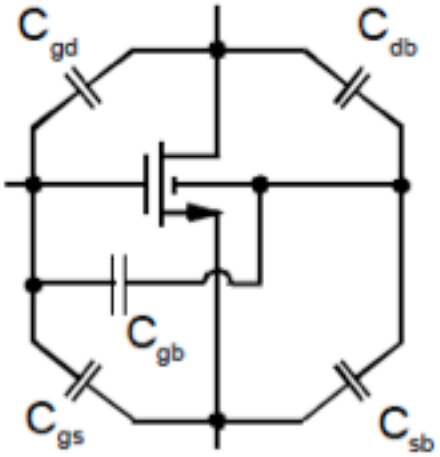
MOS transistor's caps: Summary

extrinsic cap. intrinsic cap.

	Subthreshold	Triode	Saturation
C_{gs}	C_{ov}	$\frac{1}{2}WLC_{ox}+C_{ov}$	$\frac{2}{3}WLC_{ox}+C_{ov}$
C_{gd}	C_{ov}	$\frac{1}{2}WLC_{ox}+C_{ov}$	C_{ov}
C_{gb}	$\left(\frac{1}{C_{CB}}+\frac{1}{WLC_{ox}}\right)^{-1}$	0	0
C_{sb}	C_{jsb}	$C_{jsb}+\frac{1}{2}C_{CB}$	$C_{jsb}+\frac{2}{3}C_{CB}$
C_{db}	C_{jdb}	$C_{jdb}+\frac{1}{2}C_{CB}$	C_{jdb}

$$C_{CB} = \frac{\varepsilon_{si}}{X_d} \cdot WL$$

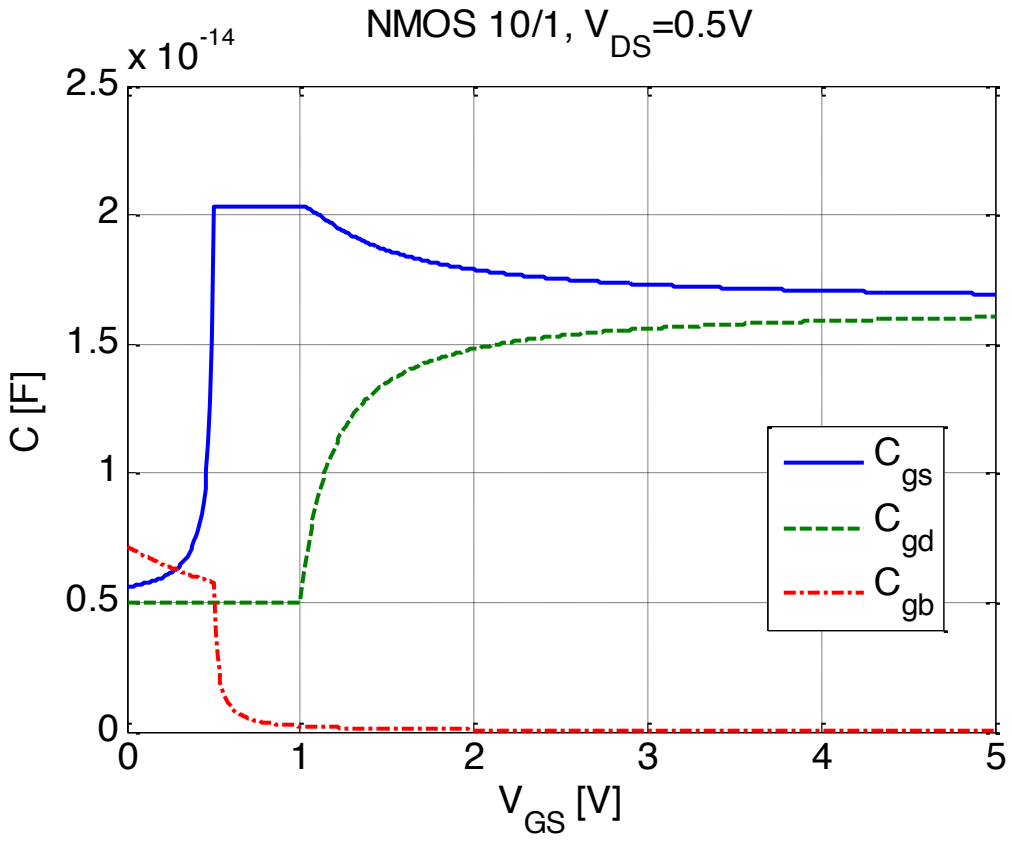
Xd is the width of the depletion region at the silicon interface



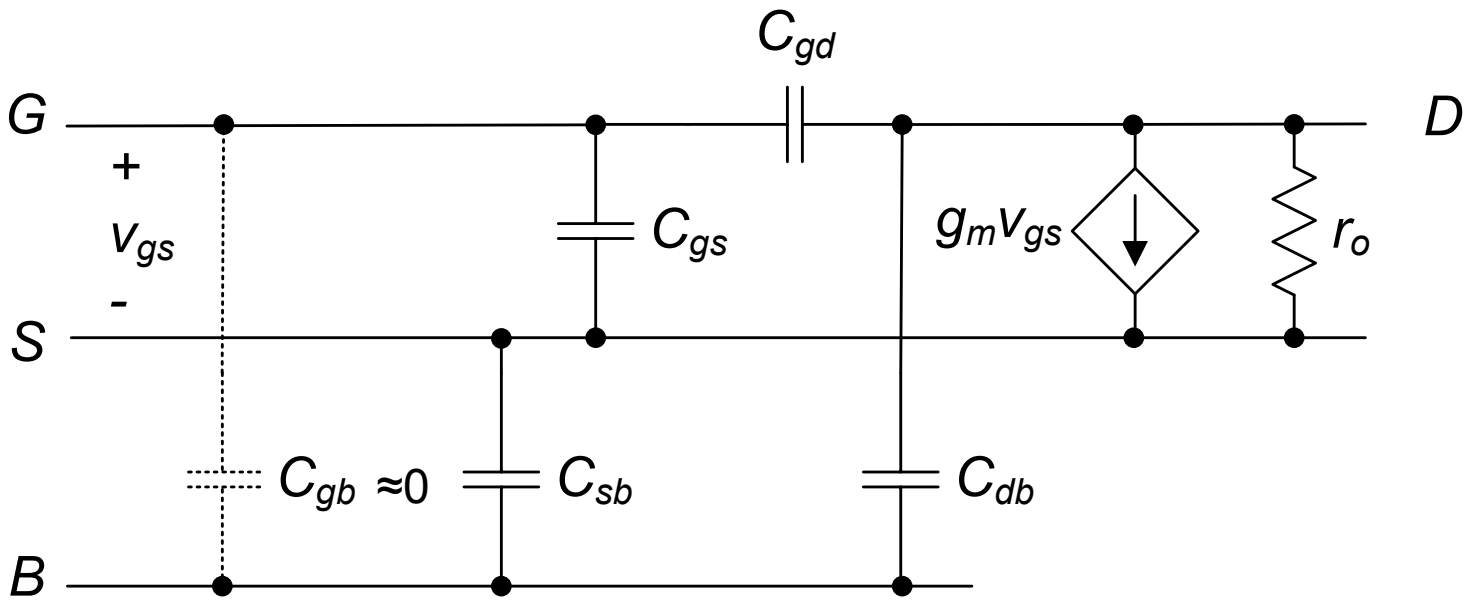
Extrinsic Capacitance

MOS Capacitance Simulation

- Note gradual transition in capacitance values

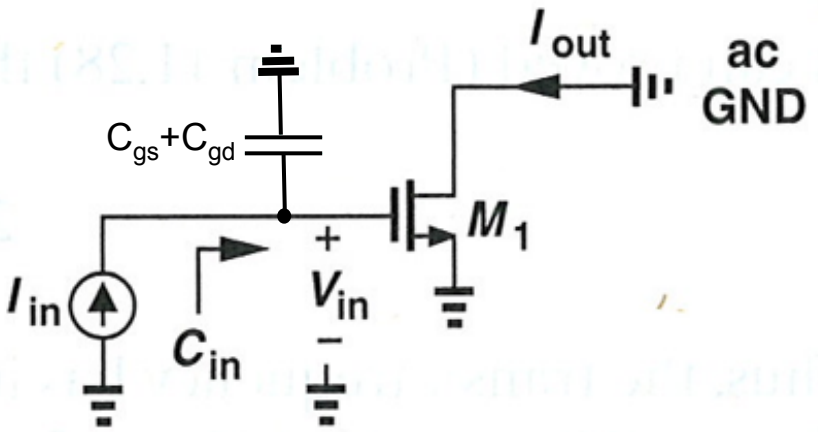


Small Signal Model with Capacitances



Transit Frequency with Extrinsic capacitances

$$\left.\frac{I_{out}}{I_{in}}\right|_{\omega=\omega_T} = 1$$



$$\omega_T = \frac{g_m}{C_{gs} + C_{gd}}$$

Parameter Summary (1)

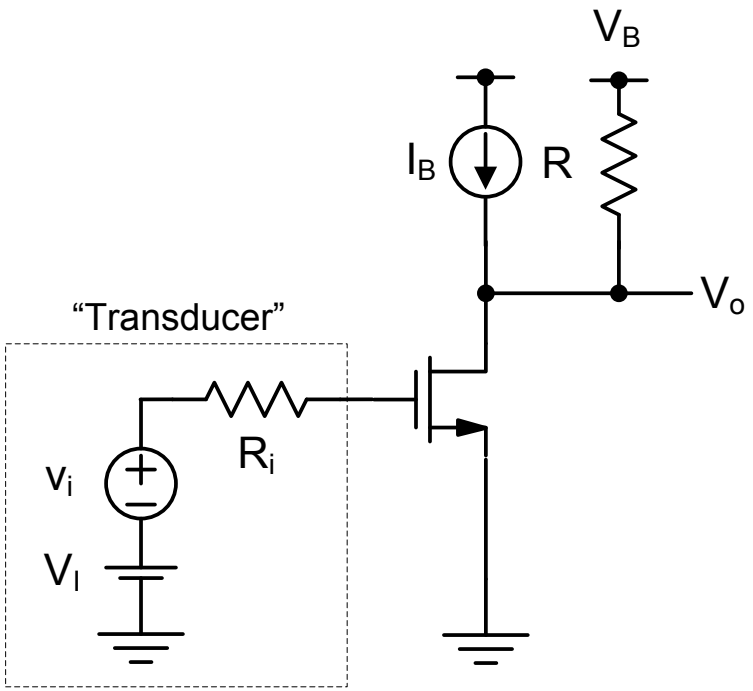
Parameter	Purpose	EE 114 Technology	
		NMOS	PMOS
KP	μC_{ox}	50 $\mu A/V^2$	25 $\mu A/V^2$
COX	ε_{ox}/t_{ox}	2.3 $fF/\mu m^2$	2.3 $fF/\mu m^2$
VTO	Threshold Voltage	0.5 V	−0.5 V
LAMBDA	Channel length modulation	0.1 $V^{-1}\mu m/L$	0.1 $V^{-1}\mu m/L$
CGDO, CGSO	Gate-drain/source overlap capacitance per length	0.5 $fF/\mu m$	0.5 $fF/\mu m$
CJ	Zero bias area capacitance	0.1 $fF/\mu m^2$	0.3 $fF/\mu m^2$
CJSW	Zero bias sidewall capacitance	0.5 $fF/\mu m$	0.35 $fF/\mu m$

Parameter Summary (2)

Parameter	Purpose	EE 114 Technology	
		NMOS	PMOS
PB	Junction Potential	0.95 V	0.95 V
MJ	Area Junction Grading Coefficient	0.5	0.5
MJSW	Area Junction Grading Coefficient	0.33	0.33
HDIF	Half-length of S/D diffusion ($=L_{diff}/2$)	1.5 μm	1.5 μm
GAMMA	Bulk Threshold Parameter	0.6 $V^{1/2}$	0.6 $V^{1/2}$
PHI	Surface Potential ($2\Phi_f$)	0.8 V	0.8 V

Needed Later

Common Source Amplifier (Revisited)



$V_B = 2.5V$

$V_I = 1.394V$

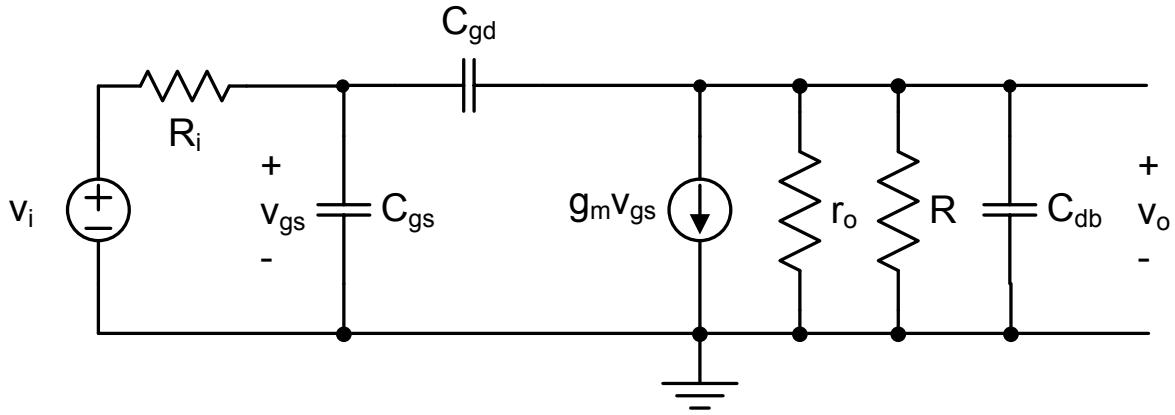
$I_B = 500mA$

$W/L = 20\mu m/1\mu m$

$R = 5k\Omega$

$R_i = 50k\Omega$

Small-Signal Model

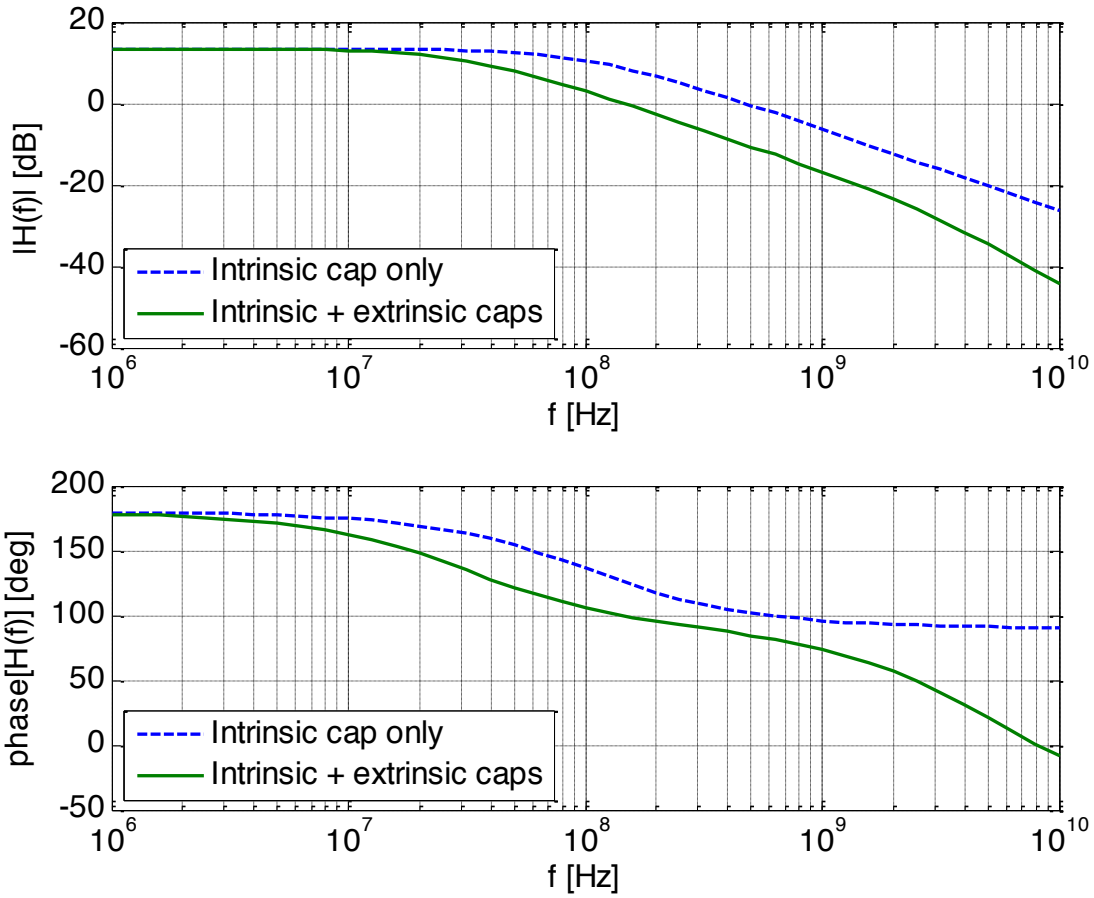


$$C_{gd} = W \cdot C'_{ov} = 20 \cdot 0.5\,fF = 10\,fF$$

$$C_{gs} = \frac{2}{3} WLC_{ox} + C_{ov} = \frac{2}{3} 20 \cdot 1 \cdot 2.3\,fF + 10\,fF = 40.67\,fF$$

$$C_{db} = \frac{AD \cdot CJ}{\left(1 + \frac{V_{DB}}{PB}\right)^{MJ}} + \frac{PD \cdot CJSW}{\left(1 + \frac{V_{DB}}{PB}\right)^{MJSW}} = \frac{60 \cdot 0.1\,fF}{\left(1 + \frac{2.5}{0.95}\right)^{0.5}} + \frac{26 \cdot 0.5\,fF}{\left(1 + \frac{2.5}{0.95}\right)^{0.33}} = 11.6\,fF$$

.AC SPICE Simulation



- Extrinsic caps reduce bandwidth from 103 MHz to 32 MHz !
- There also seems to be a second pole