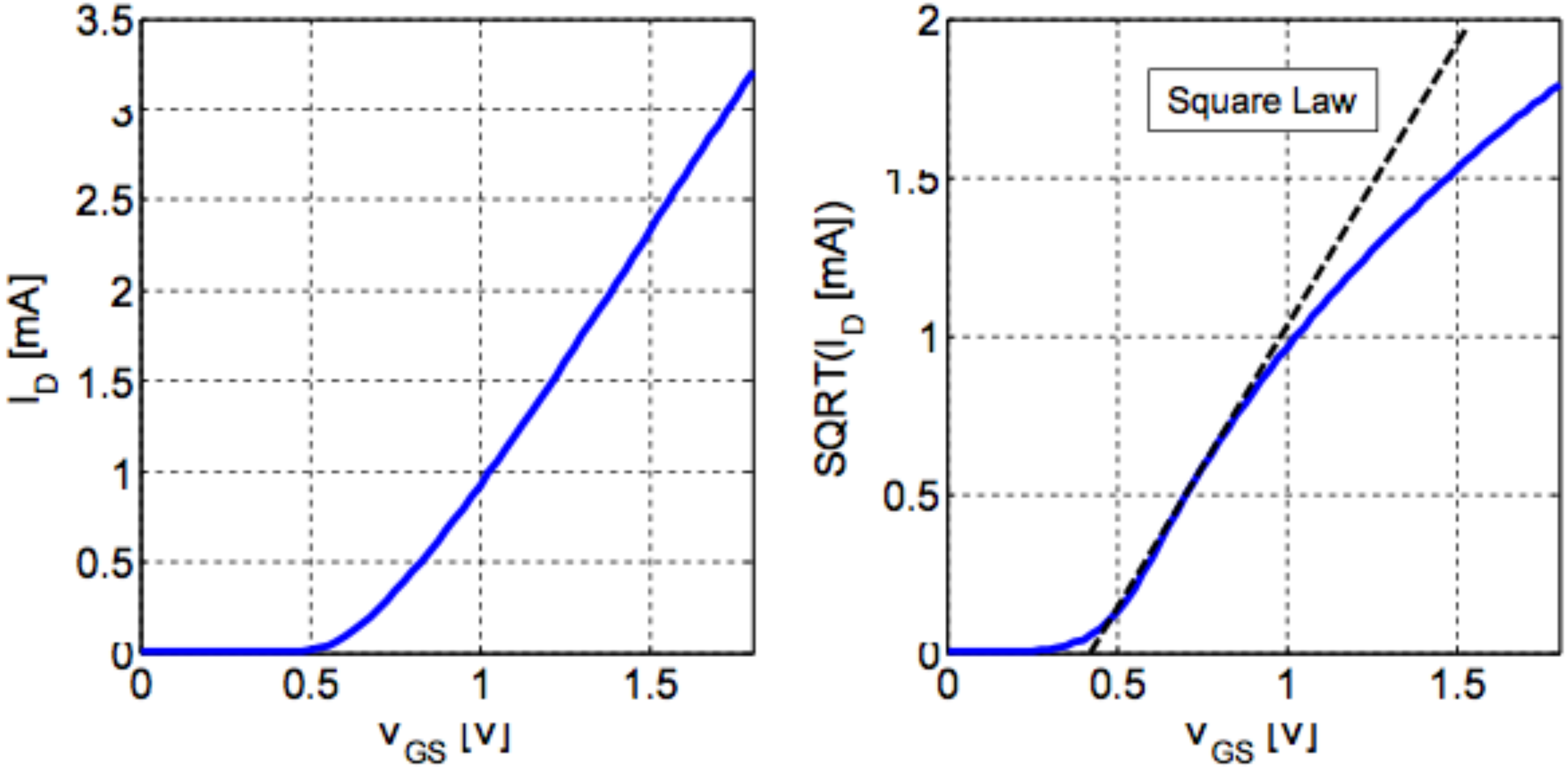
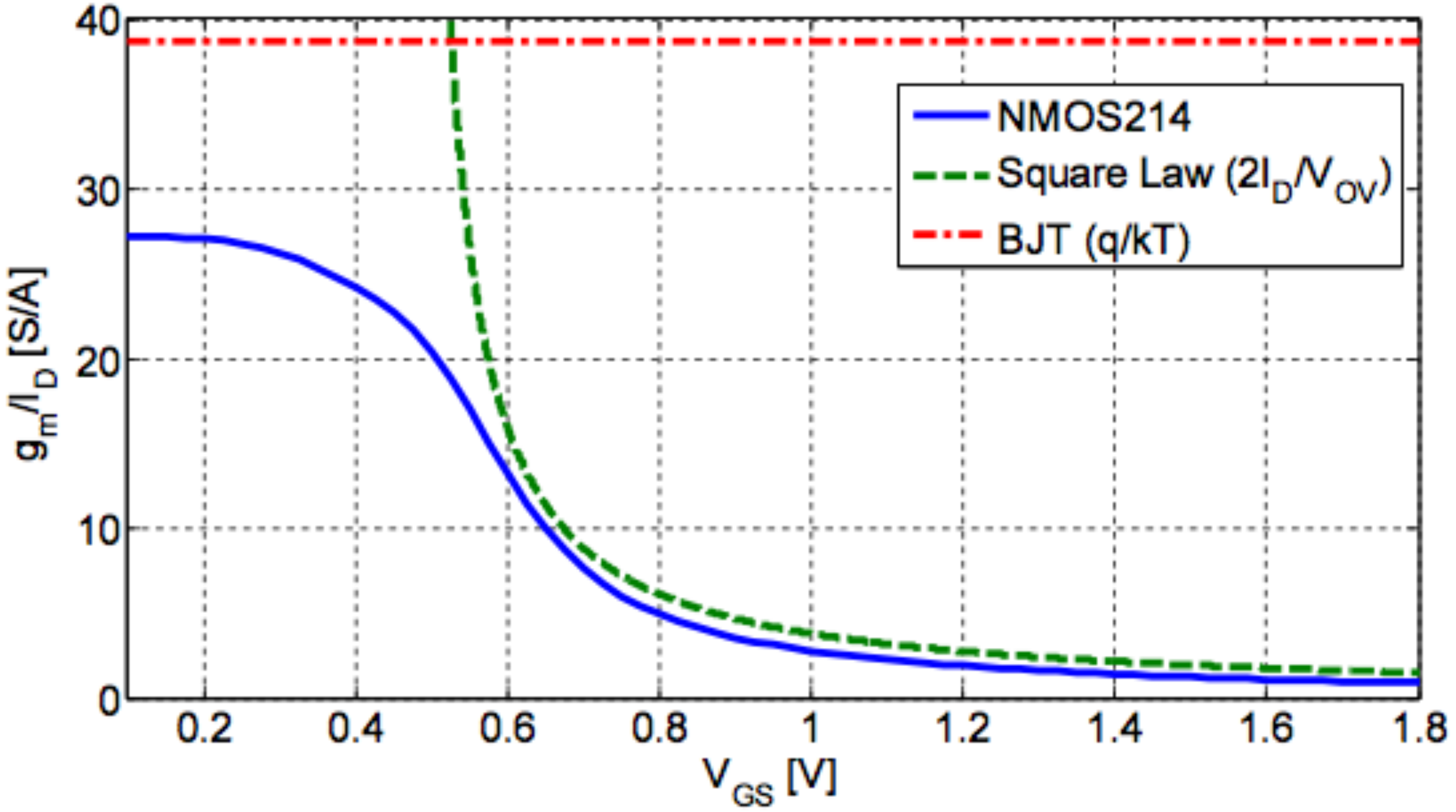
Short Channel MOSFET
vs.
Long Channel MOSFET

Issues with the Square Law model

Simulation (NMOS, 5/0.18μm, V_{DS}=1.8V)

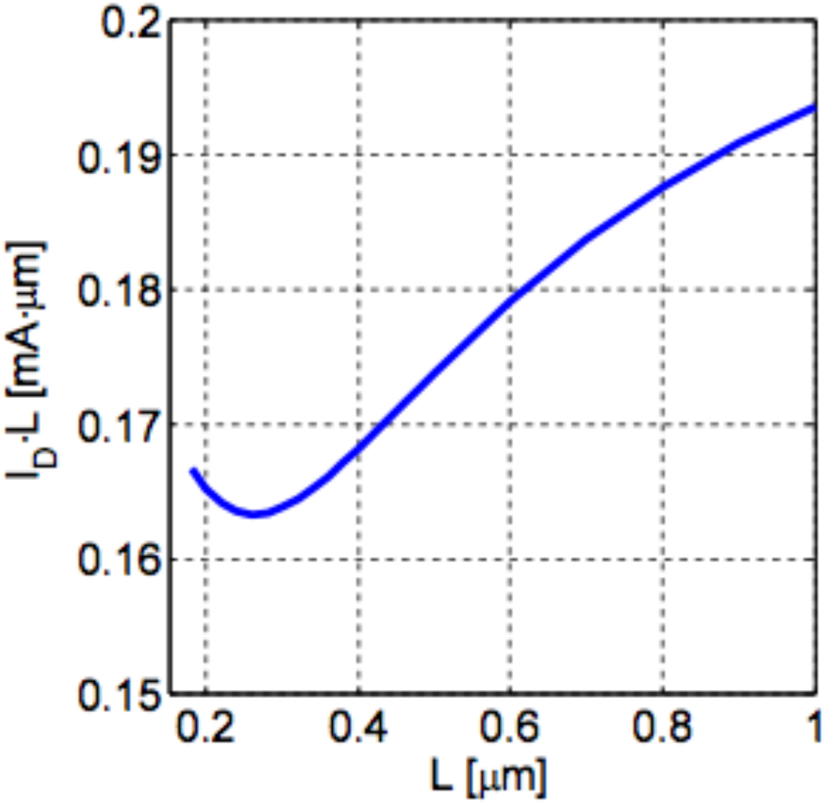


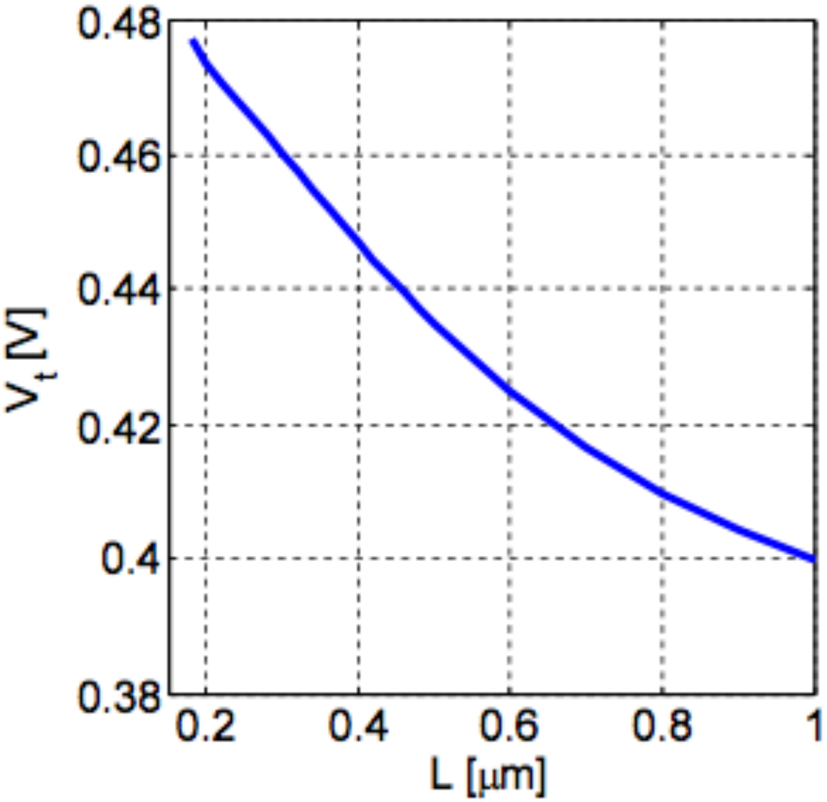
- Two observations
  - The transistor does not abruptly turn off at some V_t
  - The current is not perfectly quadratic in (V_{GS}–V_t)



- The square law fails miserably at predicting g_m/I_D for low V_{GS}

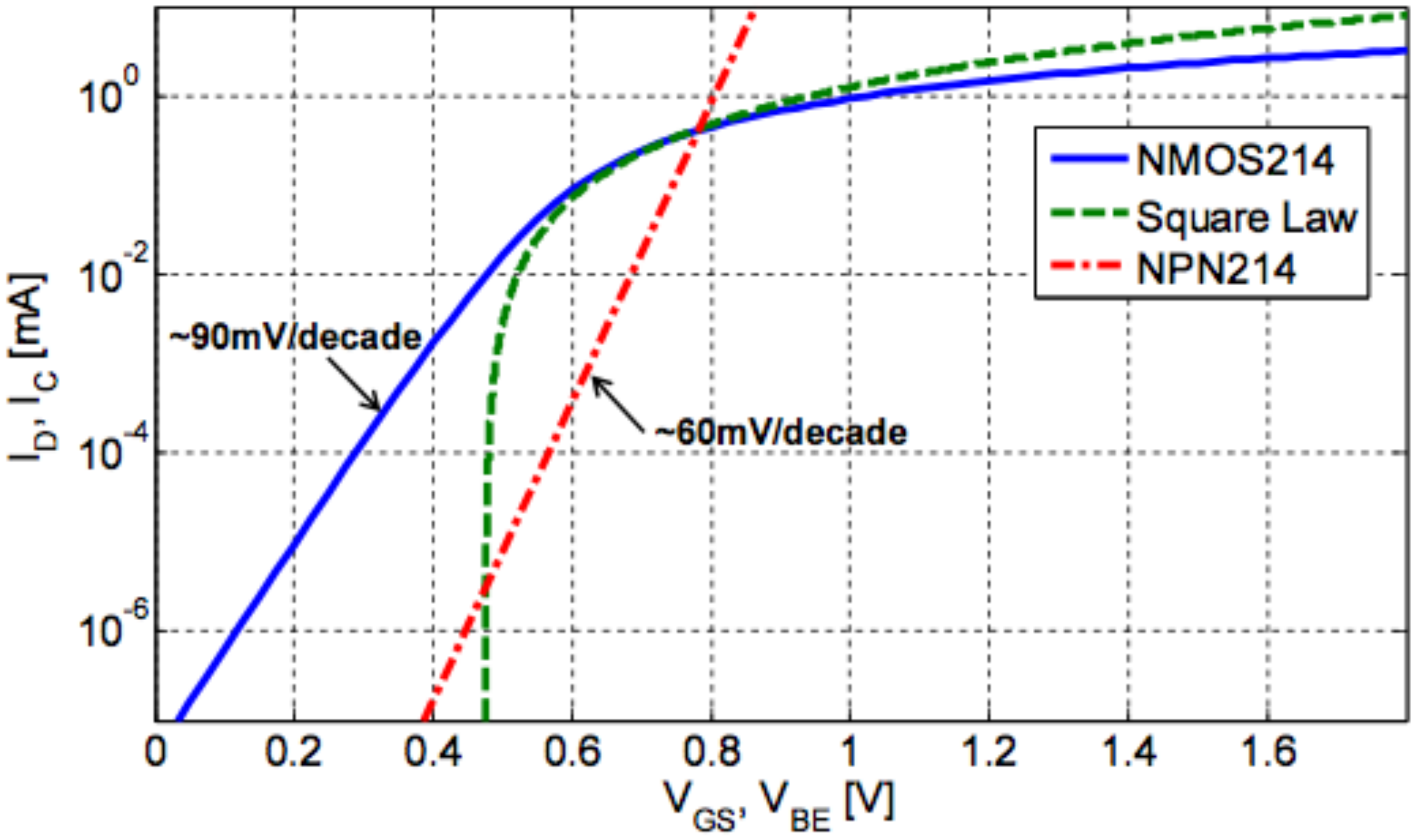
Additional Issues





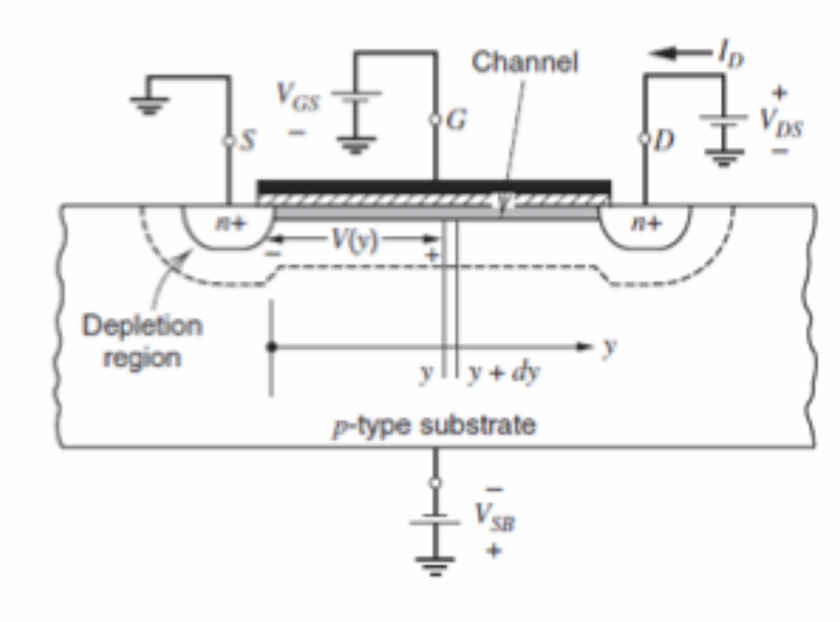
- The current does not scale perfectly with 1/L ($I_D \cdot L \neq$ const.)
- The threshold voltage of the device depends on the channel length

Currents on a Log Scale



- What is V_t, anyway? The device does not turn off at all, but really approaches an exponential IV law for low V_{GS}
- What determines the current at low V_{GS}?

Definition of Vt

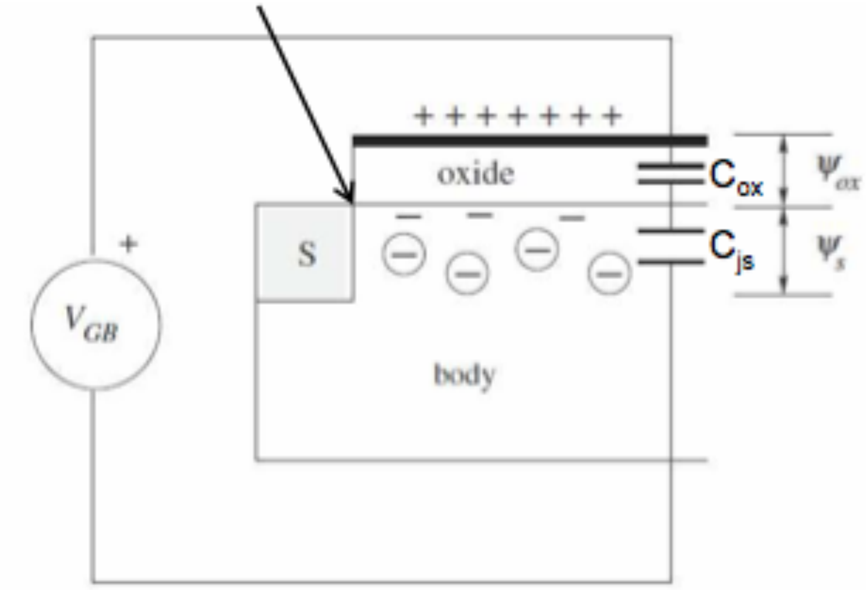


- V_t is (roughly speaking) defined as the V_{GS} at which the number of electrons at the surface equals the number of doping atoms
- Seems arbitrary, but makes sense in terms of surface charge control
  - This is the point where the surface becomes inverted (no more holes to fill) and the relationship between mobile charge and gate voltage becomes linear, $Q_n \propto C_{ox}(V_{GS}-V_t)$
  - Exactly what is assumed in the square law model

Weak Inversion

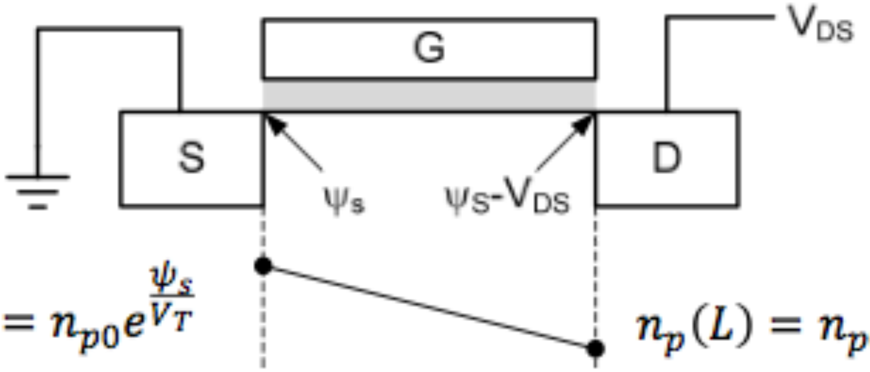
- Before inversion occurs, the electrostatic field from the gate forward-biases the source-side pn junction at the surface
- Physics governed by the "gated diode" model

Potential at this point is higher than body potential → forward bias



D.L. Pulfrey, Understanding Modern Transistors and Diodes, Cambridge University Press, 2010.

Resulting Diffusion Current



$$n_p(0) = n_{p0}e^{\frac{\psi_s}{V_T}}$$

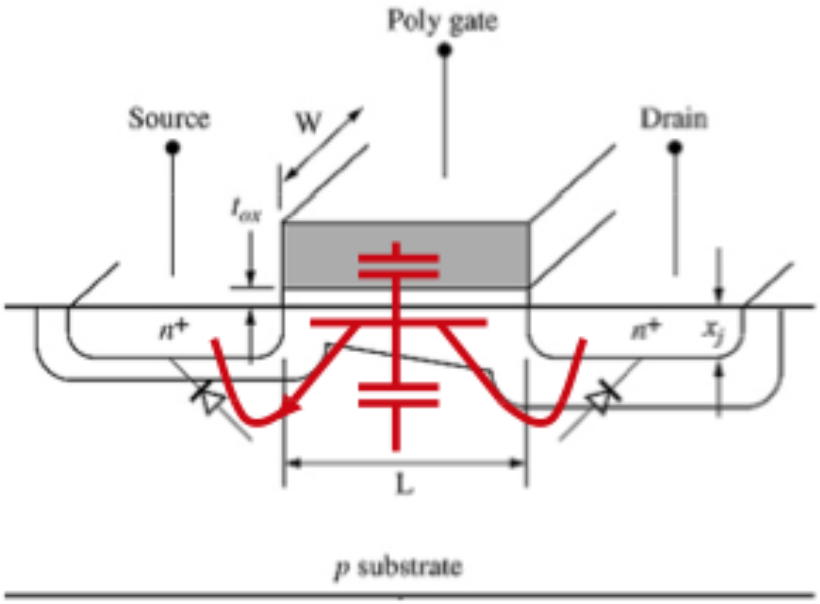
$$n_p(L) = n_{p0}e^{\frac{\psi_s - V_{DS}}{V_T}}$$

$$I_D = qAD_n \frac{n_p(L) - n_p(0)}{L}$$

$$I_D = qAD_n n_{p0} e^{\frac{\psi_s}{V_T}}(1 - e^{\frac{V_{DS}}{V_T}})$$

- The current grows exponentially with ψ_s
- The current becomes independent of V_{DS} for $V_{DS} > 3V_T$ (~78mV)

BJT Similarity



- We have
  - An NPN sandwich, mobile minority carriers in the P region
- This is a BJT!
  - Except that the base potential is here controlled through a capacitive divider, and not directly by an electrode

Capacitive Divider

$$\frac{d\psi_s}{dV_{GS}} = \frac{C_{ox}}{C_{js} + C_{ox}} = \frac{1}{n}$$

- n is called "subthreshold factor" or "nonideality factor"
- n ≅ 1.45 in the EE214B technology
- After including this relationship between ψ_s and V_{GS} and after a few additional manipulations, the final expression for the drain current becomes

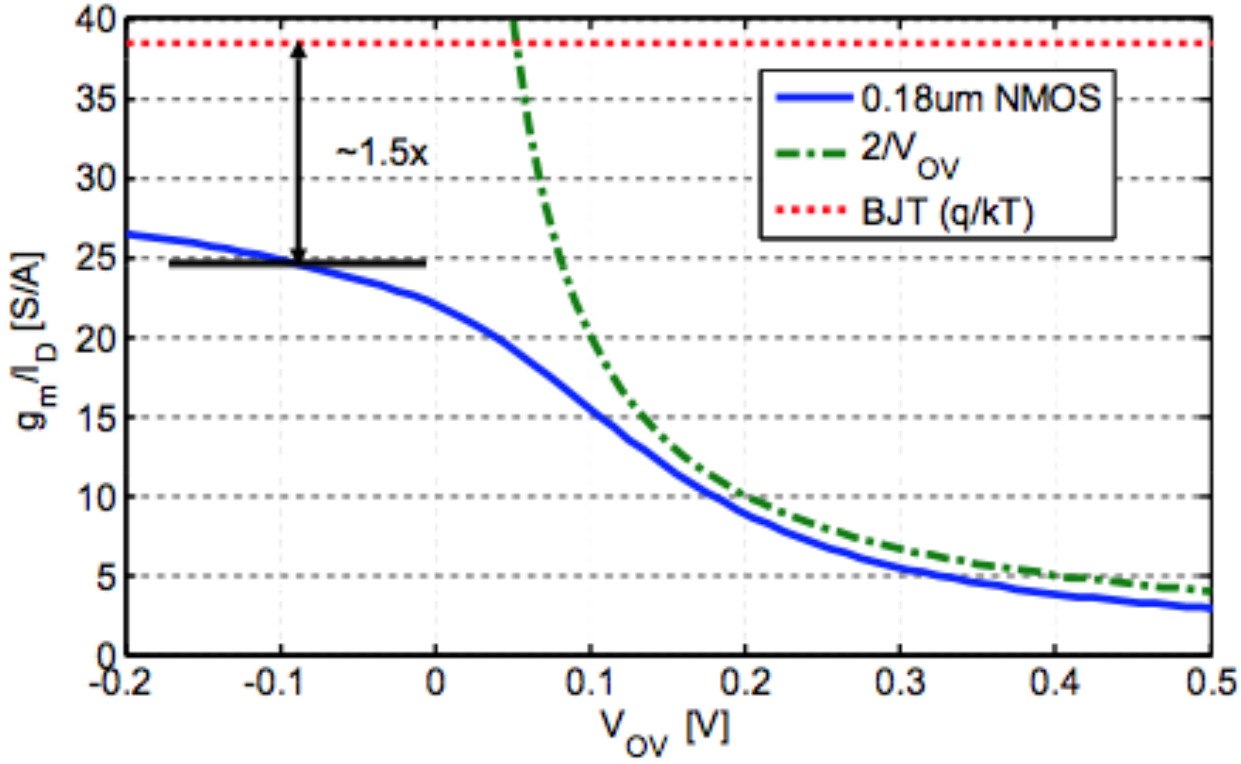
$$I_D = I_{D0} e^{\frac{V_{GS}-V_t}{V_t}} \left(1 - e^{\frac{V_{DS}}{V_t}}\right)$$

where I_{DO} depends on technology (I_{D0} ≅ 0.43μA for EE214B technology)

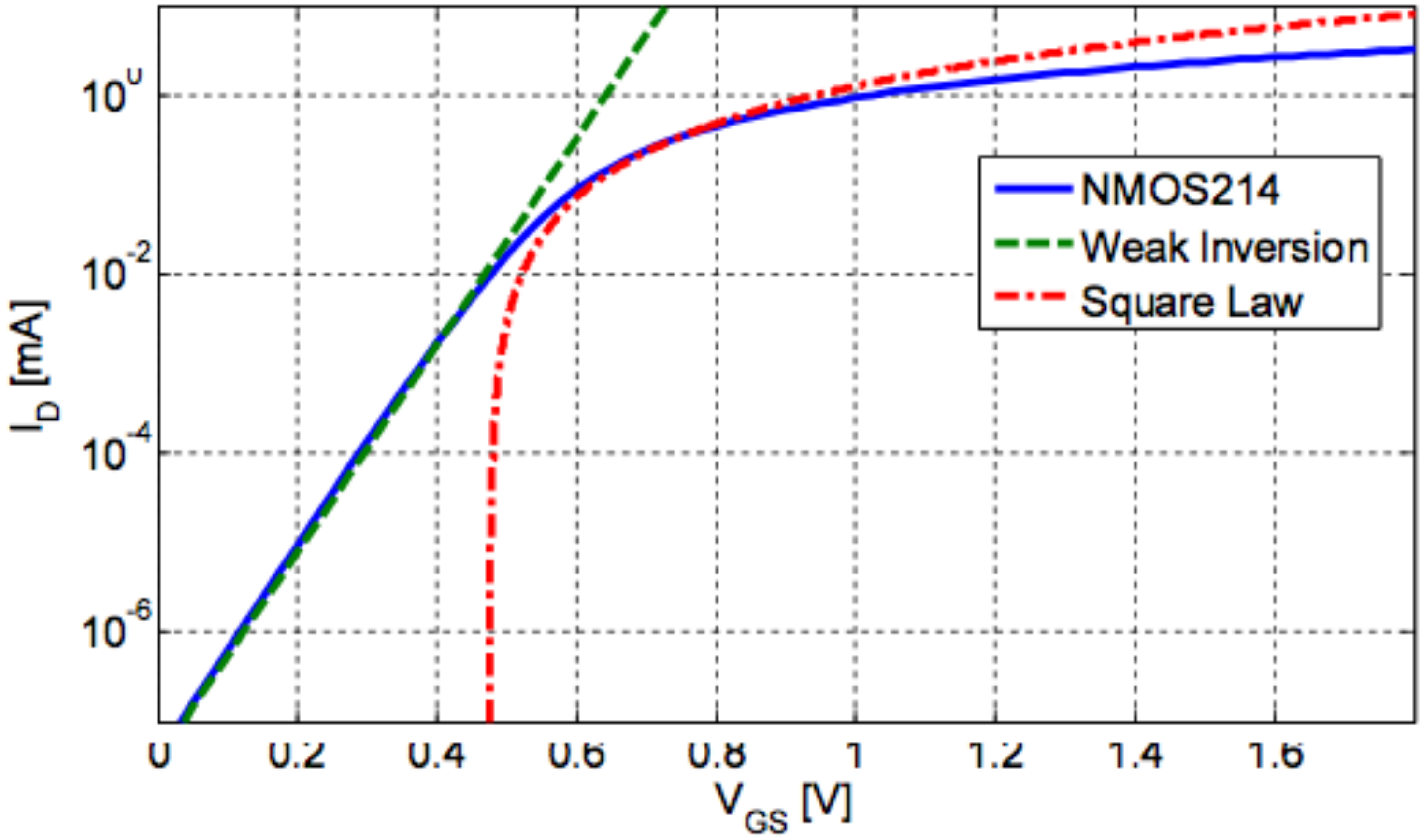
Subthreshold Transconductance

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{1}{n}\frac{I_D}{V_T} \qquad \frac{g_m}{I_D} = \frac{1}{nV_T}$$

- Similar to BJT, but unfortunately n (≅1.5) times lower

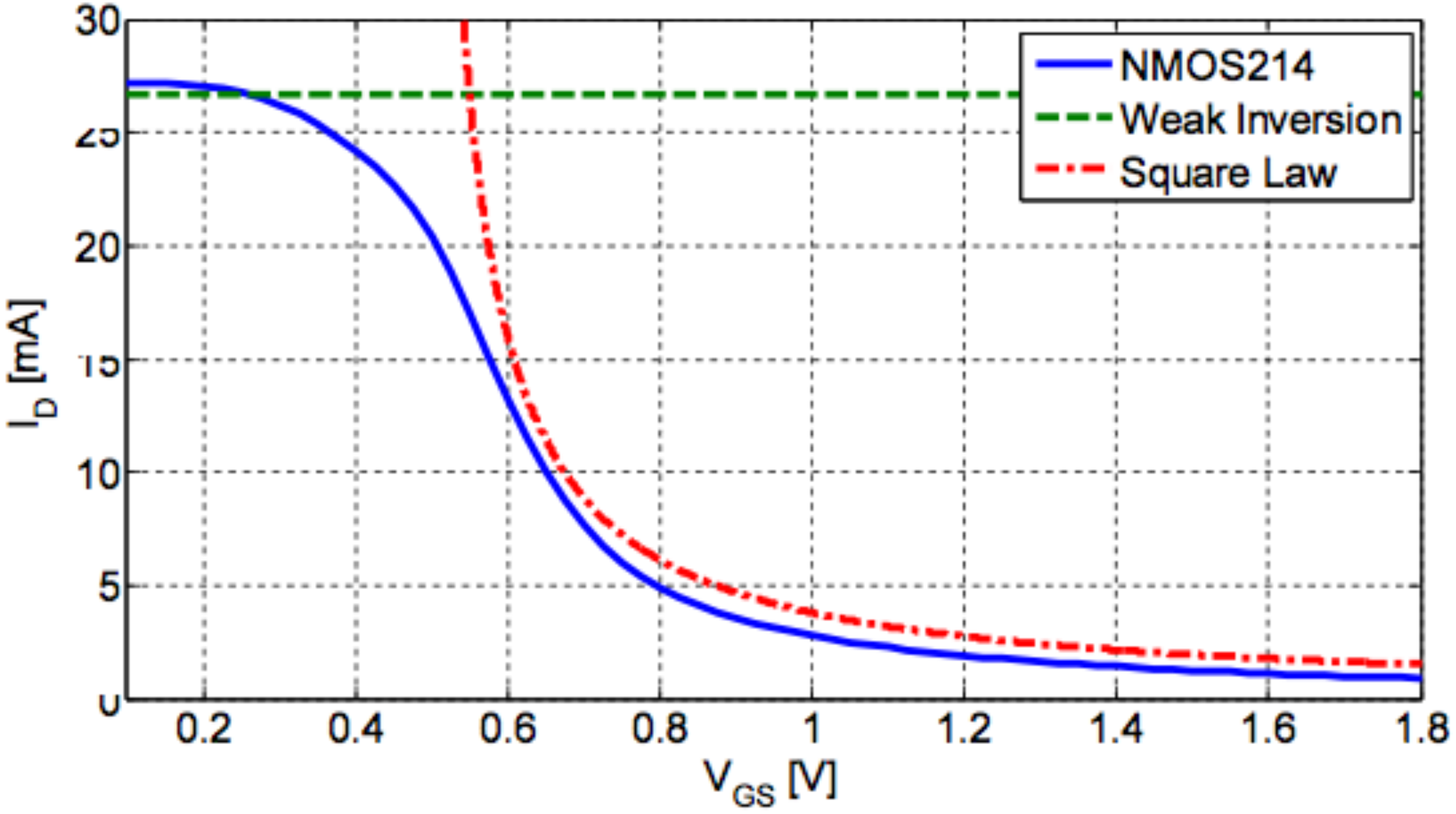


Combining the Weak Inversion Expression and Square Law



- Two remaining problems
  - The weak inversion expression and square law are disconnected
  - We still do not know what causes the discrepancies at high V_{GS}

G_m/I_D



- We now have a better idea now about the maximum possible g_m/I_D, but this does not help in the transistor region between the two IV laws

Moderate Inversion

- In the transition region between weak and strong inversion, the drain current consists of both drift and diffusion currents
- One can show that the ratio of drift/diffusion current in moderate inversion and beyond is approximately $(V_{GS}-V_t)/(kT/q)$
- This means that the square law equation (which assumes 100% drift current) does not work unless the gate overdrive is several kT/q
  - Recall that in EE214A, you used the square law model only for $V_{GS}-V_t > 150\text{mV} \cong 6\ kT/q$

Moderate Inversion

- In the transition region between subthreshold and strong inversion, we have two different current mechanisms

$$\text{Drift (MOS)} \qquad \nu = \mu E$$

$$\text{Diffusion (BJT)} \qquad \nu = D\frac{dn}{dx} = \frac{kT}{q}\mu\frac{dn}{dx}$$

- Both current components are always present
  - Neither one clearly dominates in moderate inversion
- Can show that ratio of drift/diffusion current ~$(V_{GS}-V_t)/(kT/q)$
  - MOS equation becomes dominant at several kT/q

Short Channel Effects

- The sub-square behavior at large V_{GS} is primarily due to a number of issues that fall under the category of “short channel effects”

- Onset of velocity saturation due to high lateral field
- Mobility degradation due to high vertical field
- Strong V_{DS} dependence of drain current and output resistance
- Threshold voltage depends on channel length and width

- Many more issues exist; we will once again only discuss the most relevant subset

Figures of Merit for Design

Square Law

- Transconductance efficiency
  - Want large g_m, for as little current as possible

$$\boxed{\frac{g_m}{I_D}} = \frac{2}{V_{OV}}$$

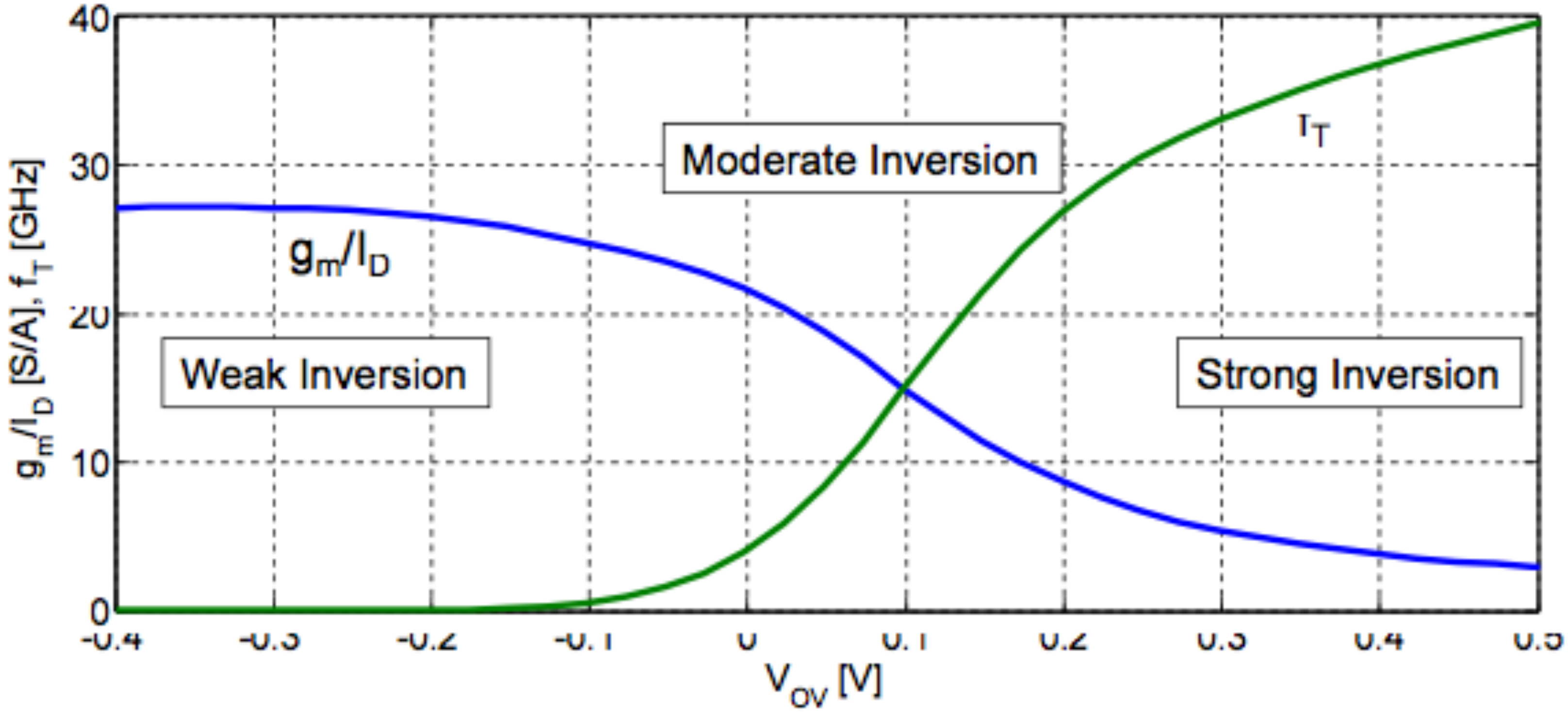
- Transit frequency
  - Want large g_m, without large C_{gg}

$$\boxed{\frac{g_m}{C_{gg}}} \cong \frac{3}{2}\frac{\mu V_{OV}}{L^2}$$

- Intrinsic gain
  - Want large g_m, but no g_o

$$\boxed{\frac{g_m}{g_o}} \cong \frac{2}{\lambda V_{OV}}$$

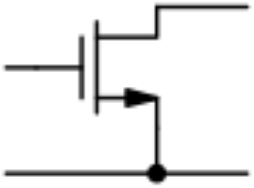
Design Tradeoff: g_m/I_D and f_T



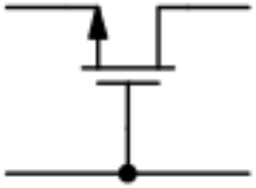
- Weak inversion: Large g_m/ID (>20 S/A), but small f_T
- Strong inversion: Small g_m/ID (<10 S/A), but large f_T

Elementary Amplifier Configurations

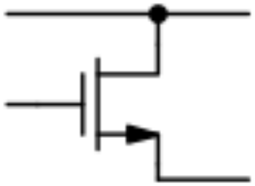
MOS



Common Source

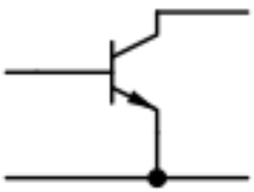


Common Gate

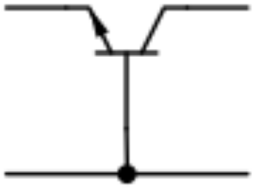


Common Drain

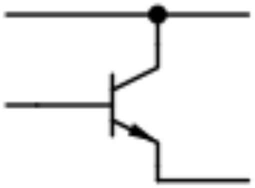
BJT



Common Emitter



Common Base



Common Collector

Transconductance Stage

Current Buffer

Voltage Buffer