

The goal of this lab. is to learn how to design and analyze a common source amplifier.

## Pre-Lab

1. Build a bias circuit resembling Figure 1.

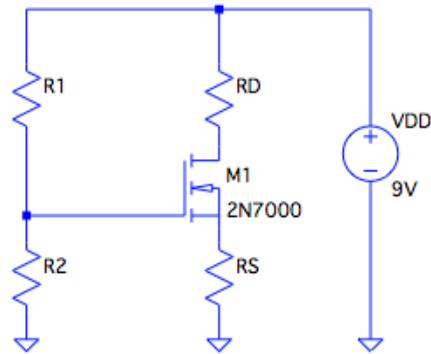


Figure 1.

Use the 2N7000 and a DC supply voltage of 9V. Choose bias resistors  $R_1$ ,  $R_2$ , and  $R_D = R_S$  to establish a bias point of  $I_D=5\text{mA}$  and  $V_{DS}=3\text{V}$ . The gate resistors ( $R_1$  and  $R_2$ ) should be larger than  $R_S$  by at least a factor of 10. Infer  $V_{TH}$  and  $\beta=\mu C_{ox}W/L$  of the 2N7000 from the datasheet.

$V_{TH} =$  \_\_\_\_\_

$\beta =$  \_\_\_\_\_

$V_{OV} =$  \_\_\_\_\_

$V_{GS} = V_{OV} + V_{TH} =$  \_\_\_\_\_

$R_1 =$  \_\_\_\_\_

$R_2 =$  \_\_\_\_\_

$R_D = R_S =$  \_\_\_\_\_

$g_m =$  \_\_\_\_\_

2. Use the proposed bias circuit to build a common source (CS) amplifier and predict the following quantities two different ways. The first prediction is done using hand calculations. The second prediction is done using SPICE. The quantities that need to be predicted are:  $g_m$ , gain, input impedance, and output impedance. The predictions should be made with and without a bypass capacitor across  $R_S$ .

In practice, use large capacitors for coupling and for creating AC shorts. For the capacitors to be sufficiently large make sure that  $1/\omega C \ll R$ , where  $R$  is the resistance facing the capacitor. If you use electrolytic capacitors pay attention to capacitor polarities.

## EE 303 - Laboratory

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For the 2N7000 use the following SPICE model:

```
.SUBCKT 2N7000 3 4 5
* Nodes      D G S
M1 3 2 5 5 MOD1
RG 4 2 343
RL 3 5 6E6
D1 5 3 DIODE1
.MODEL MOD1 NMOS VTO=2.474 RS=1.68 RD=0.0 IS=1E-15 KP=0.296
+CGSO=23.5P CGDO=4.5P CBD=53.5P PB=1 LAMBDA=267E-6
.MODEL DIODE1 D IS=1.254E-13 N=1.0207 RS=0.222
.ENDS 2N7000
```

Configuration	Predicted gm (Hand calculation)	Predicted gm (SPICE)	% Error
CS w/o bypass cap across RS			
CS w bypass across RS			

Configuration	Predicted Gain (Hand calculation)	Predicted Gain (SPICE)	% Error
CS w/o bypass cap across RS			
CS w bypass across RS			

Configuration	Predicted Rin (Hand calculation)	Predicted Rin (SPICE)	% Error
CS w/o bypass cap across RS			
CS w bypass across RS			

Configuration	Predicted Rout (Hand calculation)	Predicted Rout (SPICE)	% Error
CS w/o bypass cap across RS			
CS w bypass across RS			

Show the symbolic expressions you used for the hand prediction of the following quantities:

AV (w/o bypass cap) = \_\_\_\_\_

AV (w bypass cap) = \_\_\_\_\_

Rin (w/o bypass cap) = \_\_\_\_\_

Rin (w bypass cap) = \_\_\_\_\_

Rout (w/o bypass cap) = \_\_\_\_\_

Rout (w bypass cap) = \_\_\_\_\_

Draw the AC equivalent small signal circuit for both the case with and w/o bypass cap. across RS

a. AC circuit with bypass cap across RS

b. AC circuit w/o bypass cap across RS

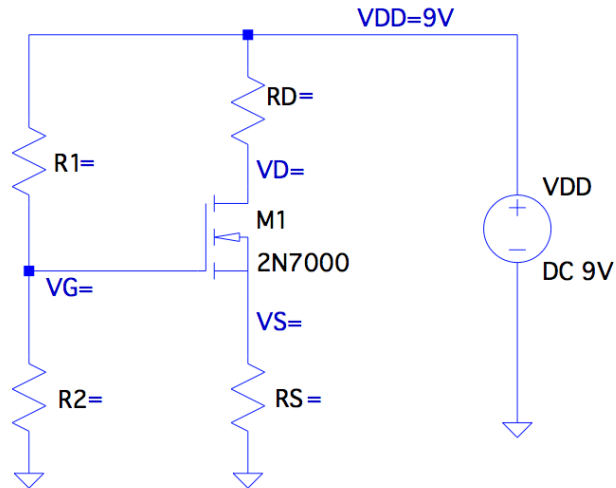
Attach the SPICE Bode plot for both the CS with and w/o bypass cap. across RS (hint: use .AC analysis).  
Clearly label the gain and the BW.

a. Attach the SPICE Bode Plot for CS w/o bypass cap across RS

- b. Attach the SPICE Bode Plot for CS with bypass cap across RS

## Lab.

1. First build the bias circuit and measure all the node voltages. Clearly annotate all voltages and resistor values on the following figure:



Based on the measurement compute  $g_m$  of the transistor.

$g_m =$  \_\_\_\_\_

2. Apply an AC signal to the gate (through a large coupling capacitor) and make a Bode Plot from 10 Hz to 100 KHz (hint: use the network analyzer tool).

Attach the Bode plot and clearly label the gain and the BW.

3. Apply an AC signal to the gate (through a large coupling capacitor), and then connect a large capacitor across RS (i.e. connect a large cap. between the source of the transistor and ground). Make a Bode Plot from 10 Hz to 100 KHz (hint: use the network analyzer tool).

Attach the Bode plot and clearly label the gain and the BW.