Name: _____

EE303 - Midterm Exam #2

Closed Book:
Two 8.5"x11" sheet of handwritten notes permitted
Calculator permitted

Important Notes:

- Read each problem completely and thoroughly
- Summarize all your answers in the boxes provided on these exam sheets
- Make sure to mark the units on your answers!
- Do all your work on the exams sheets provided. If you use any additional sheets, please turn them in, so we can consider all work for partial credit
- Do not forget to put your name in the space above

Problem #	Points	Score
1	15	
2	10	
3	15	
4	10	
5	10	
6	15	
7	10	
TOTAL	**85**	

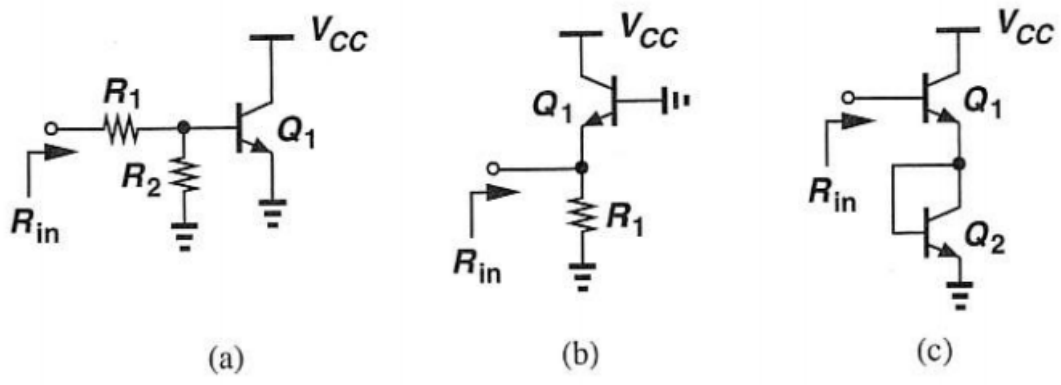
Unless otherwise specified assume:

NMOS: $\mu_n C_{OX} = 200\ \mu A/V^2$ and $V_{THn} = 0.4V$
PMOS: $\mu_p C_{OX} = 100\ \mu A/V^2$ and $V_{THp} = -0.4V$

Name:

Problem 1 [15 pts]

Compute the input resistance for the following circuits. Assume $V_A = \infty$

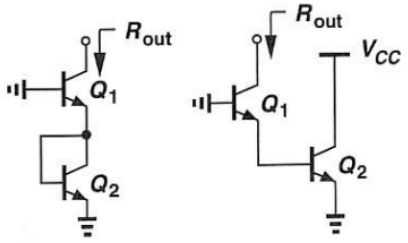


a) R_{in}	
b) R_{in}	
c) R_{in}	

Name:

Problem 2 [10 pts]

Compute the output resistance for the following circuits. Assume V_A is finite:



(a) (b)

(a) R_{out} =	
(b) R_{out} =	

Name:

Problem 3 [15 pts]

The CS stage of Fig. 7.56 must provide a voltage gain of 10 with a bias current of 0.5 mA. Assume $\lambda_1 = 0.1\ V^{-1}$, and $\lambda_2 = 0.15\ V^{-1}$.

(a) Compute the required value of $(W/L)_1$.

(b) If $(W/L)_2 = 20/0.18$, calculate the required value of V_B.

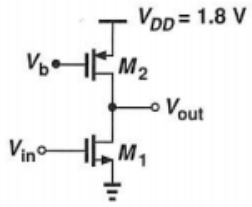


Figure 7.56

$(W/L)_1$ =	
V_B =	

Name:

Problem 4 [10 pts]

. We wish to design the circuit shown in Fig. 7.59 for a voltage gain of 3. If $(W/L)_1 = 20/0.18$, determine $(W/L)_2$. Assume $\lambda = 0$.

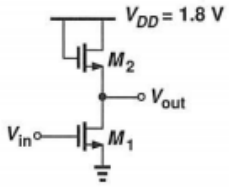


Figure 7.59

$(W/L)_2$ =	

Name:

Problem 5 [10 pts]

We wish to design the source follower shown in Fig. 7.77 for a voltage gain of 0.8. If $W/L = 30/0.18$ and $\lambda = 0$, determine the required gate bias voltage.

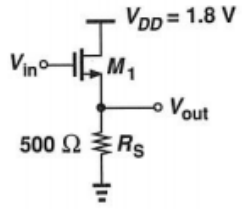


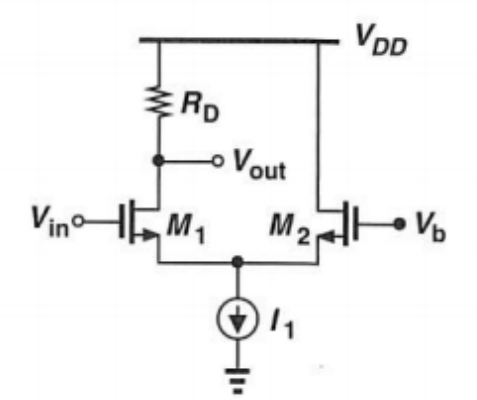
Figure 7.77

V_G =	

Name:

Problem 6 [15 pts]

Calculate the voltage gain, the input impedance and the output impedance of the circuit depicted in fig. Assume channel length modulation is negligible.
NOTE: V_b is a DC bias voltage.



$A_v = v_{out}/v_{in} =$	
$R_{in} =$	
$R_{out} =$	

Name:

Problem 7 [10 pts]

Compute the output resistance of the circuits depicted in Fig. 9.50. Assume all of the transistors operate in saturation and $g_m r_O \gg 1$.

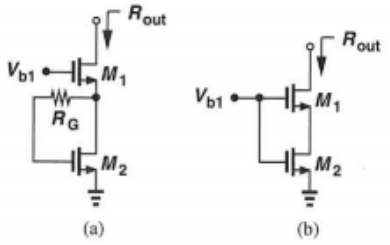


Figure 9.50

(a) R_{out} =	
(b) R_{out} =	