EE303 - Problem Set

In the following problems, unless otherwise stated, assume $\mu_n C_{ox} = 200\,\mu\text{A/V}^2$, $\mu_p C_{ox} = 100\,\mu\text{A/V}^2$, $\lambda = 0$, and $V_{TH} = 0.4\,\text{V}$ for NMOS devices and $-0.4\,\text{V}$ for PMOS devices.

Problem 1

We wish to design the circuit of Fig. 7.40 for a drain current of 1 mA. If $W/L = 20/0.18$, compute R_1 and R_2 such that the input impedance is at least 20 kΩ.

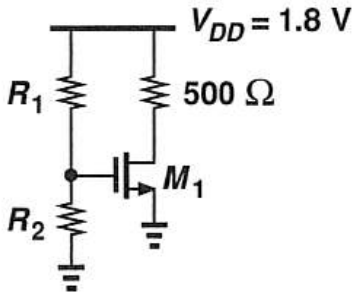

Figure 7.40

Problem 2

Consider the circuit shown in Fig. 7.41. Calculate the maximum transconductance that M_1 can provide (without going into the triode region.)

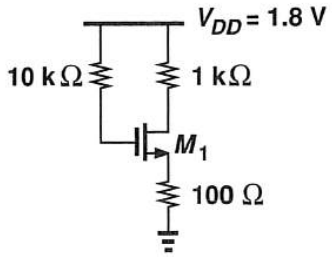

Figure 7.41

Problem 3

. The circuit of Fig. 7.42 must be designed for a voltage drop of 200 mV across R_S.
(a) Calculate the minimum allowable value of W/L if M_1 must remain in saturation.
(b) What are the required values of R_1 and R_2 if the input impedance must be at least 30 kΩ?

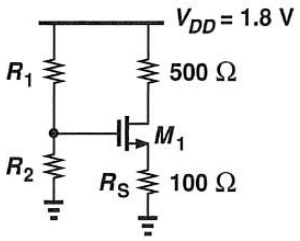

Figure 7.42

Problem 4

The self-biased stage of Fig. 7.44 must be designed for a drain current of 1 mA. If M_1 is to provide a transconductance of $1/(100\ \Omega)$, calculate the required value of R_D.

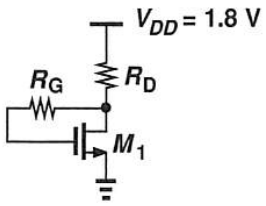

Figure 7.44

Problem 5

The CS stage of Fig. 7.56 must provide a voltage gain of 10 with a bias current of 0.5 mA. Assume $\lambda_1 = 0.1\,\mathrm{V}^{-1}$, and $\lambda_2 = 0.15\,\mathrm{V}^{-1}$.

(a) Compute the required value of $(W/L)_1$.

(b) If $(W/L)_2 = 20/0.18$, calculate the required value of V_B.

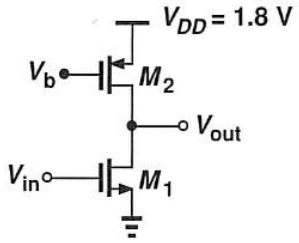

Figure 7.56