EE303 - Problem Set

In the following problems, unless otherwise stated, assume $\mu_n C_{ox} = 200\,\mu\text{A/V}^2$, $\mu_p C_{ox} = 100\,\mu\text{A/V}^2$, $\lambda = 0$, and $V_{TH} = 0.4\,\text{V}$ for NMOS devices and $-0.4\,\text{V}$ for PMOS devices.

Problem 1

. In the common-source stage of Fig. 7.54, $W/L = 30/0.18$ and $\lambda = 0$.

(a) What gate voltage yields a drain current of 0.5 mA? (Verify that M_1 operates in saturation.)

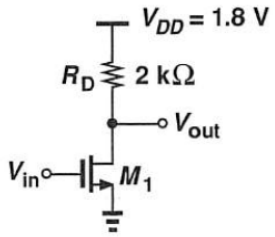


Figure 7.54

(b) With such a drain bias current, calculate the voltage gain of the stage.

Problem 2

. We wish to design the circuit shown in Fig. 7.59 for a voltage gain of 3. If $(W/L)_1 = 20/0.18$, determine $(W/L)_2$. Assume $\lambda = 0$.

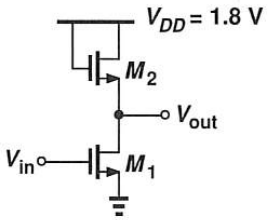


Figure 7.59

Problem 3

The degenerated CS stage of Fig. 7.61 must provide a voltage gain of 4 with a bias current of 1 mA. Assume a drop of 200 mV across R_S and $\lambda = 0$.

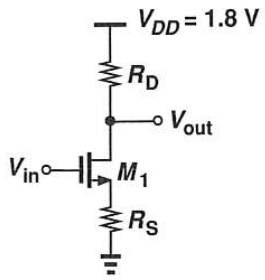


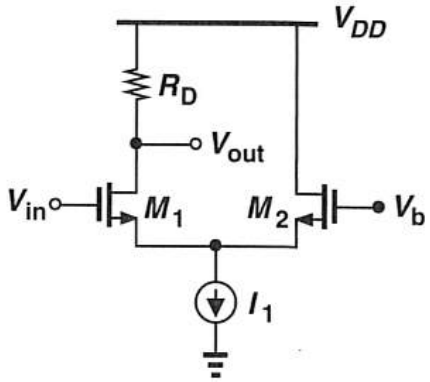
Figure 7.61

(a) If $R_D = 1\,\text{k}\Omega$, determine the required value of W/L. Does the transistor operate in saturation for this choice of W/L?

(b) If $W/L = 50/0.18$, determine the required value of R_D. Does the transistor operate in saturation for this choice of R_D?

Problem 4

Calculate the voltage gain, the input impedance and the output impedance of the circuit depicted in fig. Assume channel length modulation is negligible.
NOTE: V_b is a DC bias voltage.



Problem 5

Consider the circuit of Fig. 7.72, where a common-source stage (M_1 and R_{D1}) is followed by a common-gate stage (M_2 and R_{D2}).

(a) Writing $v_{out}/v_{in} = (v_X/v_{in})(v_{out}/v_X)$ and assuming $\lambda = 0$, compute the overall voltage gain.

(b) Simplify the result obtained in (a) if $R_{D1} \to \infty$. Explain why this result is to be expected.

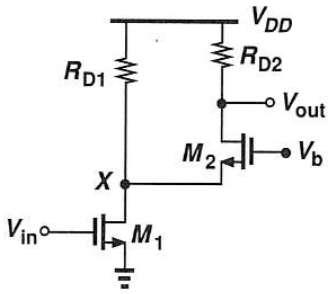


Figure 7.72

NOTE: Vb is a DC bias voltage.

Problem 6

We wish to design the source follower shown in Fig. 7.77 for a voltage gain of 0.8. If $W/L = 30/0.18$ and $\lambda = 0$, determine the required gate bias voltage.

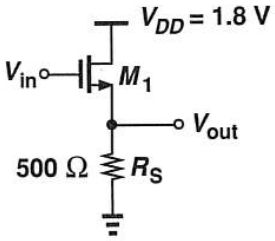


Figure 7.77

Problem 7

We wish to design the source follower of Fig. 7.79 for a voltage gain of 0.8 with a power budget of 3 mW. Compute the required value of W/L. Assume C_1 is very large and $\lambda = 0$.

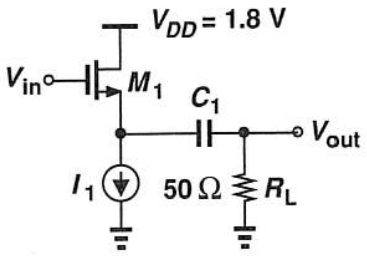


Figure 7.79