# Introduction to CMOS Digital Logic Circuits

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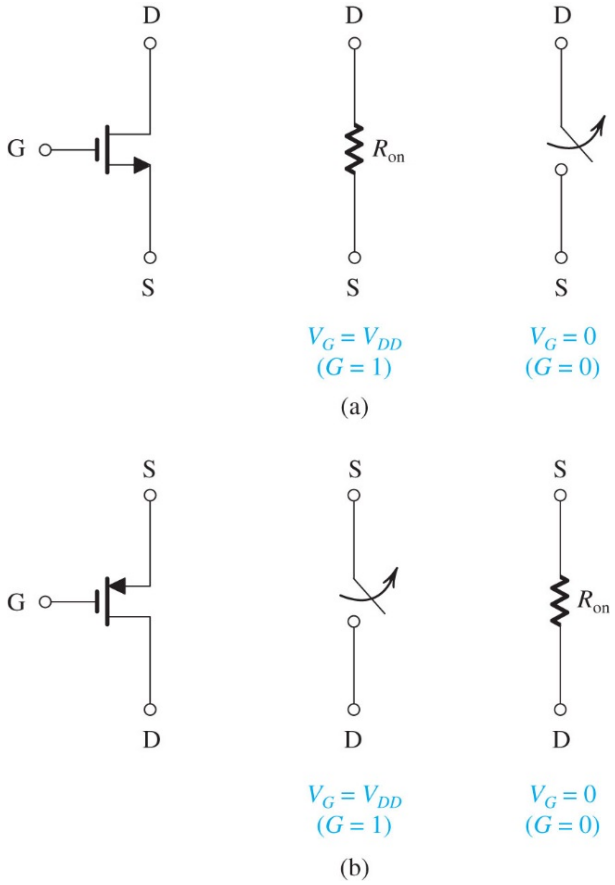
# MOSTs as switches




For a transistor in triode region if $V_{GS} - V_t << V_{DS}$:

$$R_{on} \equiv R_{DS} \approx \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_t)}$$

**Figure 14.1** Operation of the (**a**) NMOS and (**b**) PMOS transistor as an on/off switch. The gate voltage controls the operation of the transistor switch, with the voltage $V_{DD}$ representing a logic 1 and 0 V representing a logic 0. Note that the connections of the drain and source terminals are not shown.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# The CMOS inverter

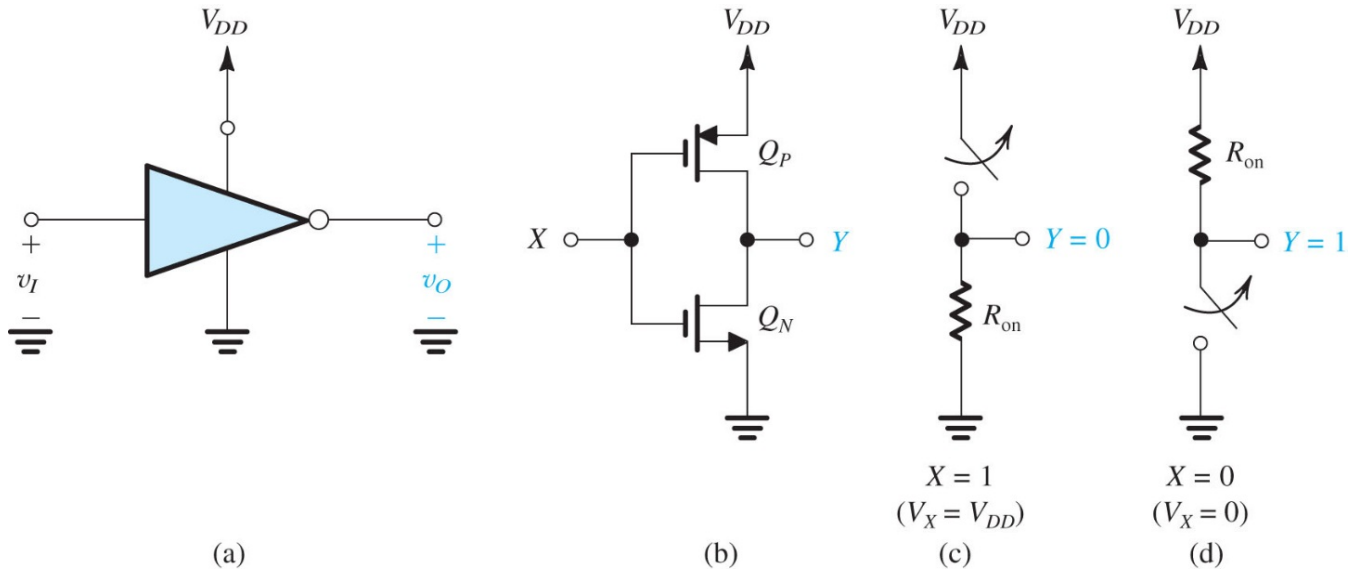


**Figure 14.2** (**a**) Block representation of the logic inverter; (**b**) its CMOS realization; (**c**) operation when the input is a logic 1; (**d**) operation when the input is a logic 0.

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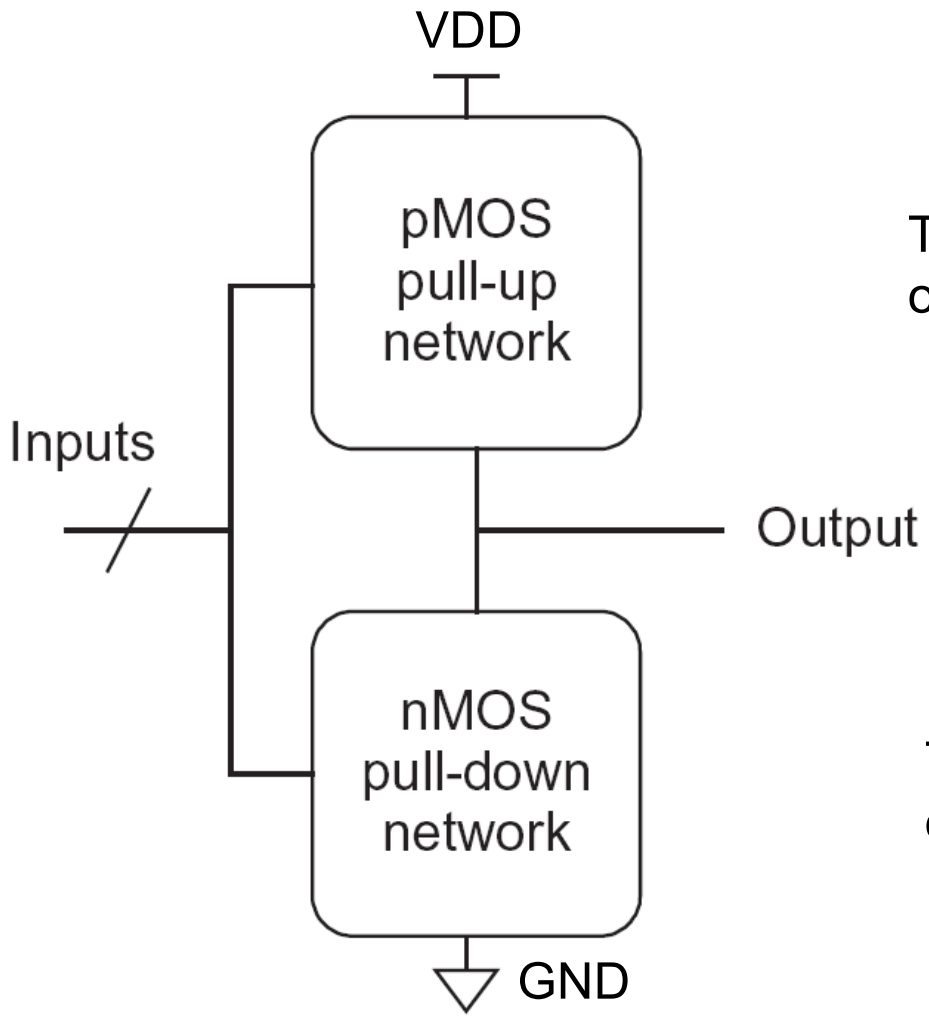
# General CMOS logic gate structure




The PUN is made only of pMOSTs

The PUN and the PDN are complementary

The PDN is made only of nMOSTs

# Examples of pull-down networks

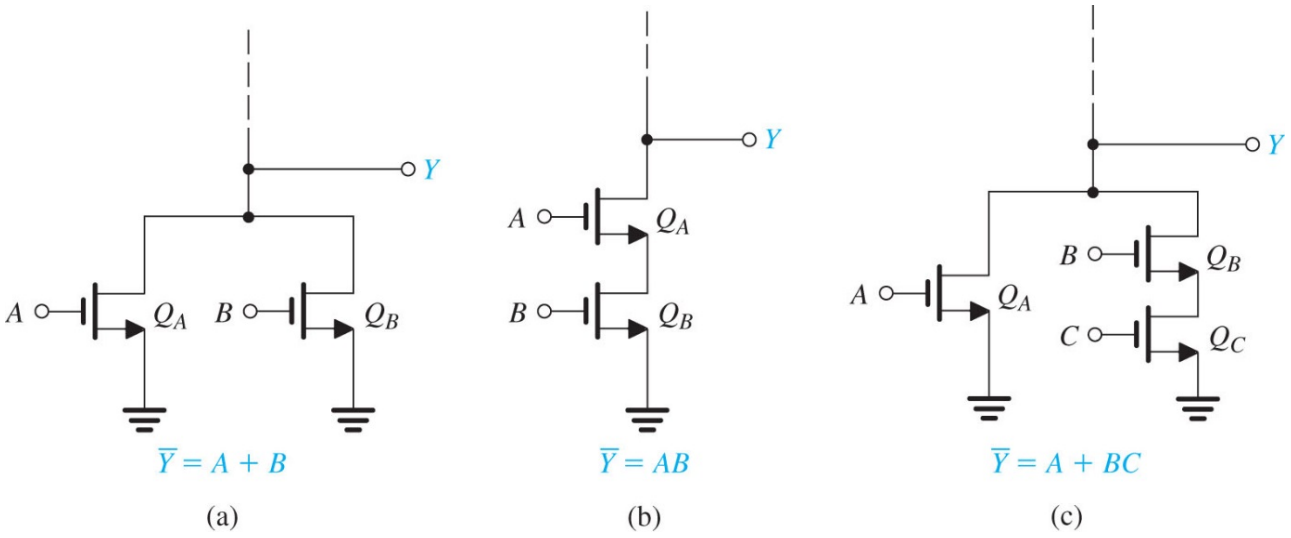



**Figure 14.4** Examples of pull-down networks.

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# Examples of pull-up networks

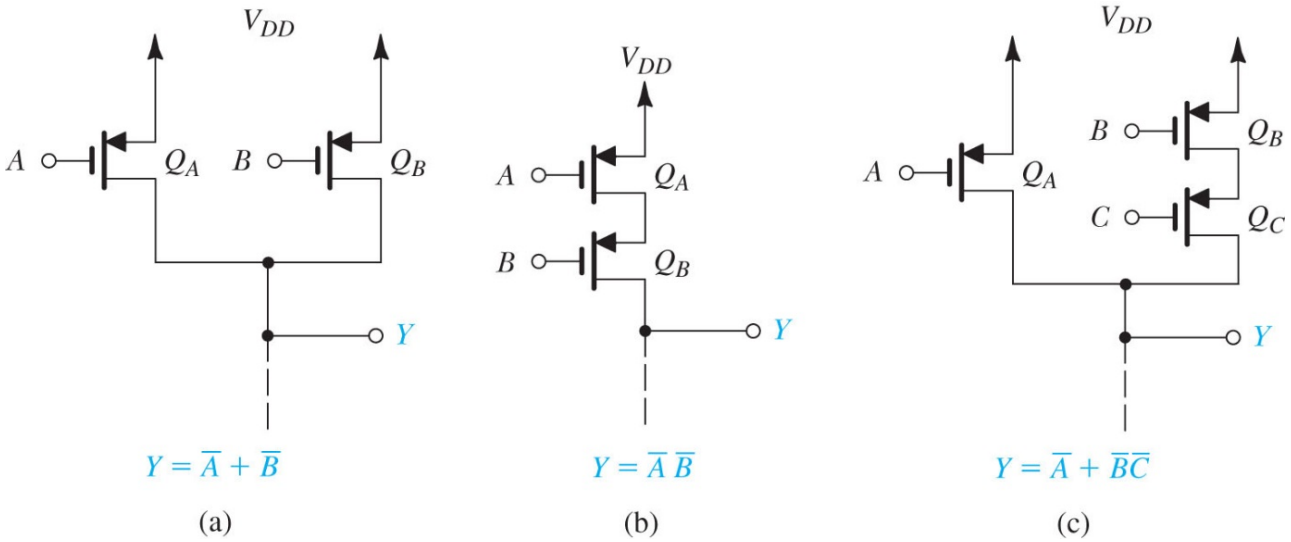


**Figure 14.5** Examples of pull-up networks.

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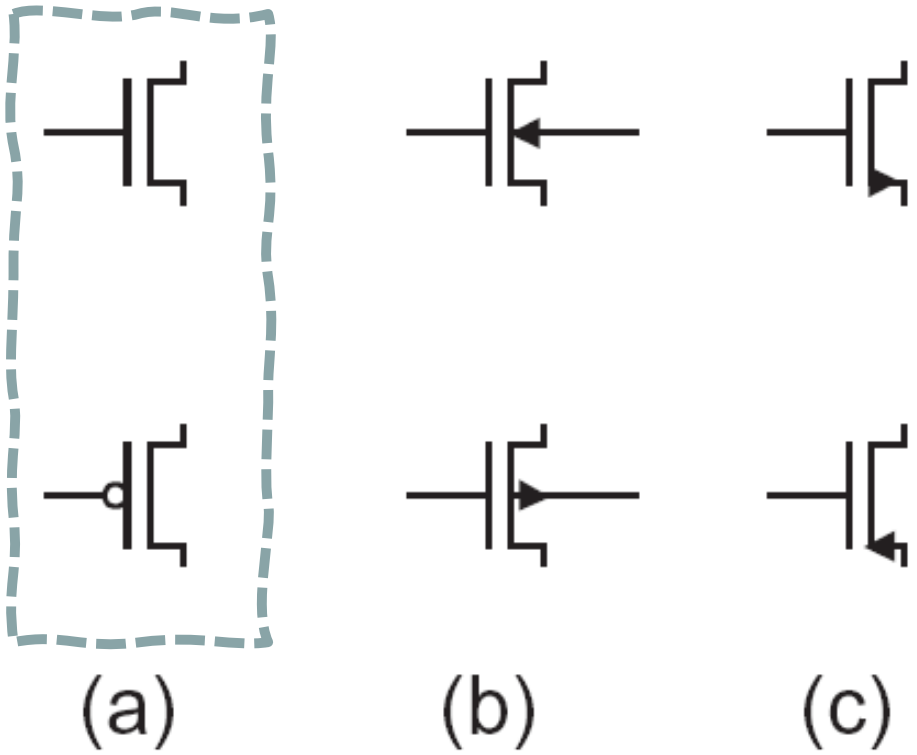
# MOSTs symbols used in “digital logic”

The body terminal of all pMOSTs is “assumed” connected to VDD

The body terminal of all nMOSTs is “assumed” connected to GND



# Example: CMOS NOR gate

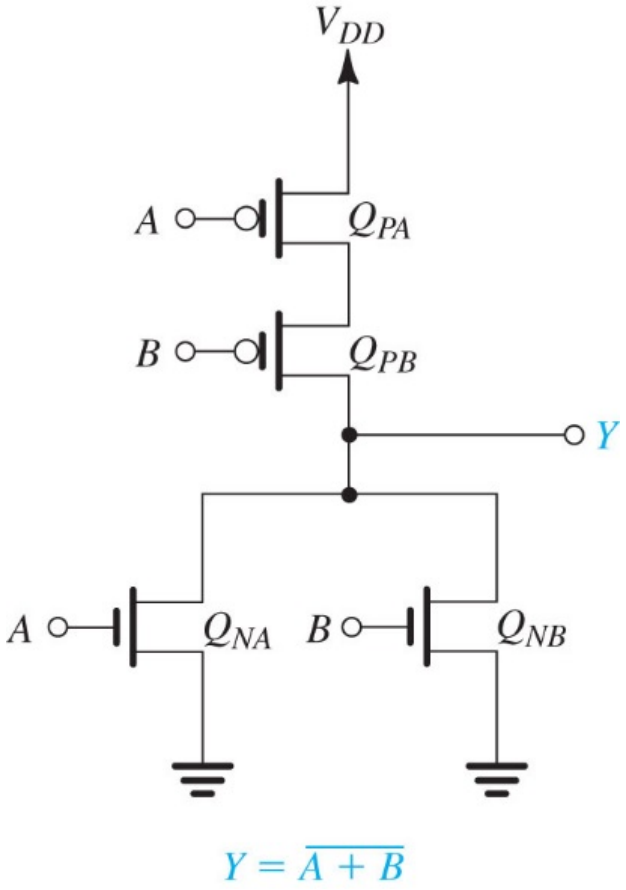



**Figure 14.7** A two-input CMOS NOR gate.

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# Example: CMOS NAND gate

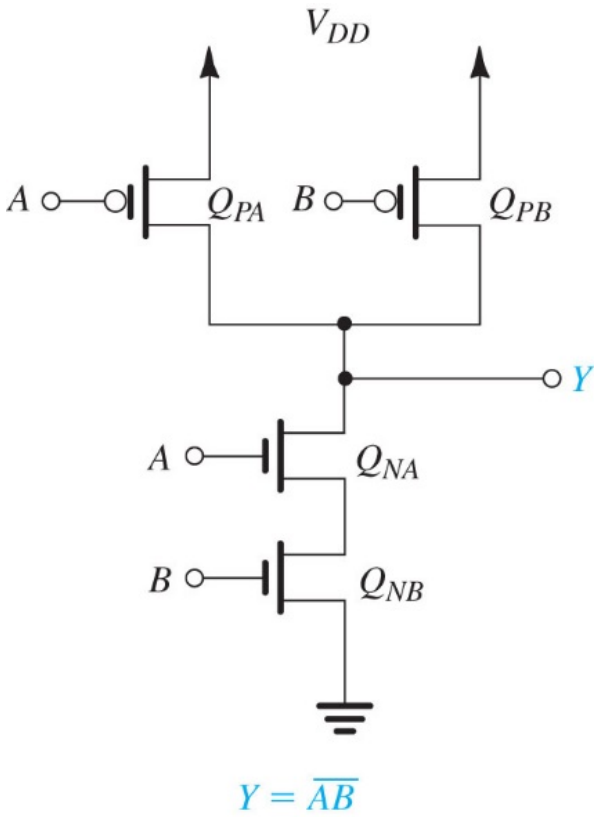


**Figure 14.8** A two-input CMOS NAND gate.

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# Example: a composite CMOS gate

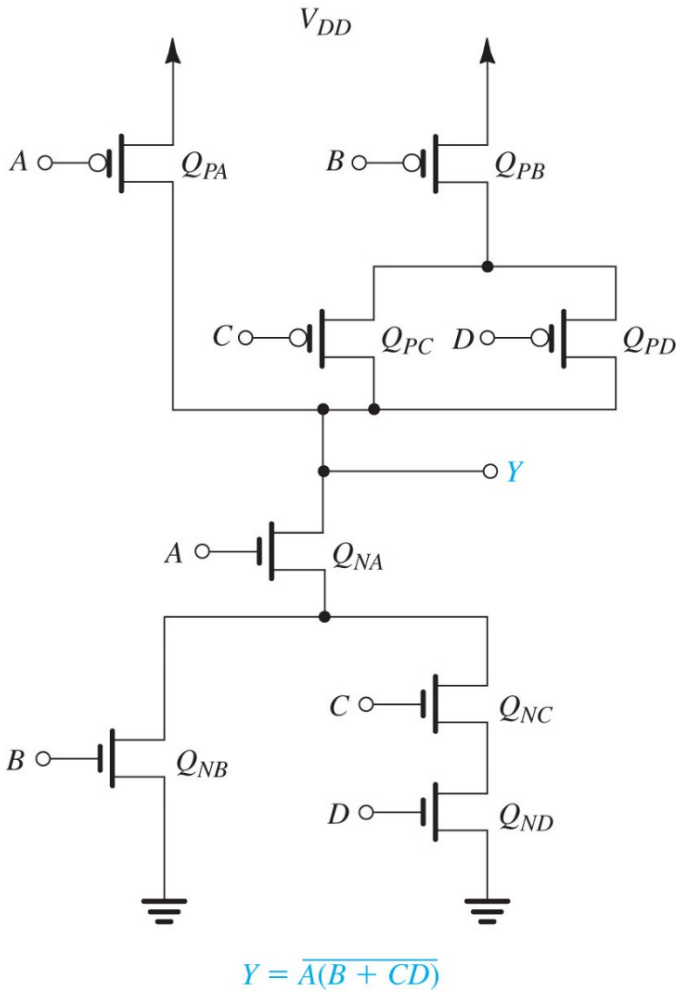


**Figure 14.9** CMOS realization of a complex gate.

| A | B | C | D | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |


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# CMOS inverter: logic symbol, implementation, and simplified model

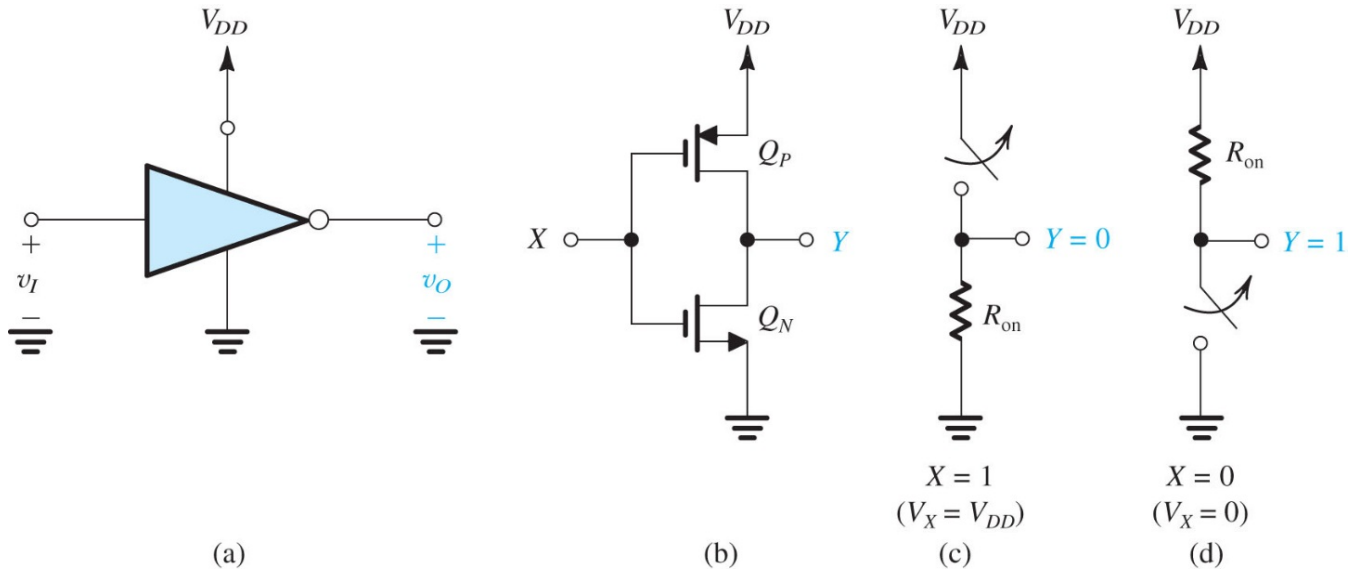


**Figure 14.2** (**a**) Block representation of the logic inverter; (**b**) its CMOS realization; (**c**) operation when the input is a logic 1; (**d**) operation when the input is a logic 0.

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# DC transfer characteristic of the ideal inverter

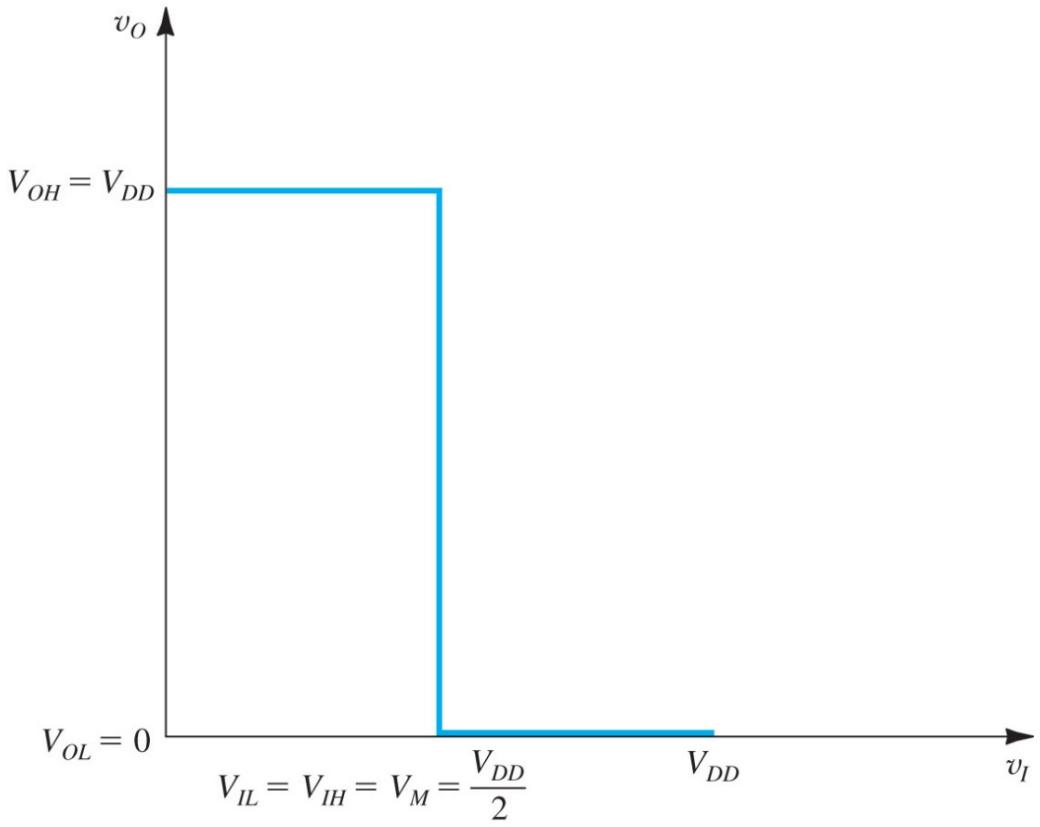


**Figure 14.16** The VTC of an ideal inverter.

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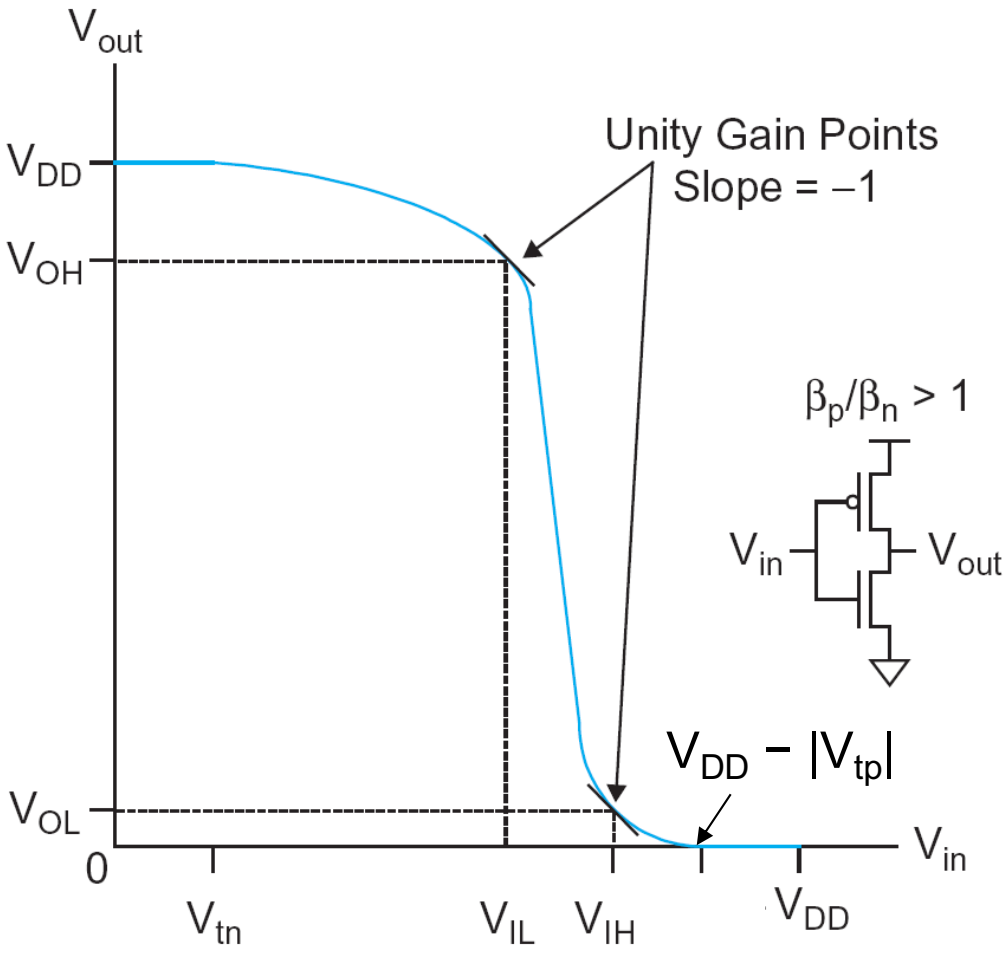
# DC transfer characteristic of “real” inverter




Typical voltage-transfer characteristic (VTC) of a logic inverter, illustrating the definition of the critical points.

# DC parameters of the logic inverter

**Table 14.1** Important Parameters of the VTC of the Logic Inverter (Refer to Fig. 14.13)

| | |
|---|---|
| $V_{OL}$: | Output low level |
| $V_{OH}$: | Output high level |
| $V_{IL}$: | Maximum value of input interpreted by the inverter as a logic 0 |
| $V_{IH}$: | Minimum value of input interpreted by the inverter as a logic 1 |
| $NM_L$: | Noise margin for low input $= V_{IL} - V_{OL}$ |
| $NM_H$: | Noise margin for high input $= V_{OH} - V_{IH}$ |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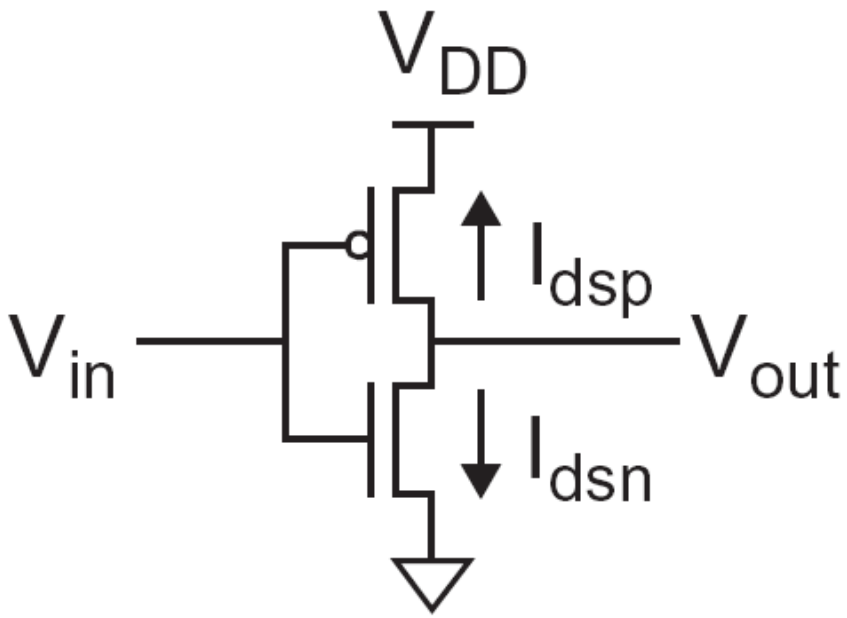
# Implementation of CMOS inverter



# CMOS inverter with $v_I$ = VDD

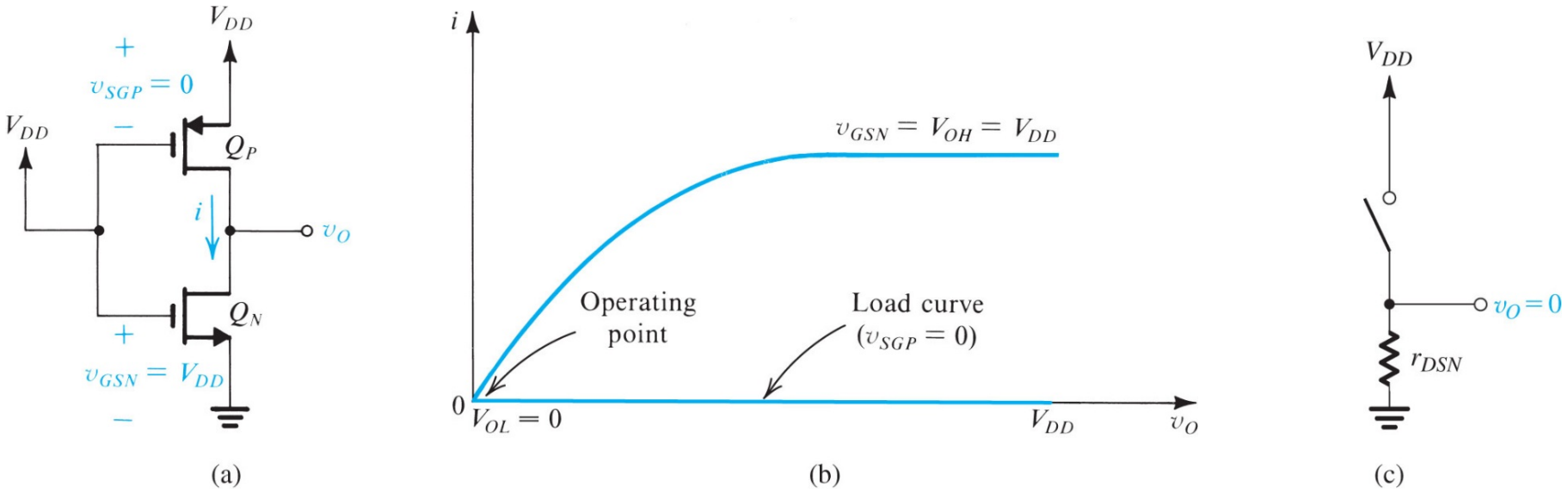



**Figure 14.23** Operation of the CMOS inverter when $v_I$ is high: **(a)** circuit with $v_I = V_{DD}$ (logic-1 level, or $V_{OH}$); **(b)** graphical construction to determine the operating point; **(c)** equivalent circuit.

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# CMOS inverter with $v_I$ = GND

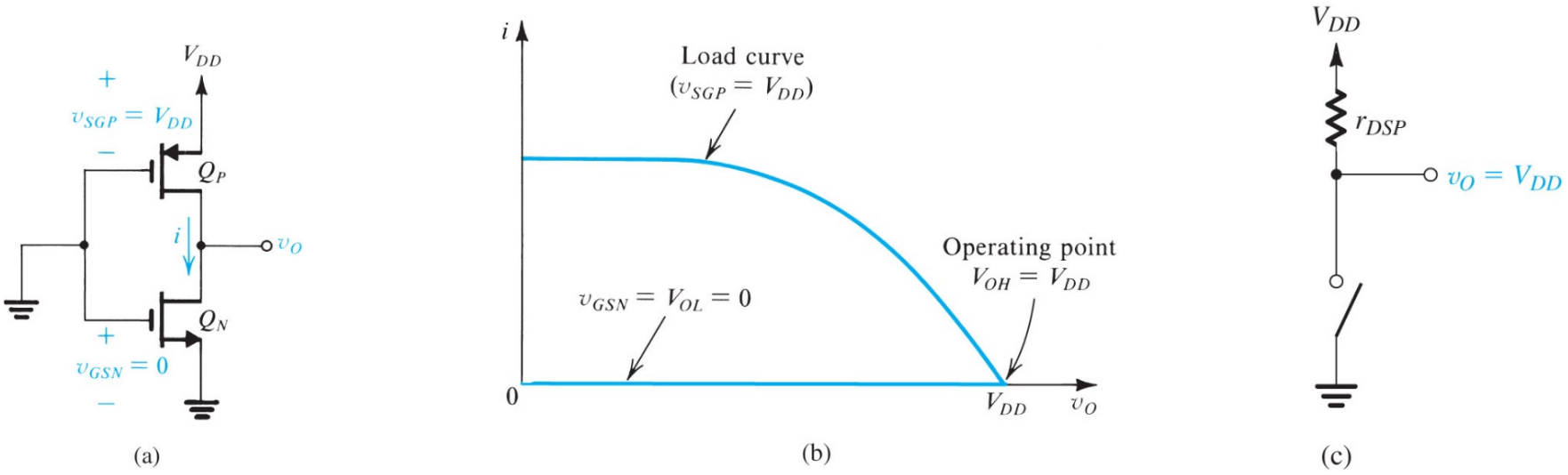


**Figure 14.24** Operation of the CMOS inverter when $v_I$ is low: **(a)** circuit with $v_I = 0$ V (logic-0 level, or $V_{OL}$); **(b)** graphical construction to determine the operating point; **(c)** equivalent circuit.

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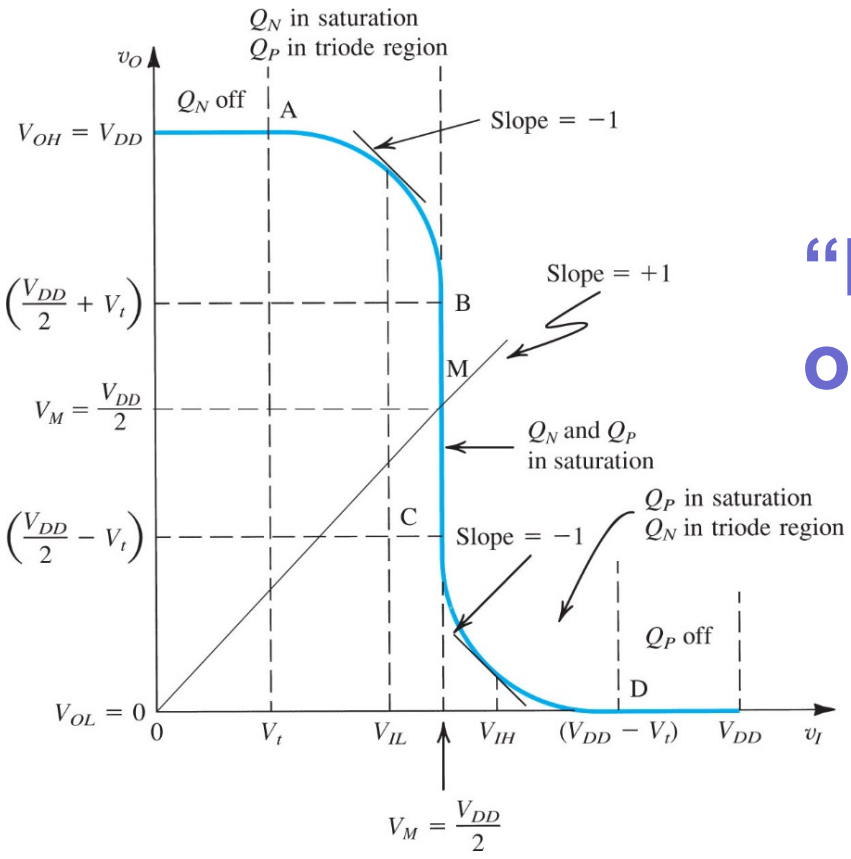
# DC transfer characteristic of a "real" inverter (with $Q_P$ and $Q_N$ matched)

$v_O$ vs. $v_I$




"Robustness" of the inverter

**Figure 14.25** The voltage-transfer characteristic of the CMOS inverter when $Q_N$ and $Q_P$ are matched.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# “Robustness” of the inverter

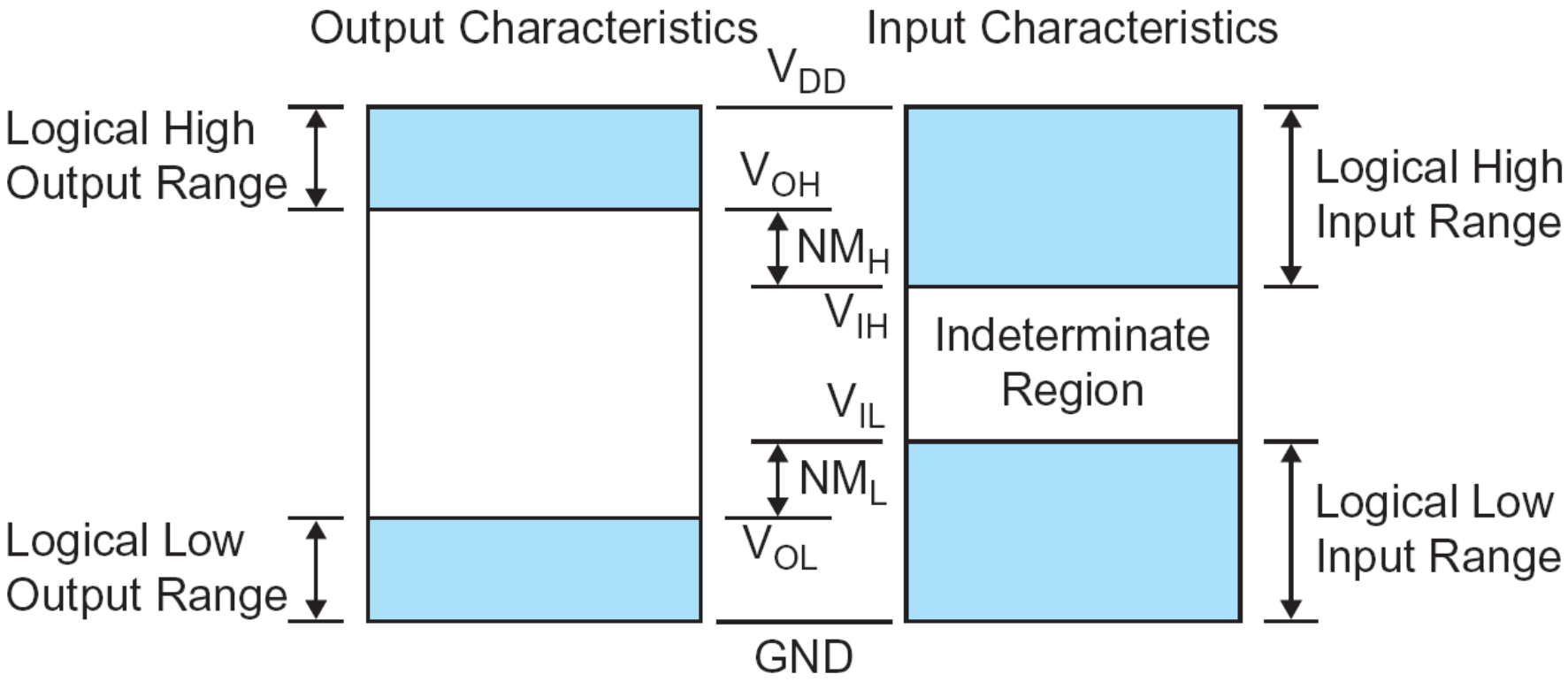
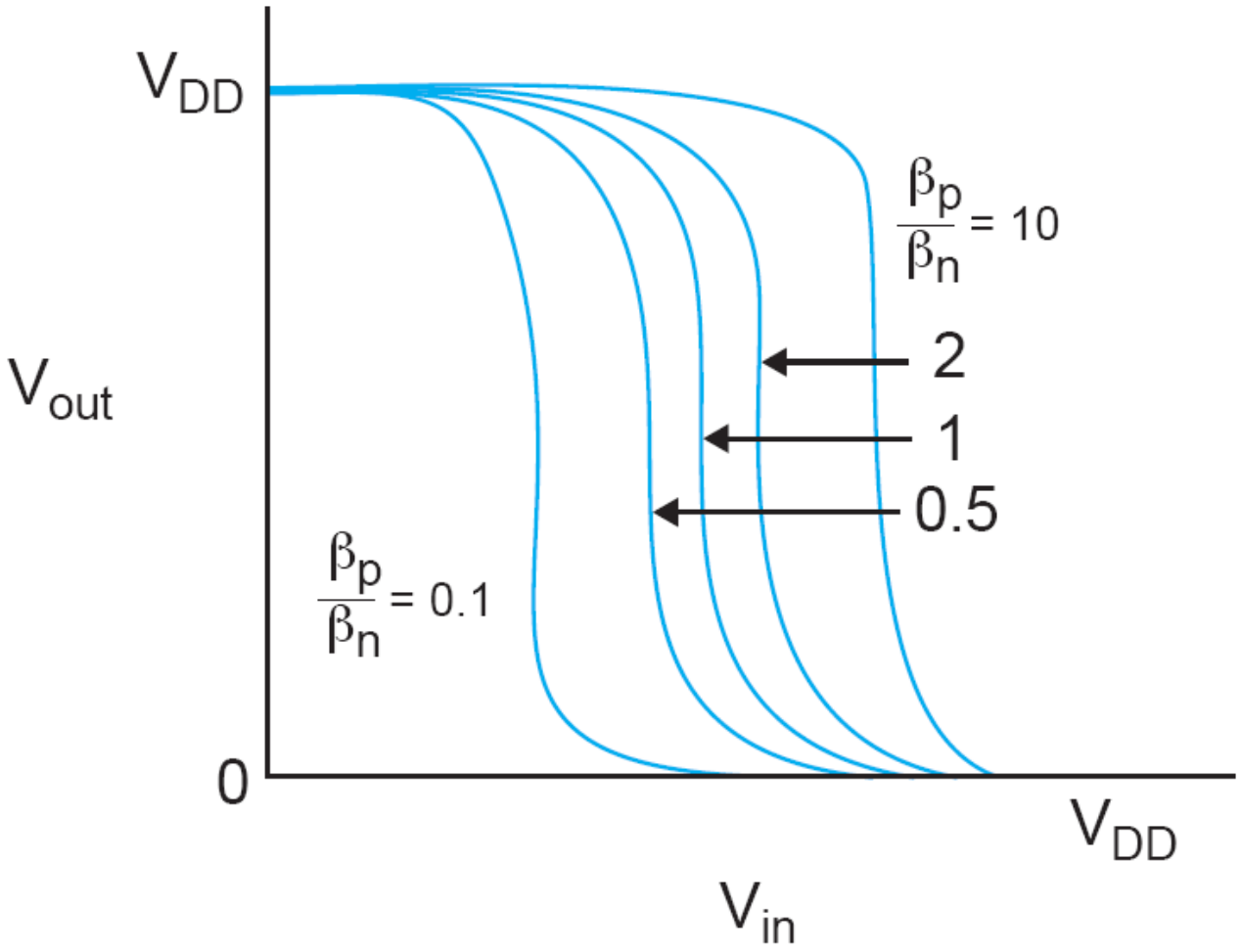



**FIGURE 2.29** Noise margin definitions

# DC transfer characteristic of a "real" inverter (with $Q_P$ and $Q_N$ mismatched)



# Speed of the logic inverter (Transient behavior)

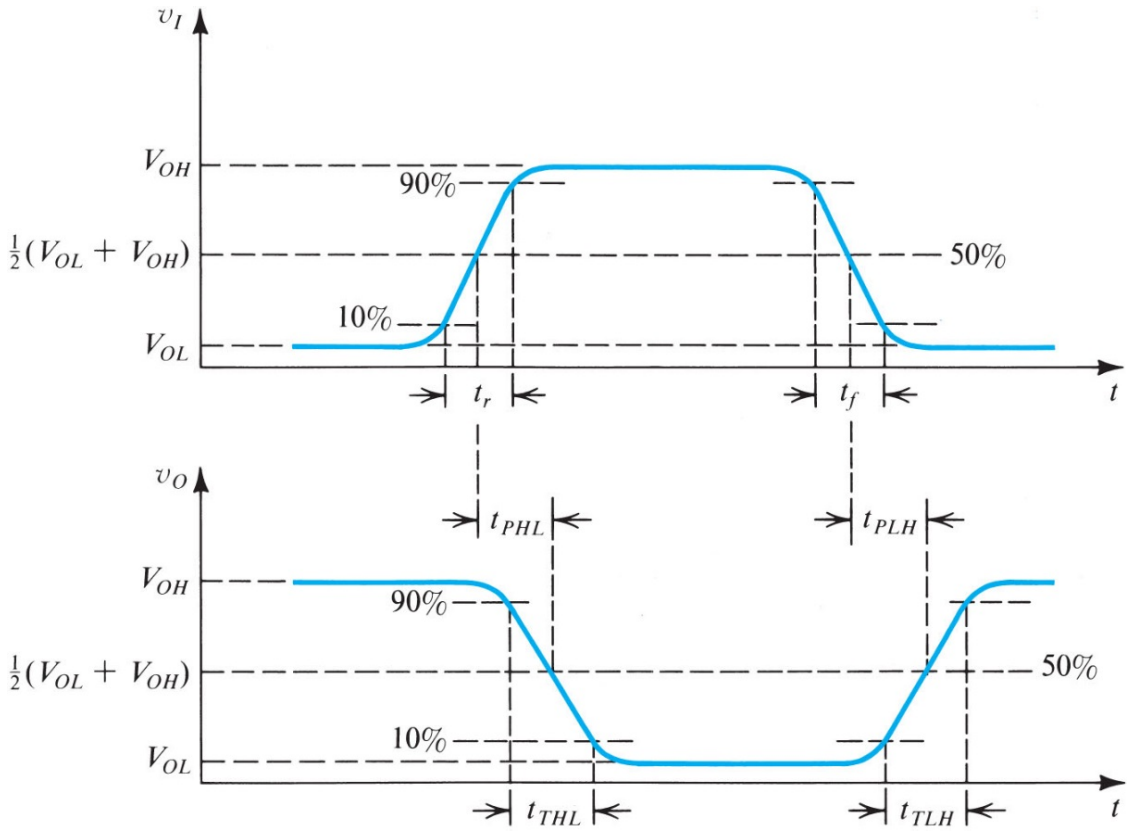



**Figure 14.29** Definitions of propagation delays and transition times of the logic inverter.

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