Introduction to CMOS
Digital Logic Circuits
MOSTs as switches

For a transistor in triode region if $V_{GS} - V_t \ll V_{DS}$:

$$R_{on} \equiv R_{DS} \approx \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_t)}$$

Figure 14.1 Operation of the (a) NMOS and (b) PMOS transistor as an on/off switch. The gate voltage controls the operation of the transistor switch, with the voltage $V_{DD}$ representing a logic 1 and 0 V representing a logic 0. Note that the connections of the drain and source terminals are not shown.
The CMOS inverter

Figure 14.2 (a) Block representation of the logic inverter; (b) its CMOS realization; (c) operation when the input is a logic 1; (d) operation when the input is a logic 0.
General CMOS logic gate structure

The PUN and the PDN are complementary.

The PUN is made only of pMOSTs.

The PDN is made only of nMOSTs.
Examples of pull-down networks

Figure 14.4 Examples of pull-down networks.
Examples of pull-up networks

Figure 14.5 Examples of pull-up networks.
MOSTs symbols used in “digital logic”

The body terminal of all pMOSTs is “assumed” connected to VDD.

The body terminal of all nMOSTs is “assumed” connected to GND.
Example: CMOS NOR gate

Figure 14.7 A two-input CMOS NOR gate.

\[ Y = \overline{A + B} \]
Example: CMOS NAND gate

Figure 14.8 A two-input CMOS NAND gate.
Example: a composite CMOS gate

Figure 14.9 CMOS realization of a complex gate.
CMOS inverter: logic symbol, implementation, and simplified model

Figure 14.2 (a) Block representation of the logic inverter; (b) its CMOS realization; (c) operation when the input is a logic 1; (d) operation when the input is a logic 0.
DC transfer characteristic of the ideal inverter

\[ V_{OH} = V_{DD} \]

\[ V_{OL} = 0 \]

\[ V_{IL} = V_{IH} = V_{M} = \frac{V_{DD}}{2} \]

\[ V_{DD} \]

**Figure 14.16** The VTC of an ideal inverter.
DC transfer characteristic of “real” inverter

Typical voltage-transfer characteristic (VTC) of a logic inverter, illustrating the definition of the critical points.
DC parameters of the logic inverter

Table 14.1 Important Parameters of the VTC of the Logic Inverter (Refer to Fig. 14.13)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
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<tbody>
<tr>
<td>$V_{OL}$</td>
<td>Output low level</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output high level</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Maximum value of input interpreted by the inverter as a logic 0</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Minimum value of input interpreted by the inverter as a logic 1</td>
</tr>
<tr>
<td>$NM_L$</td>
<td>Noise margin for low input = $V_{IL} - V_{OL}$</td>
</tr>
<tr>
<td>$NM_H$</td>
<td>Noise margin for high input = $V_{OH} - V_{IH}$</td>
</tr>
</tbody>
</table>
Implementation of CMOS inverter
CMOS inverter with $v_I = V_{DD}$

**Figure 14.23** Operation of the CMOS inverter when $v_I$ is high: (a) circuit with $v_I = V_{DD}$ (logic-1 level, or $V_{OH}$); (b) graphical construction to determine the operating point; (c) equivalent circuit.
CMOS inverter with $v_i = \text{GND}$

**Figure 14.24** Operation of the CMOS inverter when $v_i$ is low: (a) circuit with $v_i = 0$ V (logic-0 level, or $V_{OL}$); (b) graphical construction to determine the operating point; (c) equivalent circuit.
DC transfer characteristic of a “real” inverter (with $Q_P$ and $Q_N$ matched)

$v_O$ vs. $v_I$

“Robustness” of the inverter

Figure 14.25 The voltage-transfer characteristic of the CMOS inverter when $Q_N$ and $Q_P$ are matched.
“Robustness” of the inverter

**FIGURE 2.29** Noise margin definitions
DC transfer characteristic of a “real” inverter (with $Q_P$ and $Q_N$ mismatched)
Speed of the logic inverter (Transient behavior)

**Figure 14.29** Definitions of propagation delays and transition times of the logic inverter.