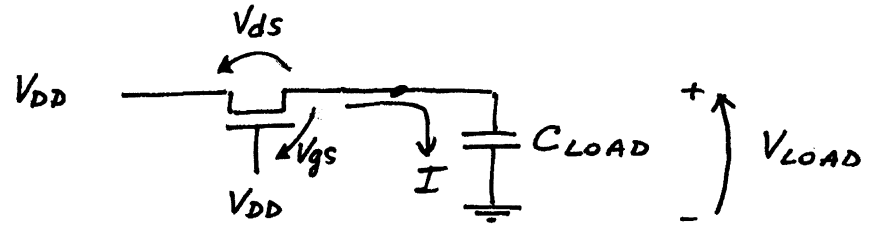
nMOS pass transistor

Let's consider we want to pass a logic one to a load through an nMOS switch.



We assume that C_{LOAD} is initially uncharged The pass transistor is in saturation region (at the beginning $V_{gs} = V_{ds} = V_{DD}$ so $V_{ds} > V_{gs} - V_T$. What about later ? Are we still in saturation or not ?)

$$I = C_{LOAD} \cdot \frac{dV_{LOAD}}{dt}$$

$$\frac{\beta}{2} \left(\underbrace{V_{DD} - V_{LOAD}}_{V_{gs}} - V_T \right)^2 = C_{LOAD} \cdot \frac{dV_{LOAD}}{dt}$$

$$dt = \frac{C_{LOAD} \cdot 2}{\beta \left(V_{DD} - V_{LOAD} - V_T \right)^2} \cdot dV_{LOAD}$$

$$\int_0^t dt = \frac{2 \cdot C_{LOAD}}{\beta} \int_0^{V_{LOAD}} \frac{dV_{LOAD}}{\left(V_{DD} - V_{LOAD} - V_T \right)^2}$$

Recalling Calculus

$$\int x^n dx = \frac{x^{n+1}}{n+1} + C$$

$$t = \frac{2 \cdot C_{LOAD}}{\beta} \left[\frac{1}{V_{DD} - V_{LOAD} - V_T} \right]_0^{V_{LOAD}}$$

$$t = \frac{2 \cdot C_{LOAD}}{\beta} \left[\frac{1}{V_{DD} - V_{LOAD} - V_T} - \frac{1}{V_{DD} - V_T} \right]$$

$$t = \frac{2\, C_{LOAD}}{\beta} \left[\frac{V_{DD} - V_T - V_{DD} + V_{LOAD} + V_T}{(V_{DD} - V_{LOAD} - V_T)(V_{DD} - V_T)} \right]$$

$$t = \frac{2\, C_{LOAD} \cdot V_{LOAD}}{\beta} \frac{1}{(V_{DD} - V_{LOAD} - V_T)(V_{DD} - V_T)}$$

$$t \cdot V_{DD} - t\, V_{LOAD} - t\, V_T = \frac{2\, C_{LOAD} \cdot V_{LOAD}}{\beta\, (V_{DD} - V_T)}$$

$$t (V_{DD} - V_T) = \frac{2 \cdot C_{LOAD} \cdot V_{LOAD}}{\beta\, (V_{DD} - V_T)} + t\, V_{LOAD}$$

$$t (V_{DD} - V_T) = \frac{2 \cdot C_{LOAD} \cdot V_{LOAD}}{\beta (V_{DD} - V_T)} + \frac{t \beta (V_{DD} - V_T) V_{LOAD}}{\beta (V_{DD} - V_T)}$$

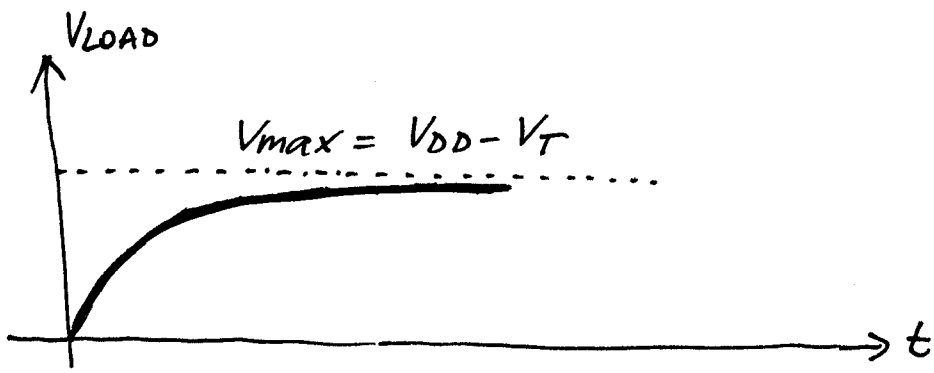
$$t (V_{DD} - V_t) = \frac{V_{LOAD} \left[2\, C_{LOAD} + t \beta (V_{DD} - V_T) \right]}{\beta (V_{DD} - V_T)}$$

$$V_{LOAD} = \frac{t \beta (V_{DD} - V_T)^2}{2\, C_{LOAD} + t \beta (V_{DD} - V_T)}$$

$$V_{LOAD} = (V_{DD} - V_T) \cdot \frac{t\beta (V_{DD} - V_T)}{2 C_{LOAD} + t\beta (V_{DD} - V_T)} =$$

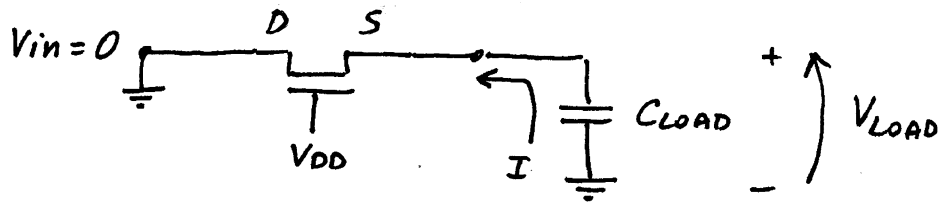
$$= (V_{DD} - V_T) \cdot \frac{1}{\frac{2 C_{LOAD}}{t\beta (V_{DD} - V_T)} + 1}$$

This result is very interesting, because shows us that we will never be able to charge the capacitor above $V_{DD} - V_T$ The nMOS transistor pass a "weak" logic 1 to the Load, in other words it is not a very good choice when we want To pass logic ones.



$$(V_{DD} - V_T) \cdot \frac{1}{\frac{2 C_{LOAD}}{t\beta (V_{DD} - V_T)} + 1} \xrightarrow[t \to \infty]{} V_{DD} - V_T$$

Let's now switch the input of our circuit from a logic 1 to a logic 0



Initially $V_{LOAD}(t=0) = V_{max} = V_{DD} - V_T$.
With $V_{gs} = V_{DD}$ and $V_{ds} = V_{max} = V_{DD} - V_T$ the transistor works in linear region
($V_{ds} < V_{gs} - V_T$)

$$-I = \beta \left[(V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

$$-I = \beta \left[(V_{DD} - V_T) V_{LOAD} - \frac{V_{LOAD}^2}{2} \right]$$

$$-C_{LOAD} \cdot \frac{dV_{LOAD}}{dt} = \beta \left[(V_{DD} - V_T) V_{LOAD} - \frac{V_{LOAD}^2}{2} \right]$$

$$\int_0^t dt = -\frac{C_{LOAD}}{\beta} \int_{V_{DD}-V_T}^{V_{LOAD}} \left[\frac{1}{(V_{DD} - V_T) V_{LOAD} - \frac{V_{LOAD}^2}{2}} \right] dV_{LOAD}$$

....

Solving the equation we will get the following result:

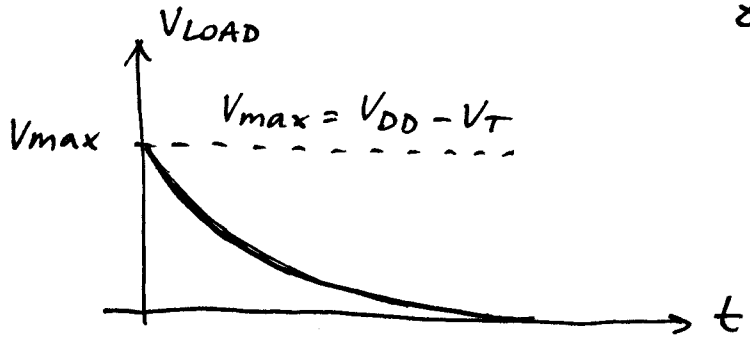
$$V_{LOAD} = (V_{DD} - V_T)\,\frac{2 \cdot e^{-t/\tau}}{1 + e^{-t/\tau}}$$

where the discharge constant time τ is:

$$\tau = \frac{C_{LOAD}}{\beta (V_{DD} - V_T)}$$

The interesting thing to notice is that:

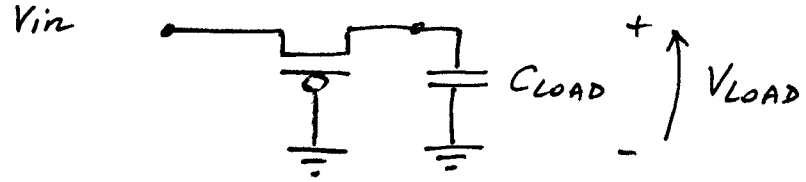
$$V_{LOAD}(t \to \infty) = (V_{DD} - V_T)\,\frac{2 \cdot \overbrace{e^{-t/\tau}}^{t \to \infty \;\to\; 0}}{1 + \underbrace{e^{-t/\tau}}_{\tau \to \infty \;\to\; 0}} = 0$$



Unlike the previous case we see that the n-MOS transistor is able to pass a low voltage (logic ϕ) without any problem.

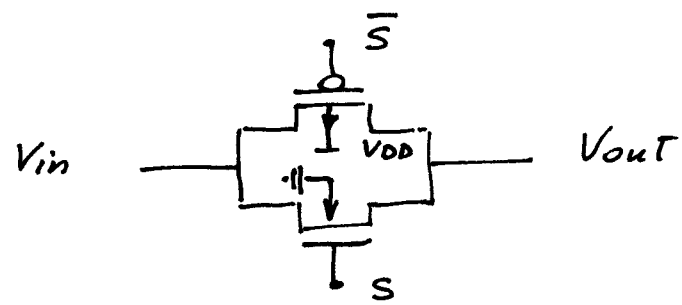
pMOS pass transistor

If we repeat the analysis done for the n-MOS transistor to the p-MOS transistor we will find out that through the use of the pMOS we can pass without any problem a logic 1 but we have trouble passing a logic ϕ (V_{LOAD} cannot go below a $V_{min} = |V_T|$)

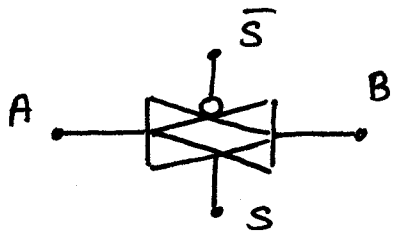


Transmission Gate

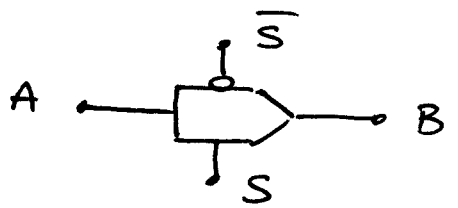
The goal is to build a gate able to transmit "well" both logic ϕ and logic 1 to a load.
Recalling how nMOS and pMOS pass transistors works, we can easily see that we can achieve the transmission gate combining an n-MOS and a p-MOS.



The P-MOS takes care of passing logic 1 while the nMOS takes care of passing logic 0.

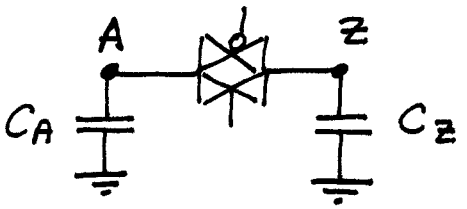


Transmission Gate symbol

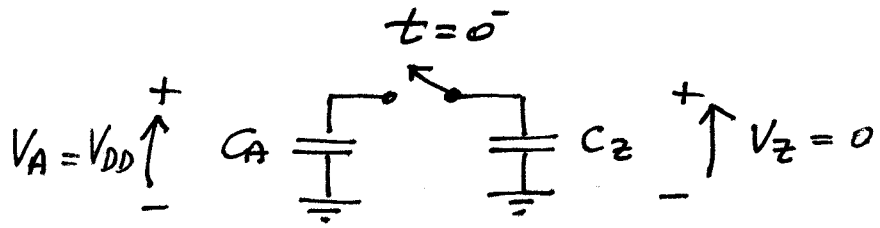


another transmission gate symbol

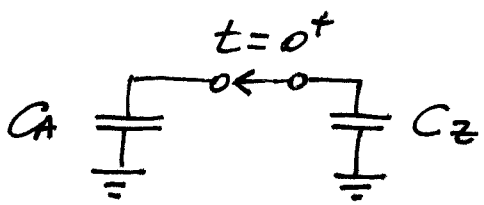
Charge Sharing problem



Suppose that C_Z is pretty big, while C_A is pretty small.
Let's assume that initially C_A is charged at V_{DD}, C_Z is uncharged, and the transmission gate is OFF.



Now, imagine we want to transfer the logic "1" from node A to node Z, switching the transmission gate ON



for $t<0 \rightarrow Q_{TOTAL} = C_A \cdot V_{DD}$

for $t>0 \rightarrow Q_{TOTAL} = (C_A + C_Z)\, V_{FINAL}$

$$C_A \cdot V_{DD} = (C_A + C_Z) \cdot V_{FINAL}$$

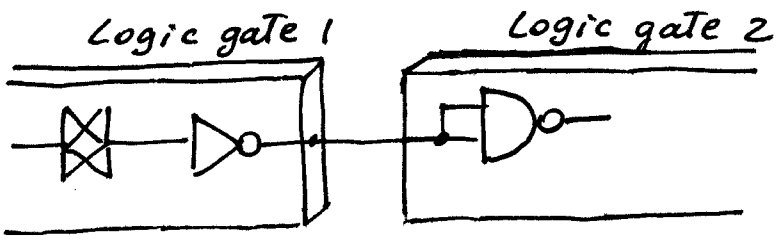
$$V_{FINAL} = V_{DD} \frac{C_A}{C_A + C_Z} \approx 0$$

$C_Z \gg C_A$

which is not at all what we wanted to achieve

The charge is shared between node A and Z. In order to solve this problem we must make sure that $C_A \gg C_Z$ (as rule of thumb $C_A > 10 \cdot C_Z$).

Typically in a logic cell no transmission gate is allowed to directly drive another logic cell (an insulation buffer is included)



Cout = 2pF
Cin = 0.02pF

typical values for a 0.5μ process