Lecture 10

Introduction to Data Conversion

Plan:

- Digital Processing of signals (vs. Analog Processing)
- Sampling of analog signals
- Quantization error
- ADC and DAC basic principle
- DAC converter circuit with binary-weighted resistors
- Two ADC converter circuits
  - Flash ADC
  - counter based tracking ADC

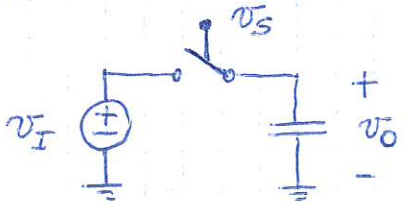
Digital Processing of Signals

- Most physical signals exist in analog form. However, an attractive alternative to process them, it is to convert them in digital form and carry the processing digitally (digital signal processing).
- There are a number of techniques and circuits to convert an analog signal to digital form (analog-to-digital or simply A/D conversion) and to convert a digital to analog form (digital-to-analog or simply D/A conversion).

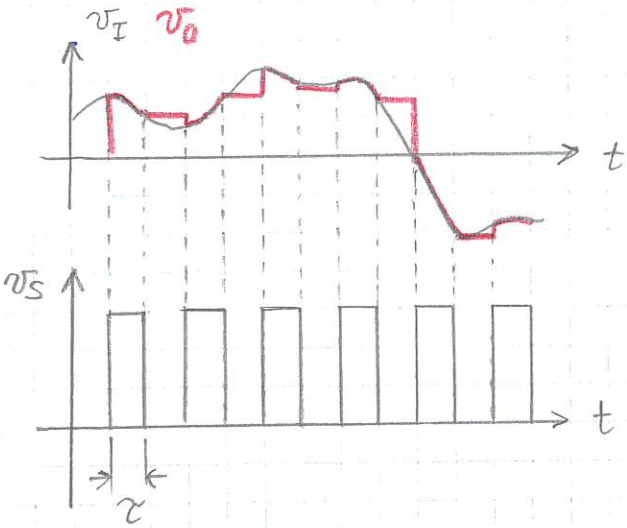
Sampling of Analog Signals

- The basic principle underlying digital signal processing is that of sampling the analog signal.

The fact that we can do our processing on a limited number of samples of an analog signal while ignoring the analog signal details between samples is based on the Shannon's sampling theorem.



sample-and-hold (S/H) circuit.



input analog signal

output signal to be fed to ADC

sampling-signal controlling the switch
(the switch closes for a small part τ of every clock period T)

Signal Quantization

- Consider an analog signal whose values range from 0 to +10V. Let's assume that we wish to convert this signal to digital form using a 4-bit digital signal → we know that a 4-bit binary number can represent 16 different values (0 to 15) → it follows that the resolution of our conversion will be $\frac{10V}{15} = \frac{2}{3}V$ → Thus an analog signal value of 0V will be represented by 0000, 2/3V will be represented by 0001, 6V will be represented by 1001 ($= \frac{6V}{2/3V} = 9 \leftrightarrow 1001$), and 10V will be represented by 1111.

  → all these sample numbers are multiples of the basic increment 2/3V (resolution)

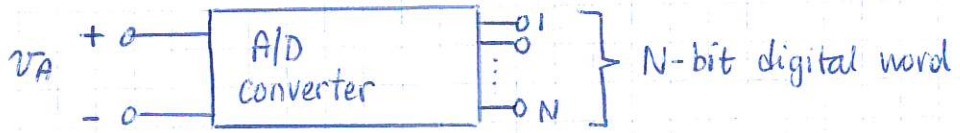
- What happen if the voltage to convert falls between successive incremental levels ?

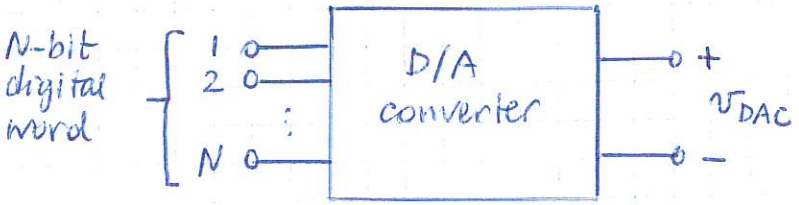
  Consider the case of a 6.2V analog level. This falls between 18/3 and 20/3 → we treat it as if it were 6V and code it as 1001 ($\frac{18}{3} = 6V \rightarrow \frac{6V}{2/3V} = 9 \leftrightarrow 1001$)

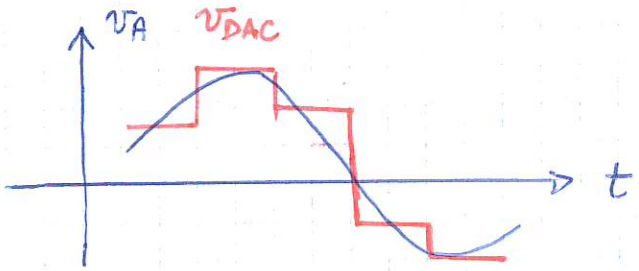
  → This inherent error in the conversion process is called quantization error

- Using more bits to represent an analog circuit reduces quantization errors but requires more complex circuitry.

ADC and DAC as functional blocks







the staircase waveform at the output of a DAC can be filtered to obtain a smoother waveform (→ through a LPF). ⟹ the filter will introduce a time delay.

Example

An analog signal in the range 0 to +10V is to be converted to an 8-bit digital signal.

a. What is the resolution of the conversion in V?
b. What is the digital representation of an input of 6V?
c. What is the representation of an input of 6.2V?
d. What is the quantization error (in absolute terms and as a % of the input) of 6.2V?
e. What is the quantization error of 6.2V as a percentage of full scale?
f. What is the largest possible quantization error as a percentage of full scale?

$$\text{Resolution} = \frac{FSR}{2^N - 1} = \frac{V_{HIGH} - V_{LOW}}{2^N - 1}$$

FSR = full scale range

V_{HIGH} = upper-voltage extreme

V_{LOW} = lower-voltage extreme

N = number-of-bits of the converter (a.k.a. resolution in bits)

$M = 2^N - 1$ = number of voltage intervals

(a) $\text{Resolution} = \frac{10V - 0V}{255} = 0.0392\ V$

(b) $D = \left\lfloor \frac{V_{in}}{\text{Resolution}} \right\rfloor = \left\lfloor \frac{6}{0.0392} \right\rfloor = \left\lfloor \frac{6}{10/255} \right\rfloor = \lfloor 153.06 \rfloor =$

$= 10011001_2 \leftarrow 153_{10}$ in binary

(c) $D = \left\lfloor \frac{6.2}{10/255} \right\rfloor = \lfloor 158.1 \rfloor = 10011110_2 \leftarrow 158_{10}$ in binary

(d) $E_q = D \times \text{Resolution} - V_{in} = 158 \times 0.0392 - 6.2 = -0.0064$

$E_q\% = 100 \times \frac{E_q}{V_{in}} = 100 \times \frac{-0.0064}{6.2} = -0.1\%$

(e) $\frac{E_q}{FSR}\% = 100 \times \frac{E_q}{FSR} = 100 \times \frac{-0.0064}{10} = -0.064\%$

(f) The largest possible quantization error is $\pm \frac{1}{2}$ Resolution.

$|E_{q_{max}}| = \frac{1}{2}\text{Resolution} = \frac{1}{2} \times 0.0392 = 0.0196$

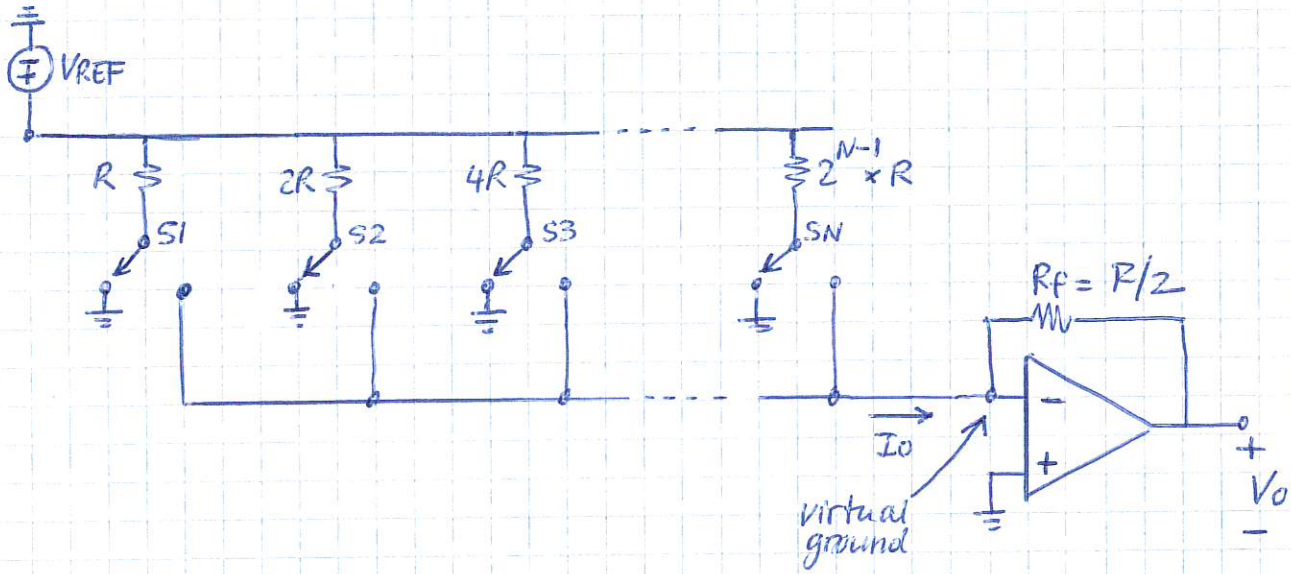
$\frac{|E_{qmax}|}{FSR}\% = 100 \times \frac{|E_{qmax}|}{FSR} = 100 \times \frac{0.0196}{10} = 0.196\%$

Basic D/A Converter Circuit

- The simplest circuit for an N-bit D/A converter consists of a reference voltage V_{REF}, N binary-weighted resistors ($R, 2R, 4R, \dots 2^{N-1}R$) and an opamp with its feedback resistance $R_F = R/2$.

- The key idea is to create an analog output voltage that is proportional to the input binary word $b_1 \dots b_N$ at the input

b_1 (MSB) ... b_N (LSB)



The switches are controlled by an N-bit digital input $b_1 b_2 \dots b_N$. The total current I_O that will flow through the feedback resistor of the op. amp is proportional to the digital word.

$$I_O = \frac{V_{REF}}{R} b_1 + \frac{V_{REF}}{2R} b_2 + \dots \frac{V_{REF}}{2^{N-1} \cdot R} \cdot b_N =$$

$$= \frac{2\,V_{REF}}{R} \left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \dots + \frac{b_N}{2^N} \right)$$

so if we select $R_F = R/2$ the output voltage level is:

$$V_O = -I_O \cdot R_F = -I_O \cdot \frac{R}{2} = -\frac{V_{REF}}{R} \left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \dots + \frac{b_N}{2^N} \right)$$

- It should be noted that the accuracy of the DAC depends critically on
  (1) the accuracy of V_{REF}
  (2) the precision of the binary-weighted resistors
  (3) the perfection of the switches

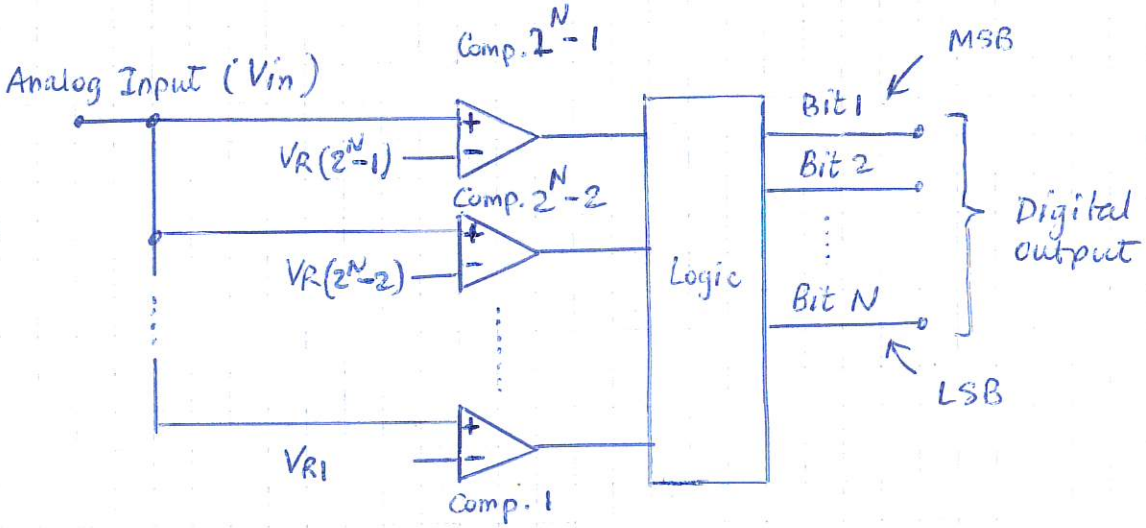
- In practice the circuit implementation of the DAC rely on binary-weighted currents generated by current sources rather than resistors

Basic A/D converter circuits

- There exists a number of A/D conversion techniques (varying in complexity and speed).
  We will see two schemes: one simple but slow (Feedback type converter) and one complex (in terms of amount of circuitry required) but extremely fast (Parallel or Flash converter)

- Parallel (a.k.a. Flash) Converter

Conceptually, flash conversion is very simple. It uses $2^N - 1$ comparators to compare the input signal level with each of the $2^N - 1$ possible quantization levels.



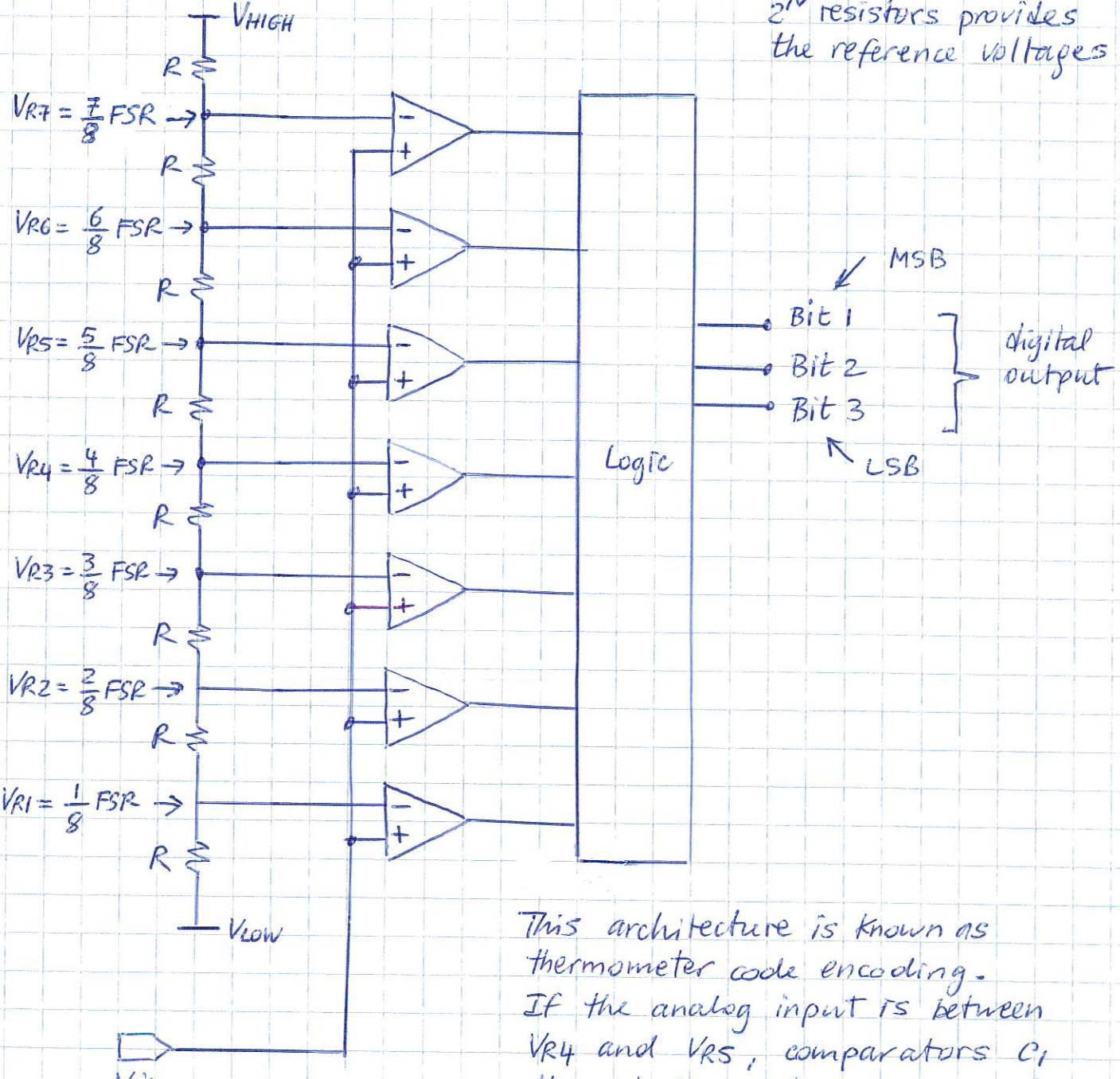
The outputs of the comparators are processed by an encoder block to provide the N bits of the output digital word.
A complete conversion can be obtained within one clock cycle, but we need a huge # of comparators ($2^N - 1$ comparators for N-bit)

If the analog input is between V_{R4} and V_{R5} comparators C_1 through C_4 produce Ones and the remaining comparators produce zeros ($\rightarrow$ thermometer architecture)

Example

Design the resistor ladder needed to generate the reference voltages required by the comparators of a 3-bit flash ADC.

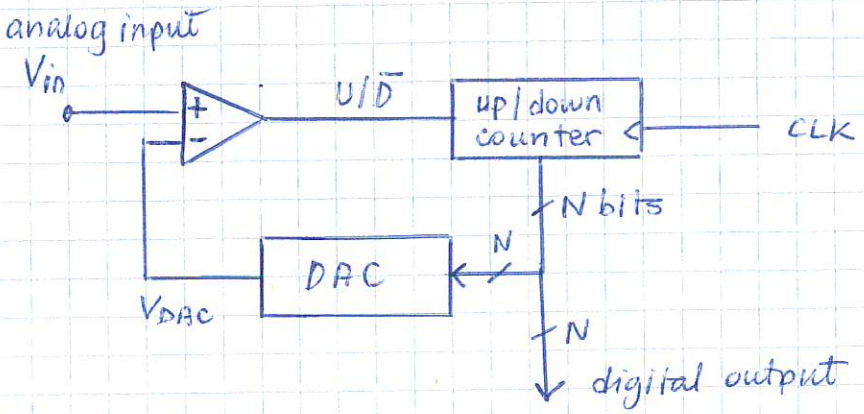
$N = 3 \rightarrow 2^N - 1 = 7$ comparators $\rightarrow$ A resistive divider with 2^N resistors provides the reference voltages



This architecture is known as thermometer code encoding. If the analog input is between V_{R4} and V_{R5}, comparators C_1 through C_4 produce ones and the remaining comparators produce zeros.

$FSR = V_{HIGH} - V_{LOW}$

The Feedback-type A/D converter (a.k.a. counter type converter)



source:
Tietze & Schenk
Electronic Circuits
Springer
pp. 975-976

The comparator compares the input voltage V_{in} with the voltage level V_{DAC}. If the difference is positive, it causes the counter to count upwards otherwise it counts downwards.
This means that the voltage level V_{DAC} rises or falls until it has reached the level of the input voltage V_{in}, and then follows the latter as it changes. (For this reason the circuit is also known as a tracking A/D converter)

One drawback with this simple circuit is that, as the clock is never switched off, the counter never stops so it oscillates by 1 LSB around the input voltage. Another issue to be aware of is that if V_{in} goes above the level V_{High} or below the level V_{Low} of the DAC, because the counter never stops its output value will roll over causing the conversion process to start over rather than tracking.