EE304 – Problem Set 3

Problem 12.1 [S&S 7/e]

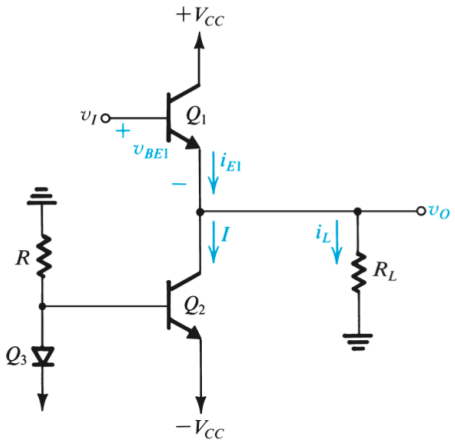

Figure 12.2 An emitter follower (Q_1) biased with a constant current I supplied by transistor Q_2.

12.1 A class A emitter follower, biased using the circuit shown in Fig. 12.2, uses $V_{CC}=10$ V, $R = R_L=1$ kΩ, with all transistors (including Q_3) identical. Assume $V_{BE}=0.7$ V, $V_{CE\,sat}=0.3$ V, and β to be very large. For linear operation, what are the upper and lower limits of output voltage, and the corresponding inputs? How do these values change if the emitter–base junction area of Q_3 is made twice as big as that of Q_2? Half as big?

Problem 12.2 [S&S 7/e]

12.2 A source-follower circuit using NMOS transistors is constructed following the pattern shown in Fig. 12.2. All three transistors used are identical, with $V_t=0.5$ V and $\mu_n C_{ox} W/L = 20\ \text{mA/V}^2$; $V_{CC}=2.5$ V, $R=R_L=1$ kΩ. For linear operation, what are the upper and lower limits of the output voltage, and the corresponding inputs?

Problem 12.10 [S&S 7/e]

12.10 Consider the feedback configuration with a class B output stage shown in Fig. 12.9. Let the amplifier gain $A_0 =$ 100 V/V. Derive an expression for v_O versus v_I, assuming that $|V_{BE}| = 0.7$ V. Sketch the transfer characteristic v_O versus v_I, and compare it with that without feedback.

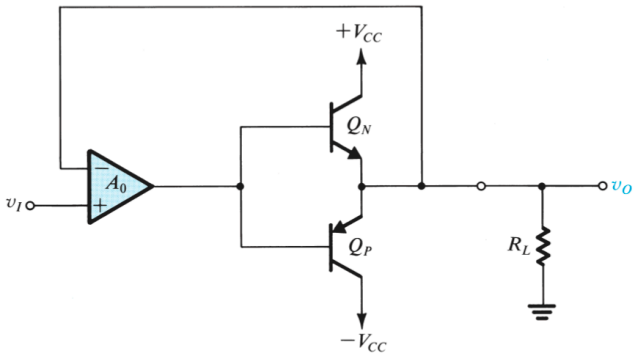

Figure 12.9 Class B circuit with an op amp connected in a negative-feedback loop to reduce crossover distortion.

Problem 12.11 [S&S 7/e]

SIM **12.11** Consider the class B output stage, using MOSFETs, shown in Fig. P12.11. Let the devices have $|V_t| =$ 0.5 V and $\mu C_{ox} W/L = 2$ mA/V^2. With a 10-kHz sine-wave input of 5-V peak and a high value of load resistance, what peak output would you expect? What fraction of the sine-wave period does the crossover interval represent? For what value of load resistor is the peak output voltage reduced to half the input?

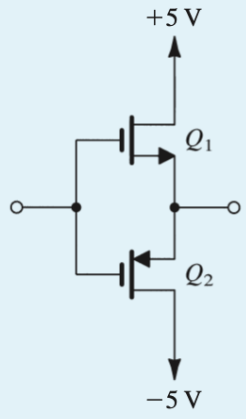

Figure P12.11