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Ground Bounce Primer

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In most circuits, the bypass capacitors connected between V_{cc} and the GND pin have a value of 0.01 or 0.1µF. But many electronics enthusiasts don't know why this bypass capacitor is used. Sometimes they ignore this capacitor and don't use it in their circuits. But this is a necessity for certain accurate calculation-based and delicate circuits.

If the bypass capacitor is omitted, then a problem called "ground bounce" begins to become an issue. This article will explain the ground bounce phenomenon and how a bypass capacitor prevents ground bounce.

To understand the concept of ground bounce, let's consider the typical output circuit shown in **Figure 1**. A and B are control inputs and turn on the NMOS transistor at high logic (more than 0.7V).

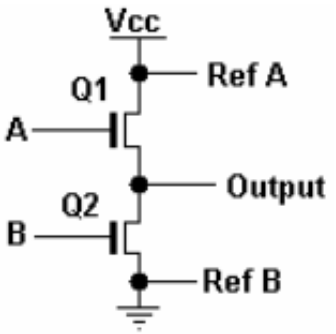

Figure 1: A typical output circuit

The output is high when Q2 turns off and Q1 turns on. Similarly, the output is low when Q2 turns on and Q1 turns off. When the signal transitions from high to low, Q2 provides a path for the current to flow from the output to ground. In most cases, the output load is capacitive, so the initial current spike is noteworthy. The output voltage is measured between the output pin of the device and Ref B, which is at ground. Similarly, when the output is high, Q2 turns off and Q1 turns on and the output voltage rises to V_{cc} less than the voltage drop across the device.

However, Ref A is not actually at V_{cc} and Ref B is not at ground. Ref A is the positive voltage point on the chip and Ref B is the ground on the chip. **Figure 2** illustrates that there is some inductance in the very small lead wires between the chip itself and the lead carrier of the package.

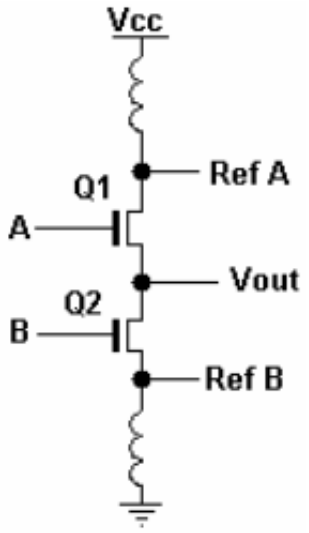

Figure 2: The effect of internal inductance

This inductance is very small, but it is significant. Consider what happens the moment Q2 turns on and Q1 turns off. A spike of current flows from the output through Q2 to ground. This current flows through the inductance in the lead. The voltage across this inductance (V Ref B) is directly related to the change in current as:

$$V = L * \frac{di}{dt} \quad \textbf{(1)}$$

di/dt is related to the rise (and/or fall) time of the device. The faster the rise and fall times, the smaller dt is, the greater di/dt (the change in current per unit time) is, and the higher the voltage drop is across any inductance. As Q2 turns on and the output voltage starts to fall, the voltage between the output and Ref B falls just as before. The voltage at Ref is relative to ground rises because of the current spike through the lead inductance. Thus, V_{out} does not fall all the way, but "bounces" above ground because of this inductive drop. This is the phenomenon called ground bounce.

You can eliminate ground bounce by using a bypass capacitor between V_{cc} and the ground rail as shown in **Figure 3**.

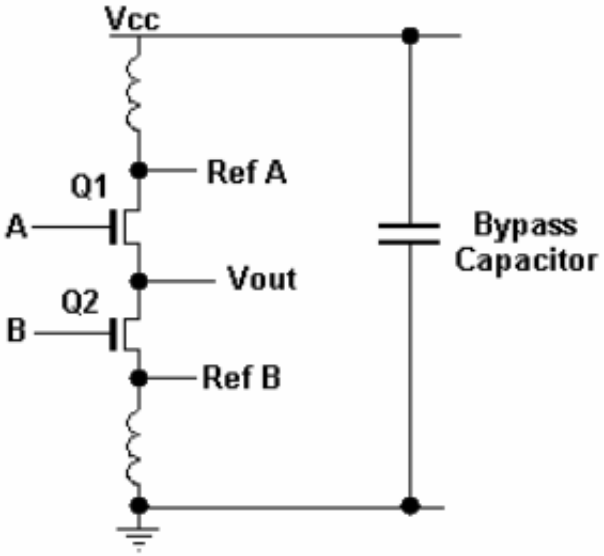

Figure 3: The bypass capacitor provides local

charge storage.

The purpose of a bypass capacitor is to provide something that looks like a regulated V_{cc} and ground right at the package for a short time until the inductance of the planes is overcome. With a well-calculated value of the bypass capacitor, the transient currents, which come into play when a device changes logic state, don't have to flow to and from the power supply, but flow to and from the bypass capacitor.

Another issue is the inductance of the capacitor leads. To avoid this, keep the capacitor as close as possible to the device you are protecting from ground bounce and use wide PCB traces to minimize the added inductance. Also, the copper tracks from the capacitor that lead to the V_{cc} plane and to the ground plane should be of same length. Ground bounce is difficult to analyze through EDA tools but you can minimize it on your end using proper design techniques.

About the Author
Vikas Kumar is a Signal Integrity Engineer at Logic Eastern. He has a Bachelors of Technology in Electronics and PG diploma in VLSI design. He has also experience in system design work in high speed SONET/SDH boards. He can be reached at emailtovkma@rediffmail.com.

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