EENGR 406 - Course Project

Using ON Semiconductor's C5 CMOS process

1. Design an op-amp that can operate with a VDD between 2 and 5 V while driving a 10 pF (max) and 1kΩ (min) load.

2. Other requirements are:
   - DC open-loop gain > 60 dB under all load and VDD conditions
   - Gain-bandwidth product should be > 100 MHz
   - Slew-rate with maximum load > 100V/microsecond

3. You will need to write a report (IEEE journal format) containing, at least, the following:
   - Simulations showing large- and small-signal operation, along with limitations, using +1 gain non-inverting and -1 gain inverting op-amp topologies
   - Show operation, including settling time and slewing, with no load and varying loads
   - Your detailed design considerations
   - Show schematics with a comparison between hand calculations and simulations along with comments
   - A table summarizing results such as input CMR as a function of VDD, unity-gain frequency, power, slew-rate, CMRR, PSRR, output swing as a function of VDD, etc.

4. You will be required to give a 10 minutes presentation of your work.

NOTE:
- Process information can be found at MOSIS.com, or at ON Semiconductor's website (http://www.onsemi.com/)
- SPICE models are in /usr/class/C5_models.mod